

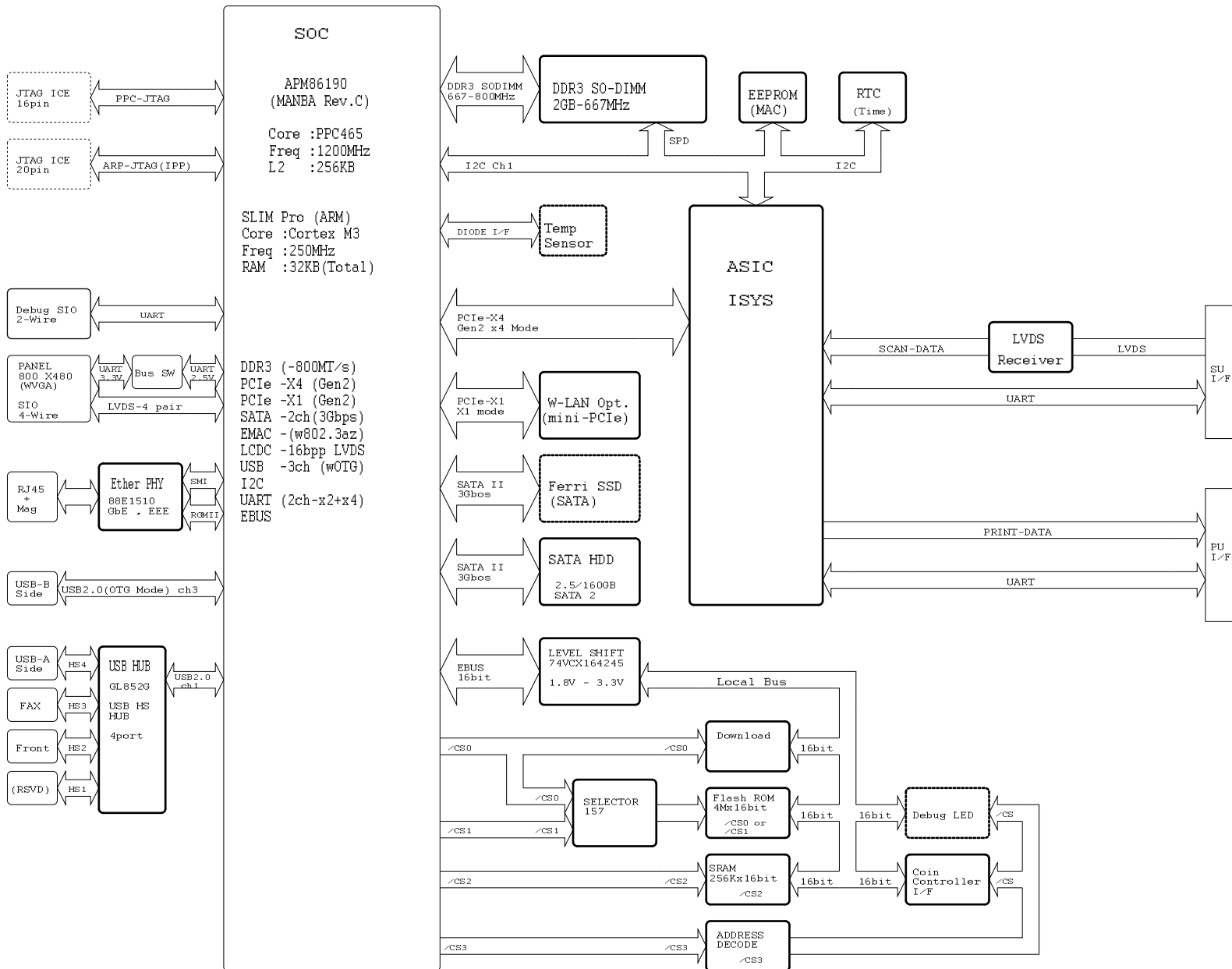
System Board
Circuit Diagram

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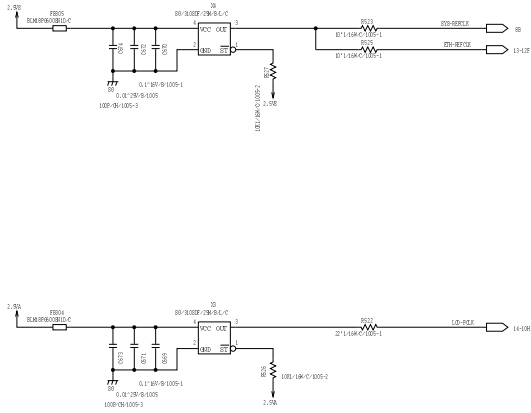
[Clock]
 SYS Ref : 25MHz
 Eth Ref : 25MHz
 CPU CORE : 1200MHz
 Memory : 667MHz (PC3-10600)
 RGMII : 125Mz
 PCIe Ref : 100MHz
 SATA Ref : 100MHz
 PCIe x4 : 50bps(Gen2)
 PCIe x1 : 2.5Gbps(Gen1)
 SATA : 3Gbps
 LCD : 33MHz
 I2C : 100KHz
 RTC : 32.768kHz

[UART baud rate]
 Debug : 57.6kbps
 Panel : 76.8kbps
 Scanner : 137.5kbps
 Printer : 68.75kbps

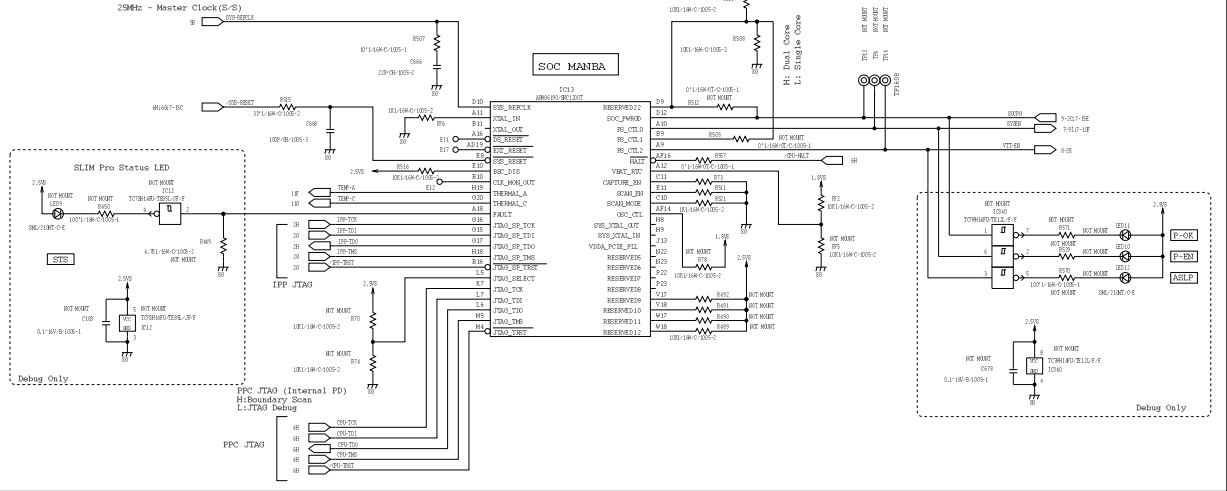
[Image Data Transfer Clock]
 Scanner : 48MHz SDR
 Printer : 19MHz DDR (St.Helens)
 3.5MHz DDR (Mosel)



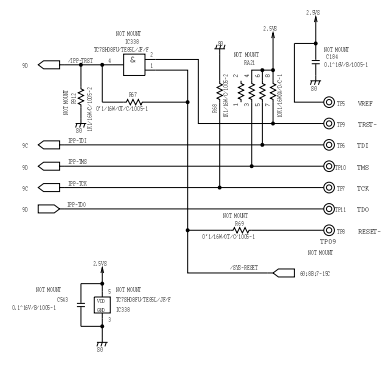
MANBA Clock



APM86190 (MANBA)



ARM(IPP) JTAG

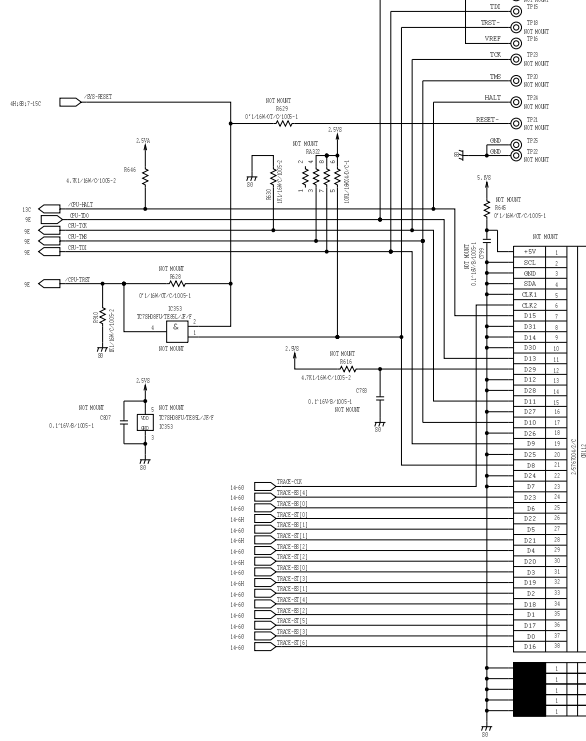


PWB
183 184 185 186

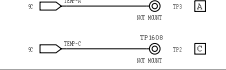
Heat Sink
183 184 185 186

LABEL
183 184 185 186

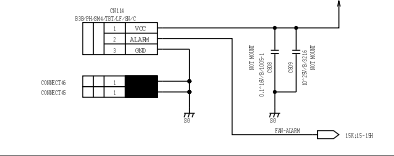
PPC JTAG



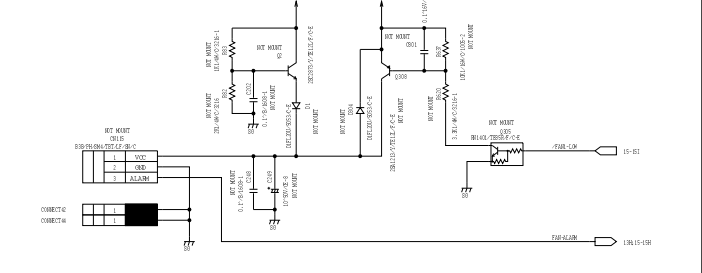
THERMAL SENSOR



CPU FAN 12V (debug)

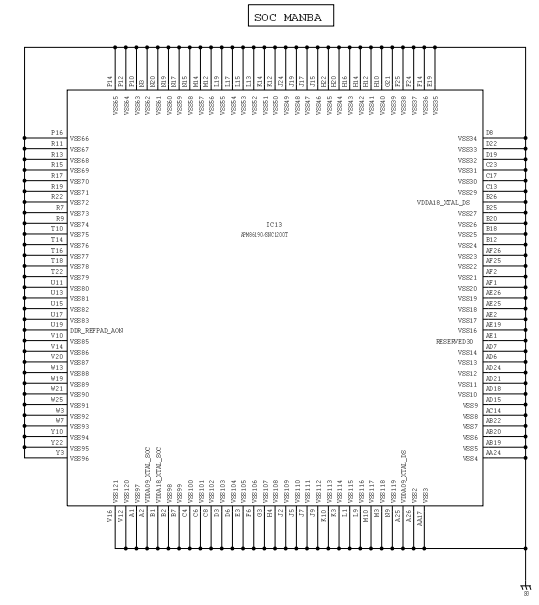
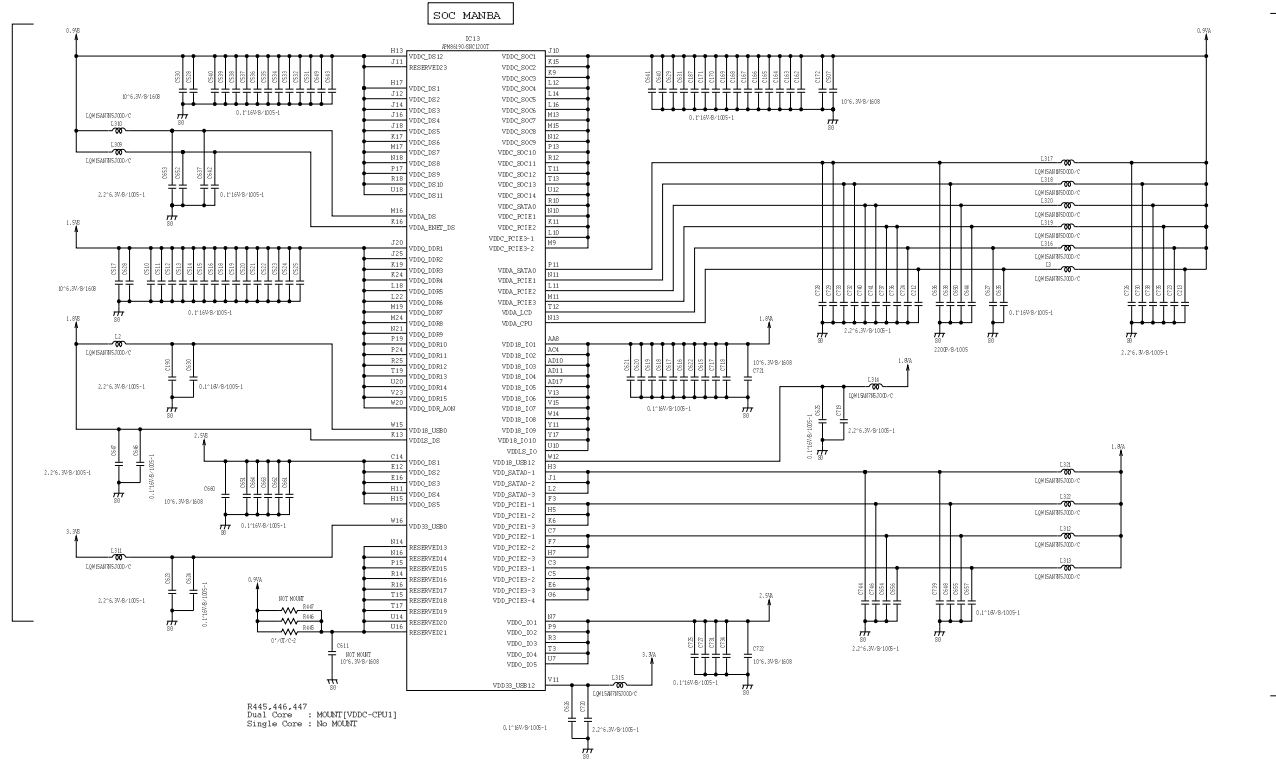


CPU FAN 24V



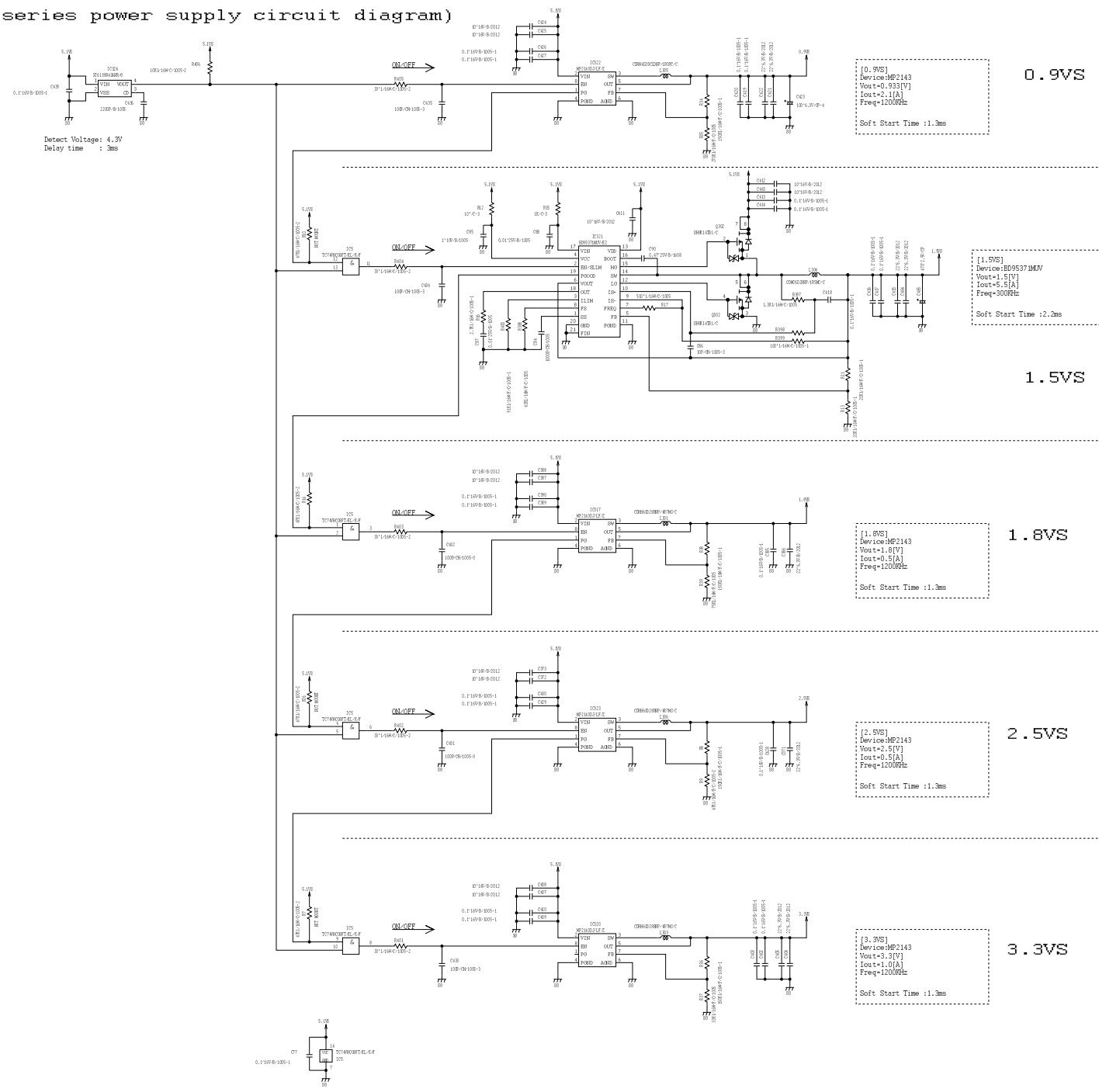
Deep Sleep
Power Domain

SoC
Power Domain



DEEP SLEEP POWER (S series power supply circuit diagram)

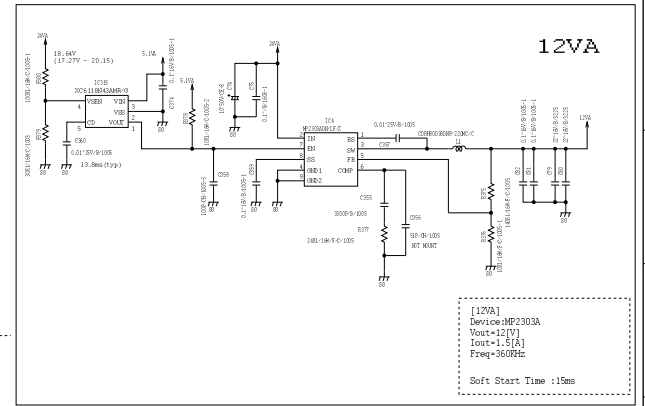
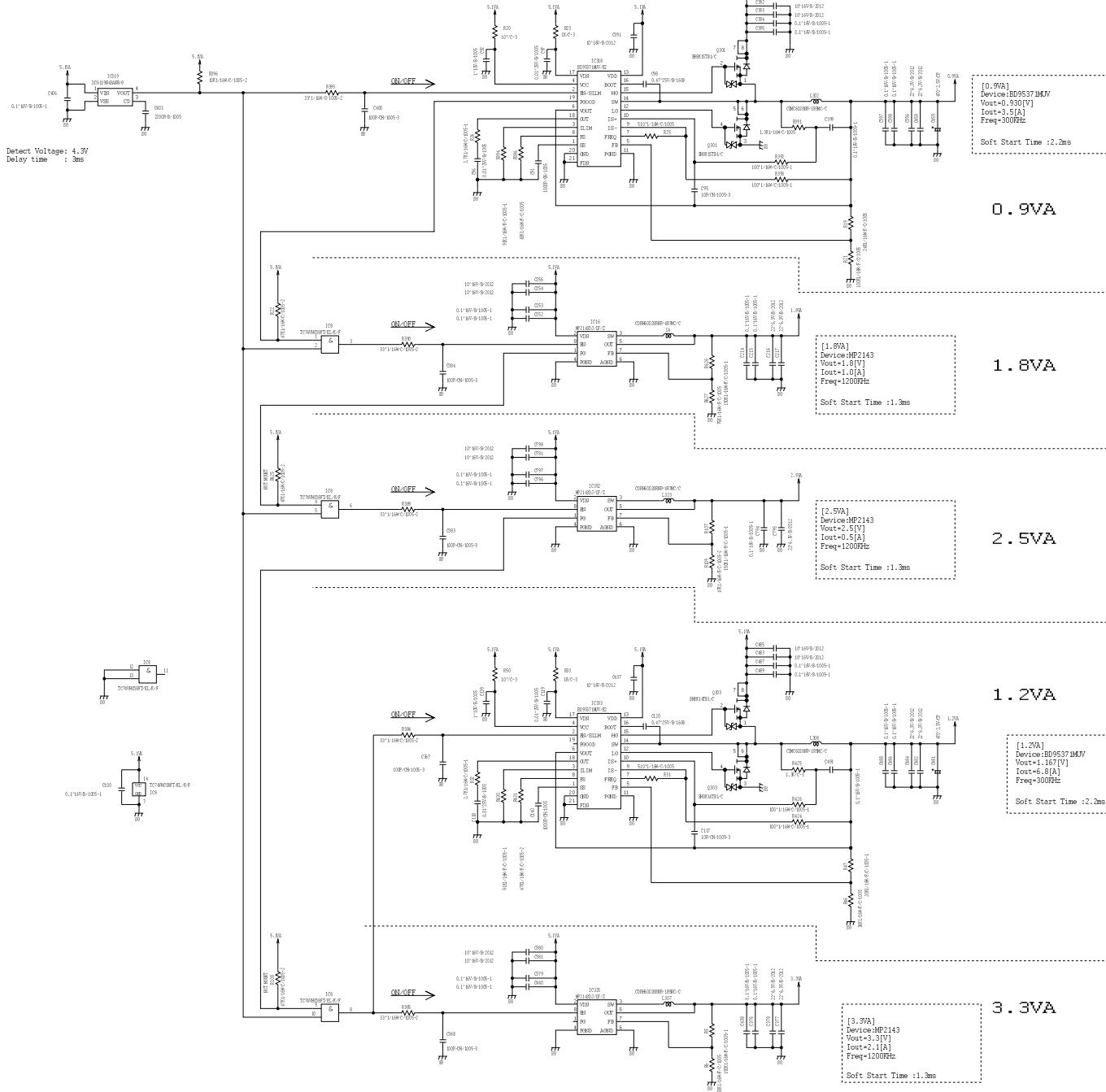
Power supply start-up sequence



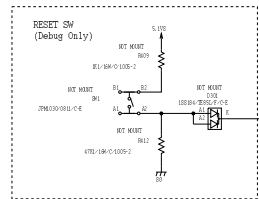
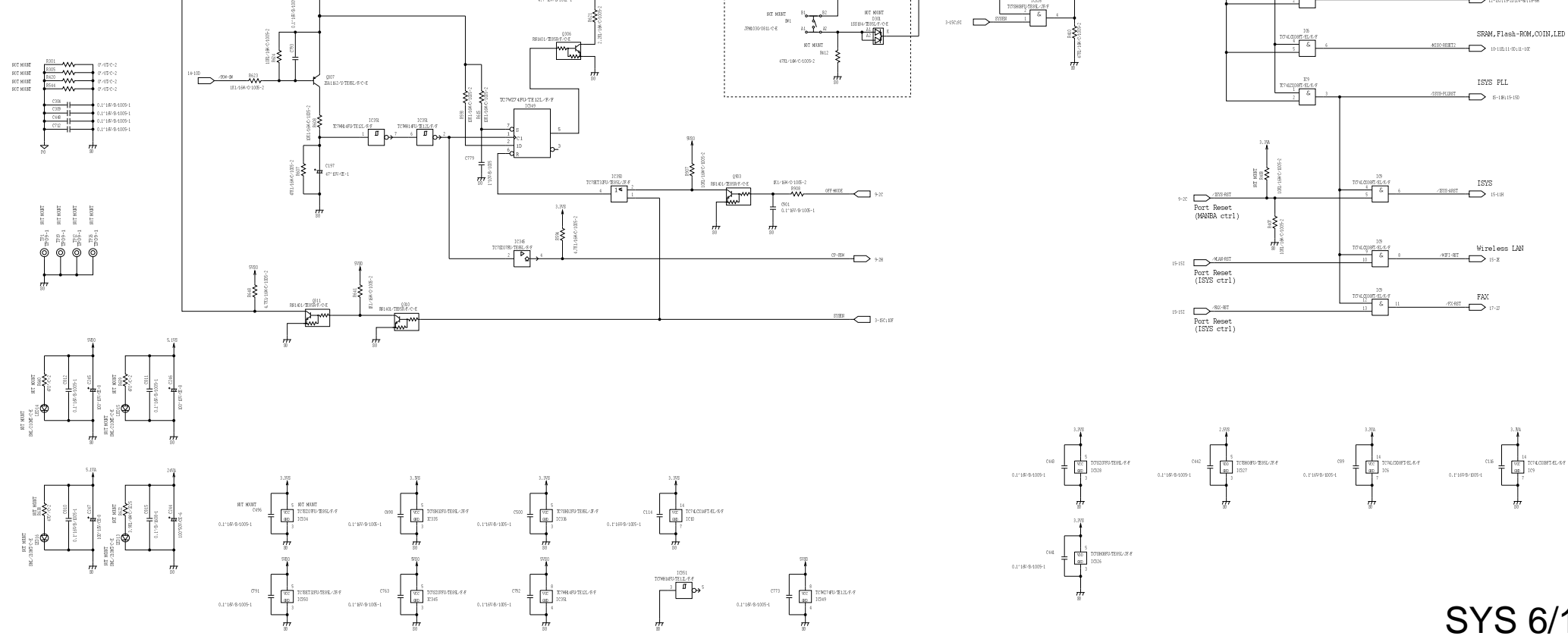
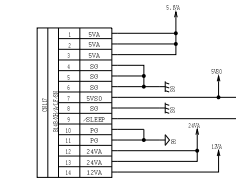
SOC POWER (A series power supply circuit diagram)

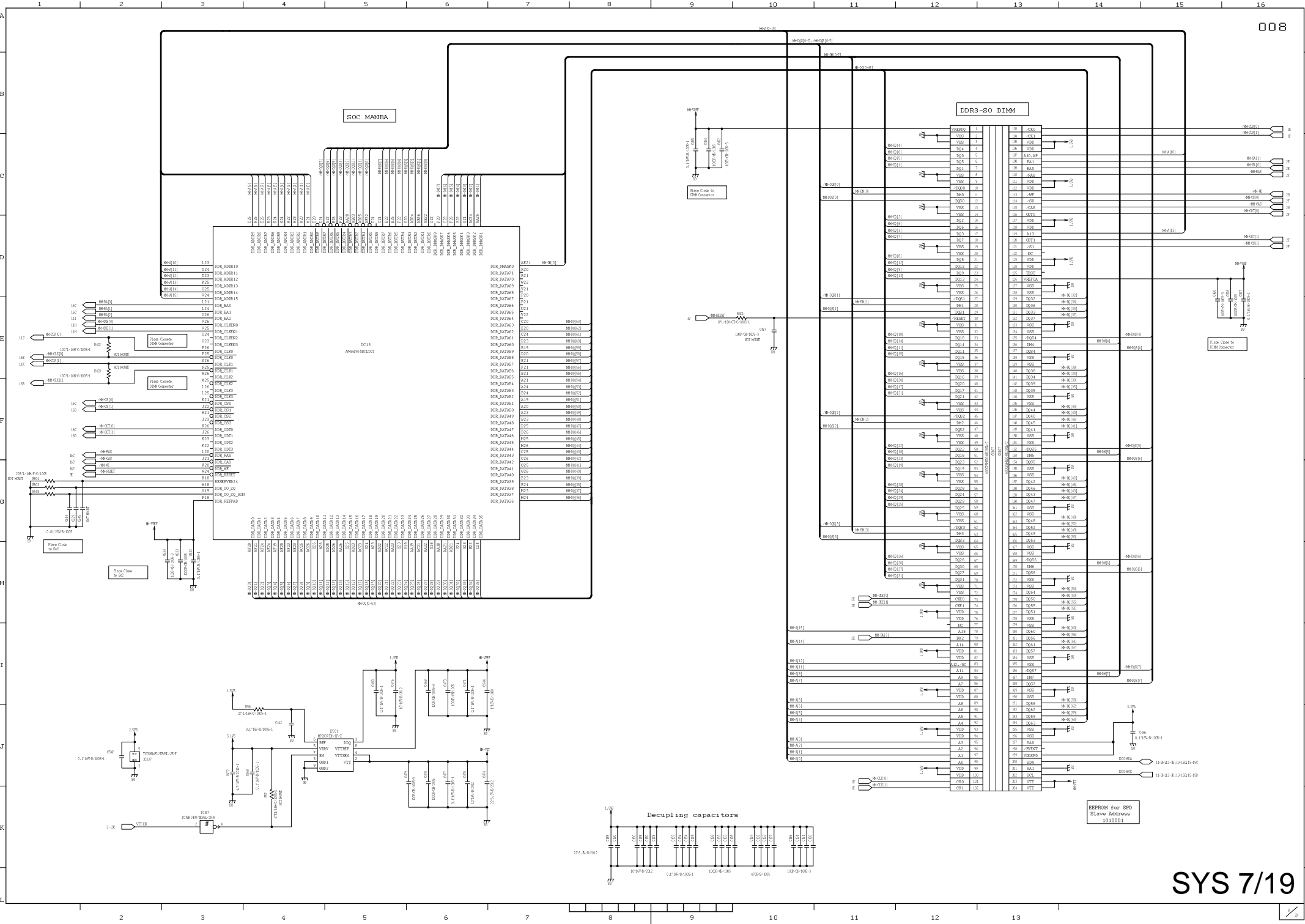
006

Power supply start-up sequence

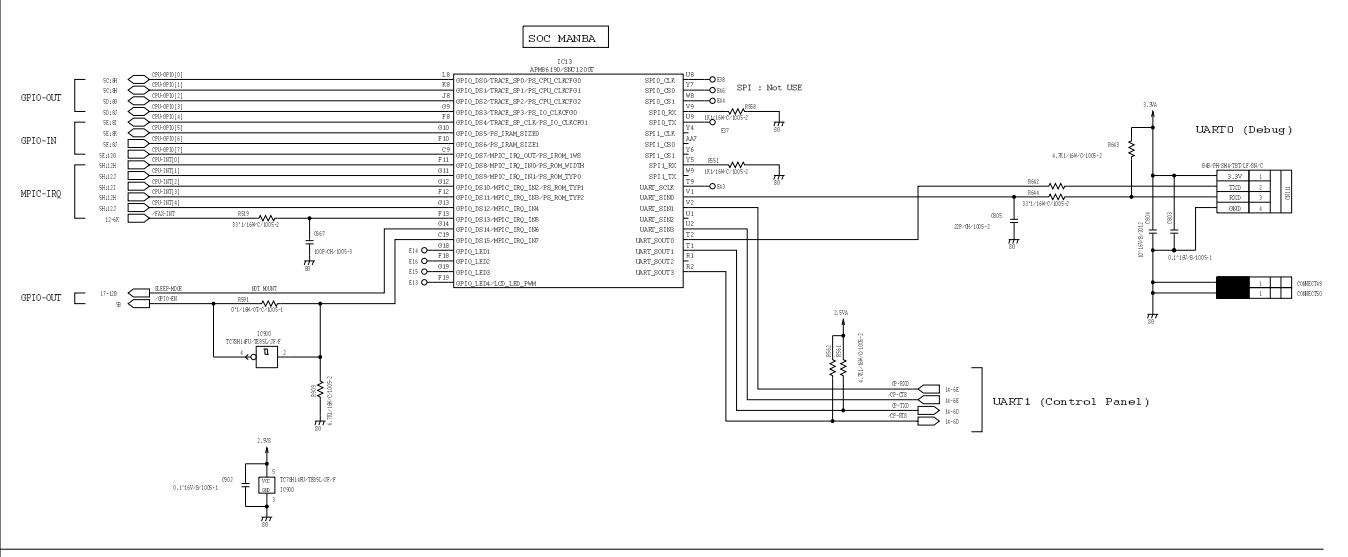
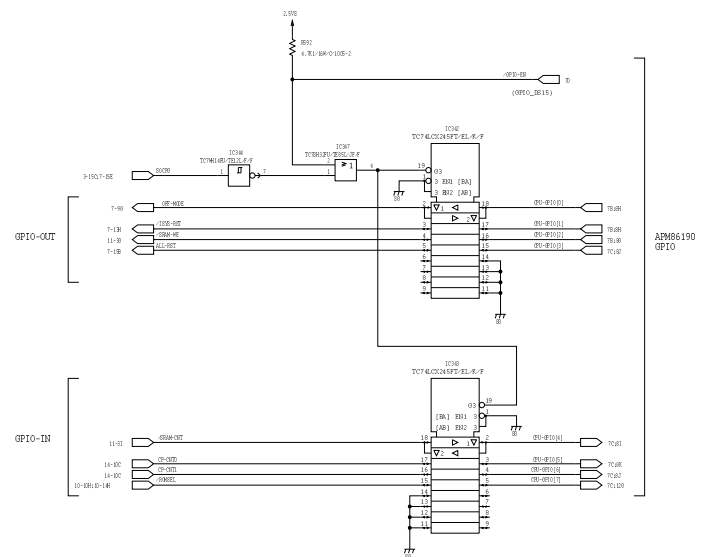


MAIN POWER
LVPS INPUT

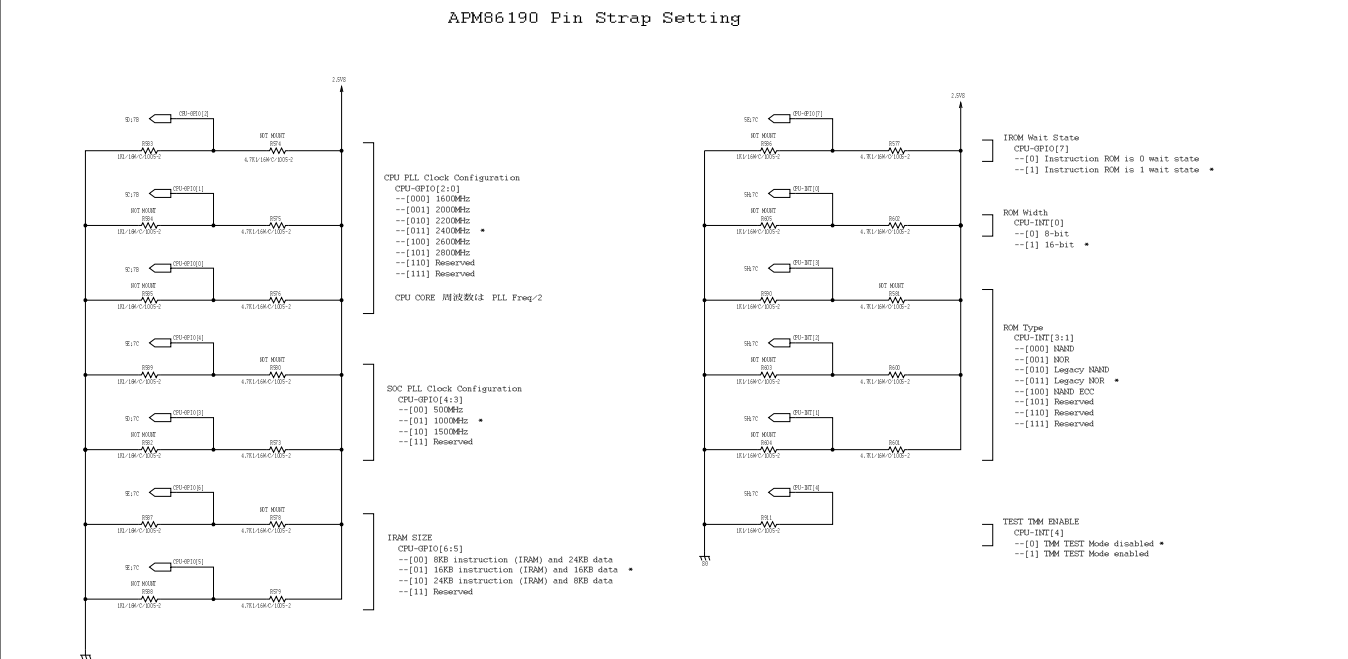
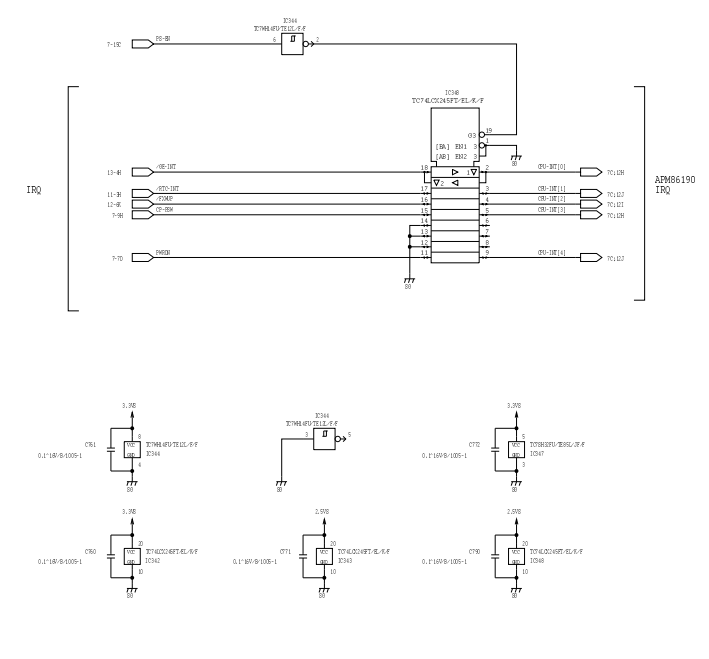




MANBA (GP IO / IRQ / SPI / UART)



APM86190 Pin Strap Setting

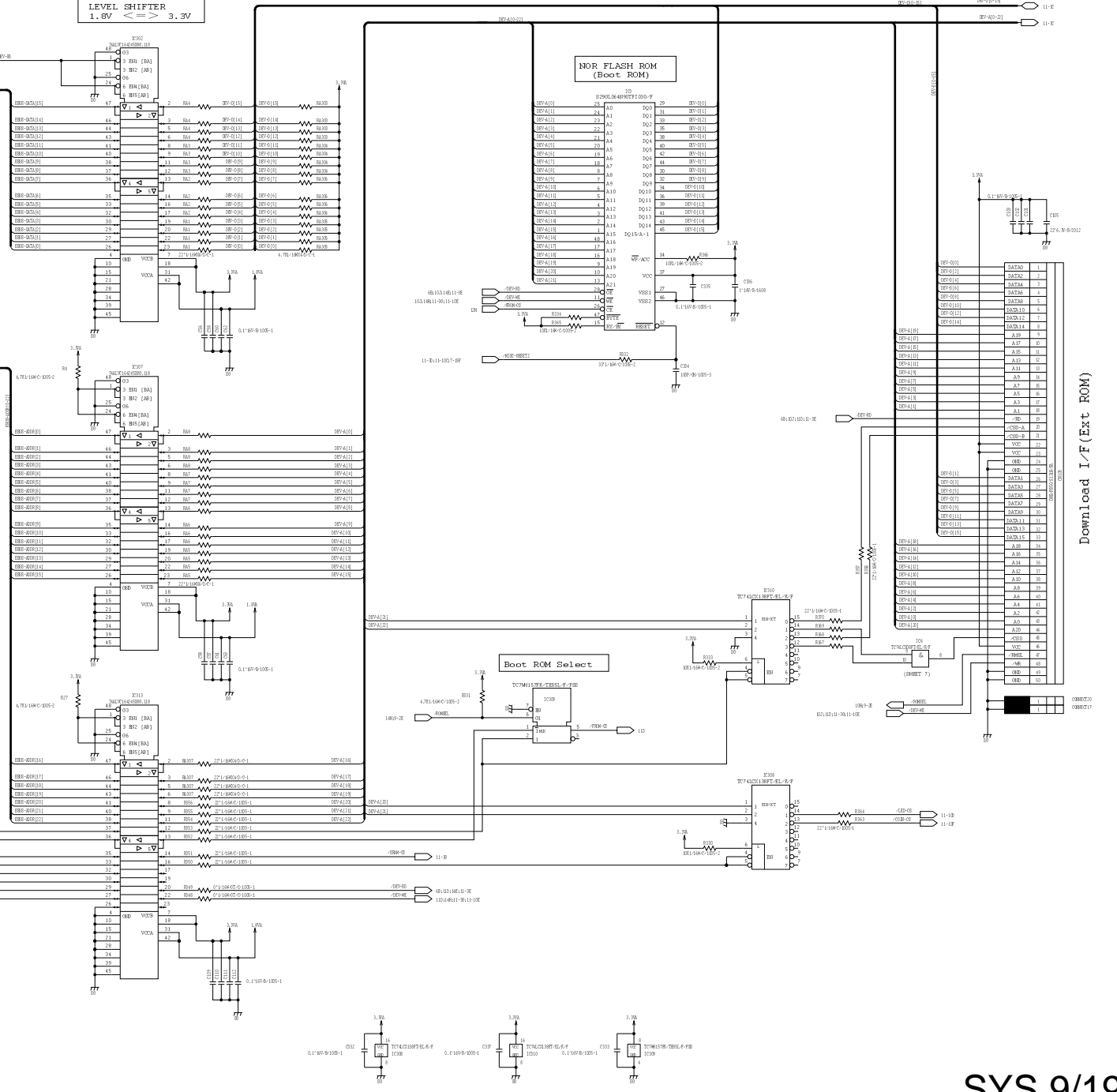


LEVEL SHIFTER
1.5V <=> 3.3V

NOR FLASH ROM
(Boot ROM)

SOC MANBA

SOC MANBA		AM1110 (SOC MANBA)	
EBUS-DATA[0]	AM0	EMMC_ADDR0	EMMC_DATA0-OP0_FL0
EBUS-DATA[1]	AM1	EMMC_ADDR1	EMMC_DATA1-OP0_FL1
EBUS-DATA[2]	AM2	EMMC_ADDR2	EMMC_DATA2-OP0_FL2
EBUS-DATA[3]	AM3	EMMC_ADDR3	EMMC_DATA3-OP0_FL3
EBUS-DATA[4]	AM4	EMMC_ADDR4	EMMC_DATA4-OP0_FL4
EBUS-DATA[5]	AM5	EMMC_ADDR5	EMMC_DATA5-OP0_FL5
EBUS-DATA[6]	AM6	EMMC_ADDR6	EMMC_DATA6-OP0_FL6
EBUS-DATA[7]	AM7	EMMC_ADDR7	EMMC_DATA7-OP0_FL7
EBUS-DATA[8]	AM8	EMMC_ADDR8	EMMC_DATA8-OP0_FL8
EBUS-DATA[9]	AM9	EMMC_ADDR9	EMMC_DATA9-OP0_FL9
EBUS-DATA[10]	AM10	EMMC_ADDR10	EMMC_DATA10-OP0_FL10
EBUS-DATA[11]	AM11	EMMC_ADDR11	EMMC_DATA11-OP0_FL11
EBUS-DATA[12]	AM12	EMMC_ADDR12	EMMC_DATA12-OP0_FL12
EBUS-DATA[13]	AM13	EMMC_ADDR13	EMMC_DATA13-OP0_FL13
EBUS-DATA[14]	AM14	EMMC_ADDR14	EMMC_DATA14-OP0_FL14
EBUS-DATA[15]	AM15	EMMC_ADDR15	EMMC_DATA15-OP0_FL15
EBUS-DATA[16]	AM16	EMMC_ADDR16	EMMC_DATA16-OP0_FL16
EBUS-DATA[17]	AM17	EMMC_ADDR17	EMMC_DATA17-OP0_FL17
EBUS-DATA[18]	AM18	EMMC_ADDR18	EMMC_DATA18-OP0_FL18
EBUS-DATA[19]	AM19	EMMC_ADDR19	EMMC_DATA19-OP0_FL19
EBUS-DATA[20]	AM20	EMMC_ADDR20	EMMC_DATA20-OP0_FL20
EBUS-DATA[21]	AM21	EMMC_ADDR21	EMMC_DATA21-OP0_FL21
EBUS-DATA[22]	AM22	EMMC_ADDR22	EMMC_DATA22-OP0_FL22
EBUS-DATA[23]	AM23	EMMC_ADDR23	EMMC_DATA23-OP0_FL23
EBUS-DATA[24]	AM24	EMMC_ADDR24	EMMC_DATA24-OP0_FL24
EBUS-DATA[25]	AM25	EMMC_ADDR25	EMMC_DATA25-OP0_FL25
EBUS-DATA[26]	AM26	EMMC_ADDR26	EMMC_DATA26-OP0_FL26
EBUS-DATA[27]	AM27	EMMC_ADDR27	EMMC_DATA27-OP0_FL27
EBUS-DATA[28]	AM28	EMMC_ADDR28	EMMC_DATA28-OP0_FL28
EBUS-DATA[29]	AM29	EMMC_ADDR29	EMMC_DATA29-OP0_FL29
EBUS-DATA[30]	AM30	EMMC_ADDR30	EMMC_DATA30-OP0_FL30
EBUS-DATA[31]	AM31	EMMC_ADDR31	EMMC_DATA31-OP0_FL31
EBUS-DATA[32]	AM32	EMMC_ADDR32	EMMC_DATA32-OP0_FL32
EBUS-DATA[33]	AM33	EMMC_ADDR33	EMMC_DATA33-OP0_FL33
EBUS-DATA[34]	AM34	EMMC_ADDR34	EMMC_DATA34-OP0_FL34
EBUS-DATA[35]	AM35	EMMC_ADDR35	EMMC_DATA35-OP0_FL35
EBUS-DATA[36]	AM36	EMMC_ADDR36	EMMC_DATA36-OP0_FL36
EBUS-DATA[37]	AM37	EMMC_ADDR37	EMMC_DATA37-OP0_FL37
EBUS-DATA[38]	AM38	EMMC_ADDR38	EMMC_DATA38-OP0_FL38
EBUS-DATA[39]	AM39	EMMC_ADDR39	EMMC_DATA39-OP0_FL39
EBUS-DATA[40]	AM40	EMMC_ADDR40	EMMC_DATA40-OP0_FL40
EBUS-DATA[41]	AM41	EMMC_ADDR41	EMMC_DATA41-OP0_FL41
EBUS-DATA[42]	AM42	EMMC_ADDR42	EMMC_DATA42-OP0_FL42
EBUS-DATA[43]	AM43	EMMC_ADDR43	EMMC_DATA43-OP0_FL43
EBUS-DATA[44]	AM44	EMMC_ADDR44	EMMC_DATA44-OP0_FL44
EBUS-DATA[45]	AM45	EMMC_ADDR45	EMMC_DATA45-OP0_FL45
EBUS-DATA[46]	AM46	EMMC_ADDR46	EMMC_DATA46-OP0_FL46
EBUS-DATA[47]	AM47	EMMC_ADDR47	EMMC_DATA47-OP0_FL47
EBUS-DATA[48]	AM48	EMMC_ADDR48	EMMC_DATA48-OP0_FL48
EBUS-DATA[49]	AM49	EMMC_ADDR49	EMMC_DATA49-OP0_FL49
EBUS-DATA[50]	AM50	EMMC_ADDR50	EMMC_DATA50-OP0_FL50
EBUS-DATA[51]	AM51	EMMC_ADDR51	EMMC_DATA51-OP0_FL51
EBUS-DATA[52]	AM52	EMMC_ADDR52	EMMC_DATA52-OP0_FL52
EBUS-DATA[53]	AM53	EMMC_ADDR53	EMMC_DATA53-OP0_FL53
EBUS-DATA[54]	AM54	EMMC_ADDR54	EMMC_DATA54-OP0_FL54
EBUS-DATA[55]	AM55	EMMC_ADDR55	EMMC_DATA55-OP0_FL55
EBUS-DATA[56]	AM56	EMMC_ADDR56	EMMC_DATA56-OP0_FL56
EBUS-DATA[57]	AM57	EMMC_ADDR57	EMMC_DATA57-OP0_FL57
EBUS-DATA[58]	AM58	EMMC_ADDR58	EMMC_DATA58-OP0_FL58
EBUS-DATA[59]	AM59	EMMC_ADDR59	EMMC_DATA59-OP0_FL59
EBUS-DATA[60]	AM60	EMMC_ADDR60	EMMC_DATA60-OP0_FL60
EBUS-DATA[61]	AM61	EMMC_ADDR61	EMMC_DATA61-OP0_FL61
EBUS-DATA[62]	AM62	EMMC_ADDR62	EMMC_DATA62-OP0_FL62
EBUS-DATA[63]	AM63	EMMC_ADDR63	EMMC_DATA63-OP0_FL63
EBUS-DATA[64]	AM64	EMMC_ADDR64	EMMC_DATA64-OP0_FL64
EBUS-DATA[65]	AM65	EMMC_ADDR65	EMMC_DATA65-OP0_FL65
EBUS-DATA[66]	AM66	EMMC_ADDR66	EMMC_DATA66-OP0_FL66
EBUS-DATA[67]	AM67	EMMC_ADDR67	EMMC_DATA67-OP0_FL67
EBUS-DATA[68]	AM68	EMMC_ADDR68	EMMC_DATA68-OP0_FL68
EBUS-DATA[69]	AM69	EMMC_ADDR69	EMMC_DATA69-OP0_FL69
EBUS-DATA[70]	AM70	EMMC_ADDR70	EMMC_DATA70-OP0_FL70
EBUS-DATA[71]	AM71	EMMC_ADDR71	EMMC_DATA71-OP0_FL71
EBUS-DATA[72]	AM72	EMMC_ADDR72	EMMC_DATA72-OP0_FL72
EBUS-DATA[73]	AM73	EMMC_ADDR73	EMMC_DATA73-OP0_FL73
EBUS-DATA[74]	AM74	EMMC_ADDR74	EMMC_DATA74-OP0_FL74
EBUS-DATA[75]	AM75	EMMC_ADDR75	EMMC_DATA75-OP0_FL75
EBUS-DATA[76]	AM76	EMMC_ADDR76	EMMC_DATA76-OP0_FL76
EBUS-DATA[77]	AM77	EMMC_ADDR77	EMMC_DATA77-OP0_FL77
EBUS-DATA[78]	AM78	EMMC_ADDR78	EMMC_DATA78-OP0_FL78
EBUS-DATA[79]	AM79	EMMC_ADDR79	EMMC_DATA79-OP0_FL79
EBUS-DATA[80]	AM80	EMMC_ADDR80	EMMC_DATA80-OP0_FL80
EBUS-DATA[81]	AM81	EMMC_ADDR81	EMMC_DATA81-OP0_FL81
EBUS-DATA[82]	AM82	EMMC_ADDR82	EMMC_DATA82-OP0_FL82
EBUS-DATA[83]	AM83	EMMC_ADDR83	EMMC_DATA83-OP0_FL83
EBUS-DATA[84]	AM84	EMMC_ADDR84	EMMC_DATA84-OP0_FL84
EBUS-DATA[85]	AM85	EMMC_ADDR85	EMMC_DATA85-OP0_FL85
EBUS-DATA[86]	AM86	EMMC_ADDR86	EMMC_DATA86-OP0_FL86
EBUS-DATA[87]	AM87	EMMC_ADDR87	EMMC_DATA87-OP0_FL87
EBUS-DATA[88]	AM88	EMMC_ADDR88	EMMC_DATA88-OP0_FL88
EBUS-DATA[89]	AM89	EMMC_ADDR89	EMMC_DATA89-OP0_FL89
EBUS-DATA[90]	AM90	EMMC_ADDR90	EMMC_DATA90-OP0_FL90
EBUS-DATA[91]	AM91	EMMC_ADDR91	EMMC_DATA91-OP0_FL91
EBUS-DATA[92]	AM92	EMMC_ADDR92	EMMC_DATA92-OP0_FL92
EBUS-DATA[93]	AM93	EMMC_ADDR93	EMMC_DATA93-OP0_FL93
EBUS-DATA[94]	AM94	EMMC_ADDR94	EMMC_DATA94-OP0_FL94
EBUS-DATA[95]	AM95	EMMC_ADDR95	EMMC_DATA95-OP0_FL95
EBUS-DATA[96]	AM96	EMMC_ADDR96	EMMC_DATA96-OP0_FL96
EBUS-DATA[97]	AM97	EMMC_ADDR97	EMMC_DATA97-OP0_FL97
EBUS-DATA[98]	AM98	EMMC_ADDR98	EMMC_DATA98-OP0_FL98
EBUS-DATA[99]	AM99	EMMC_ADDR99	EMMC_DATA99-OP0_FL99

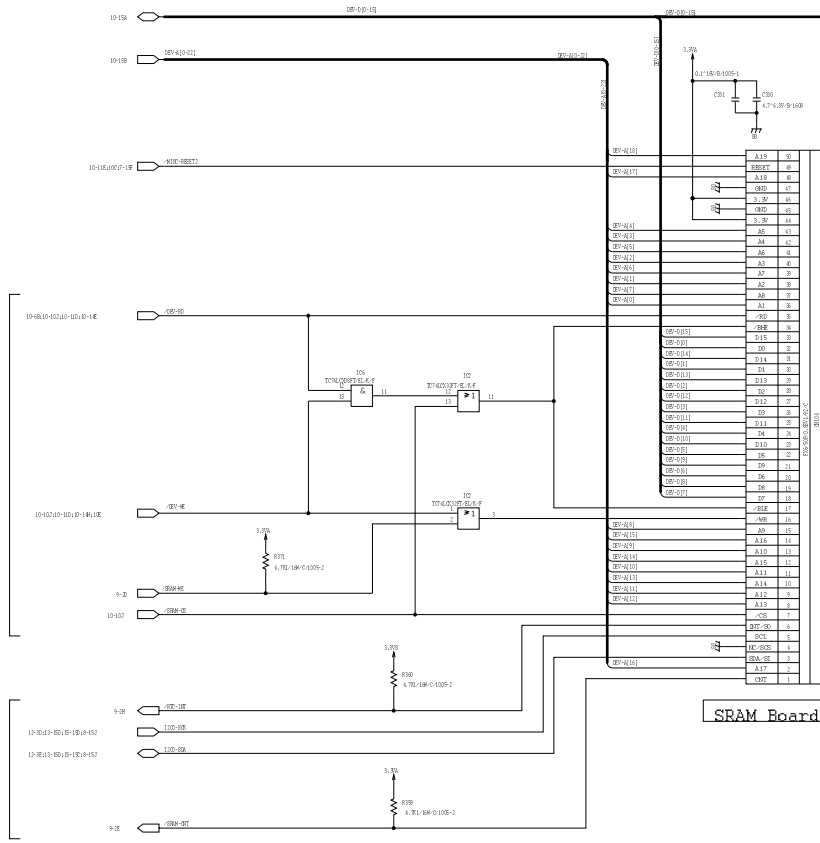


Download I/F (Ext ROM)

EBUS -- 2/2

SRAM I/F (EBUS)

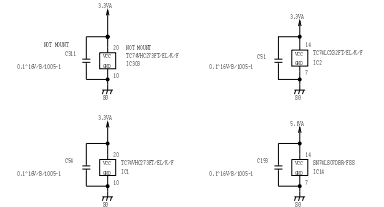
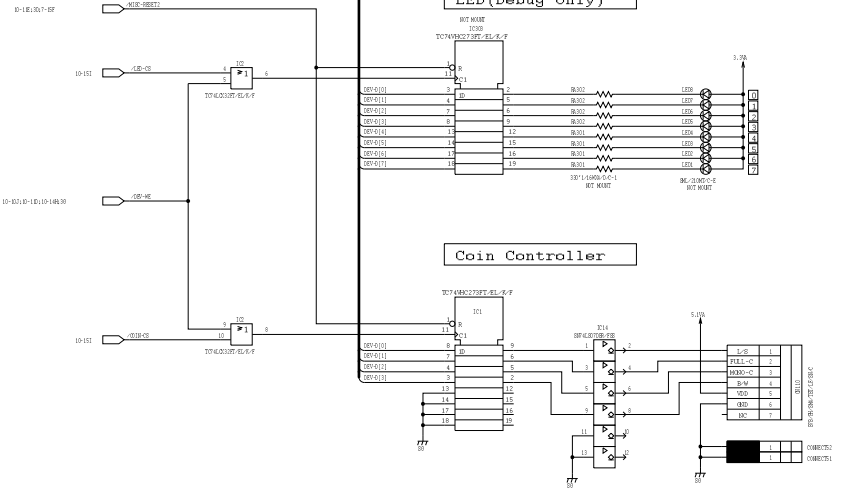
RTC I/F (I2C, GPIO, IRQ)



SRAM Board I/F

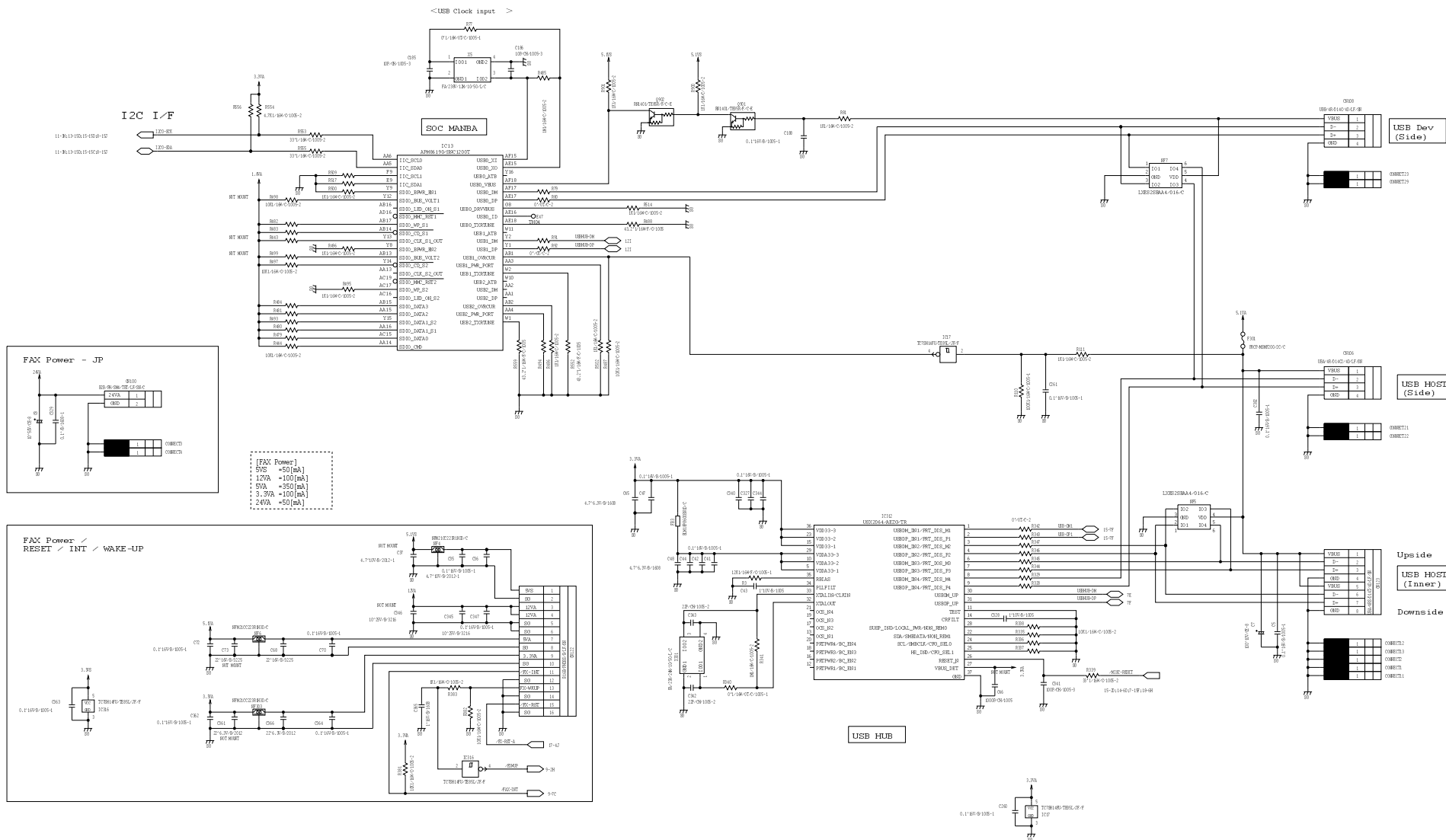
LED (Debug Only)

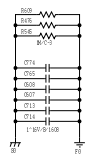
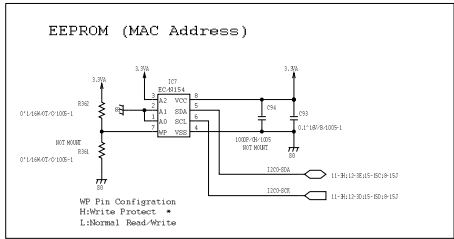
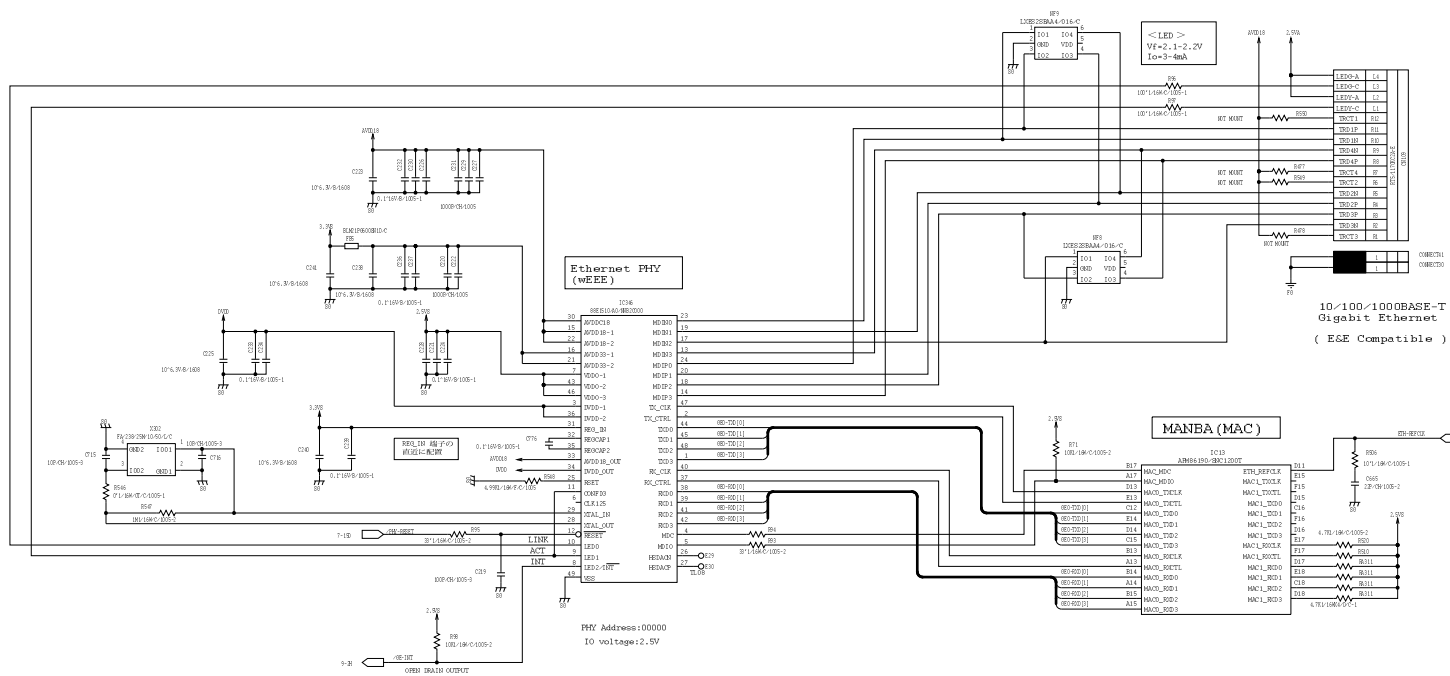
Coin Controller

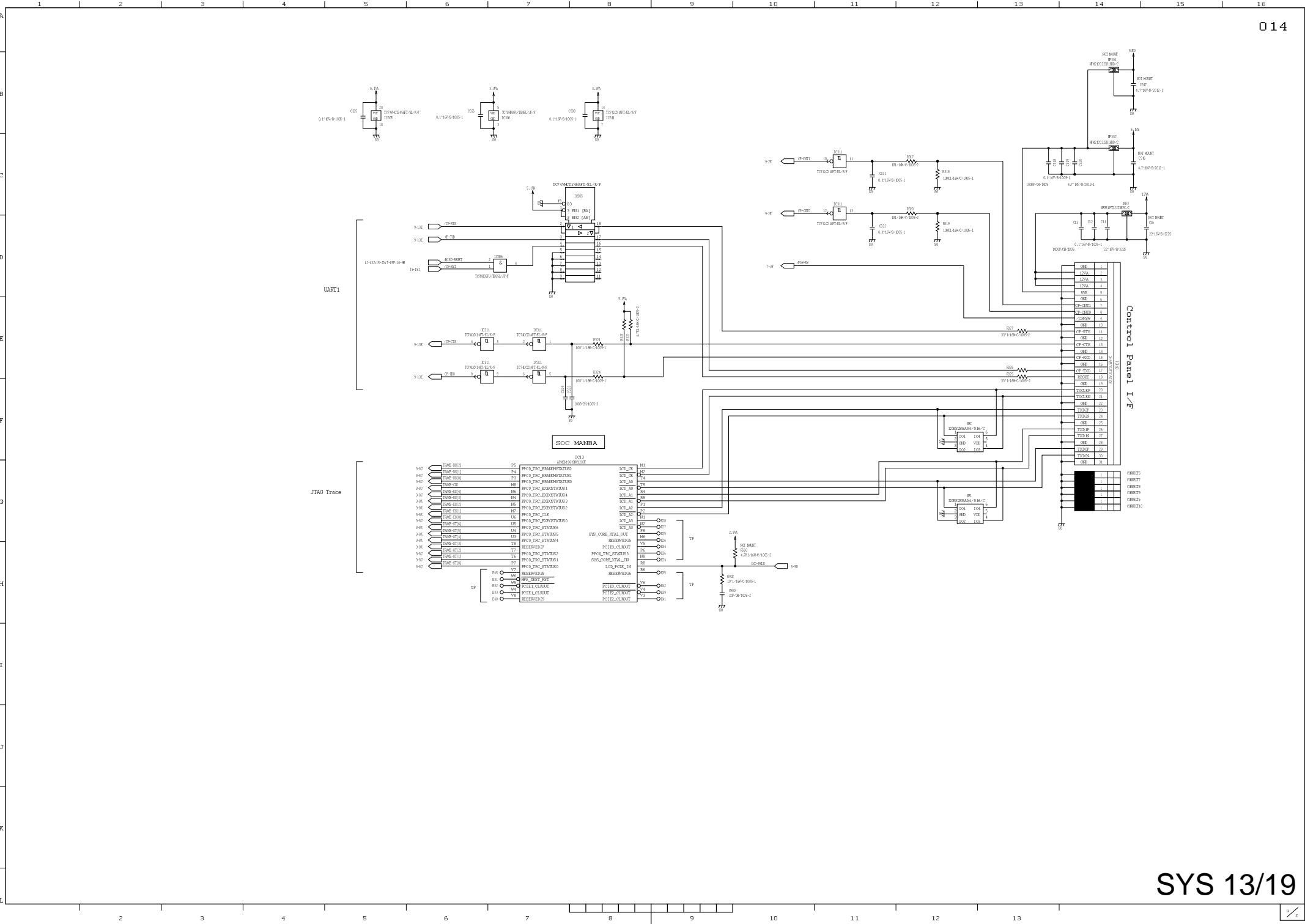


I2C Slave Address

Controller	Address SA[6:0]	Device Name
I2C0	1010001	EEPROM for MMIO DIMM SPD
	1010100	EEPROM for Ethernet Port0 MAC ADDRESS
	0110010	KTC
	0010011	(Reserved)
	0011100	ASIC ISYS
I2C1	-----	Not Use





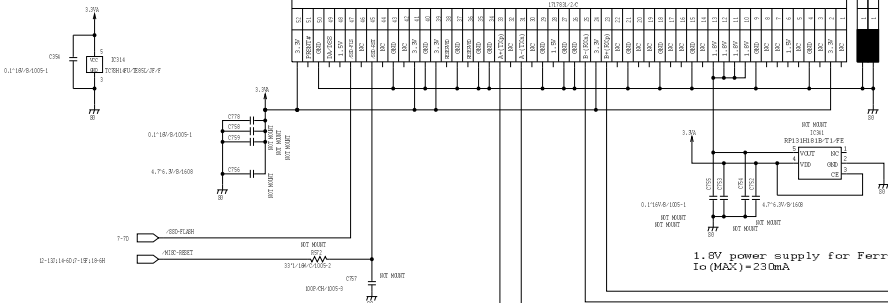


SerDes[PCIE / SATA] / ISYS-GPIO/IRQ

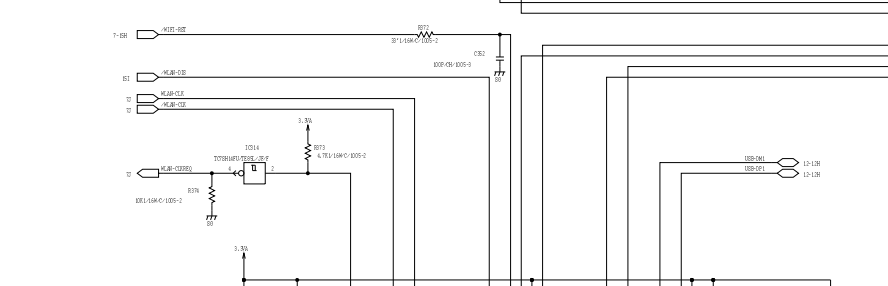
Clip

SATA Mini Card SSD Slot (Ferri SSD)

PCI Express Mini Card Size

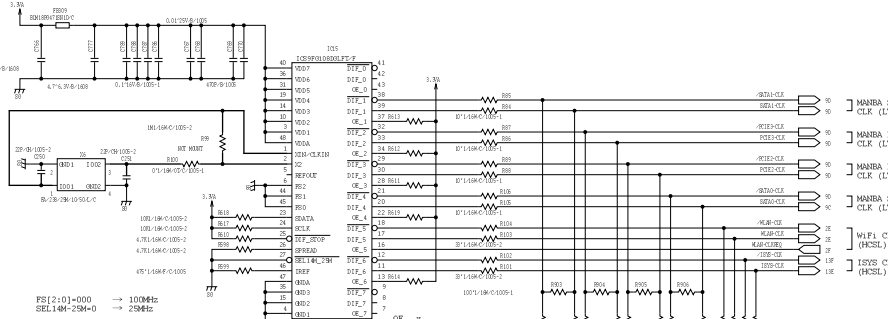


1.8V power supply for Ferri SSD
Io(MAX)=230mA

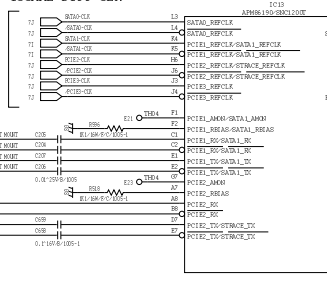


PCI Express Mini Card Slot For Wireless LAN Card

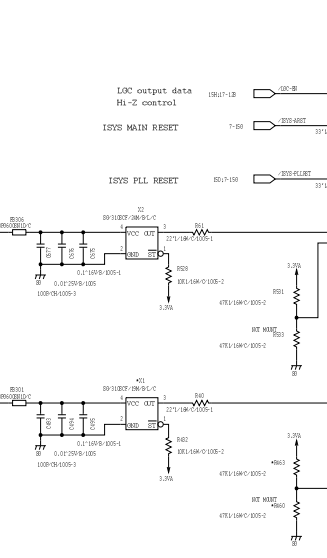
SerDes Clock (Diff-100MHz)



SerDes Reference CLK 100MHz Diff CLK

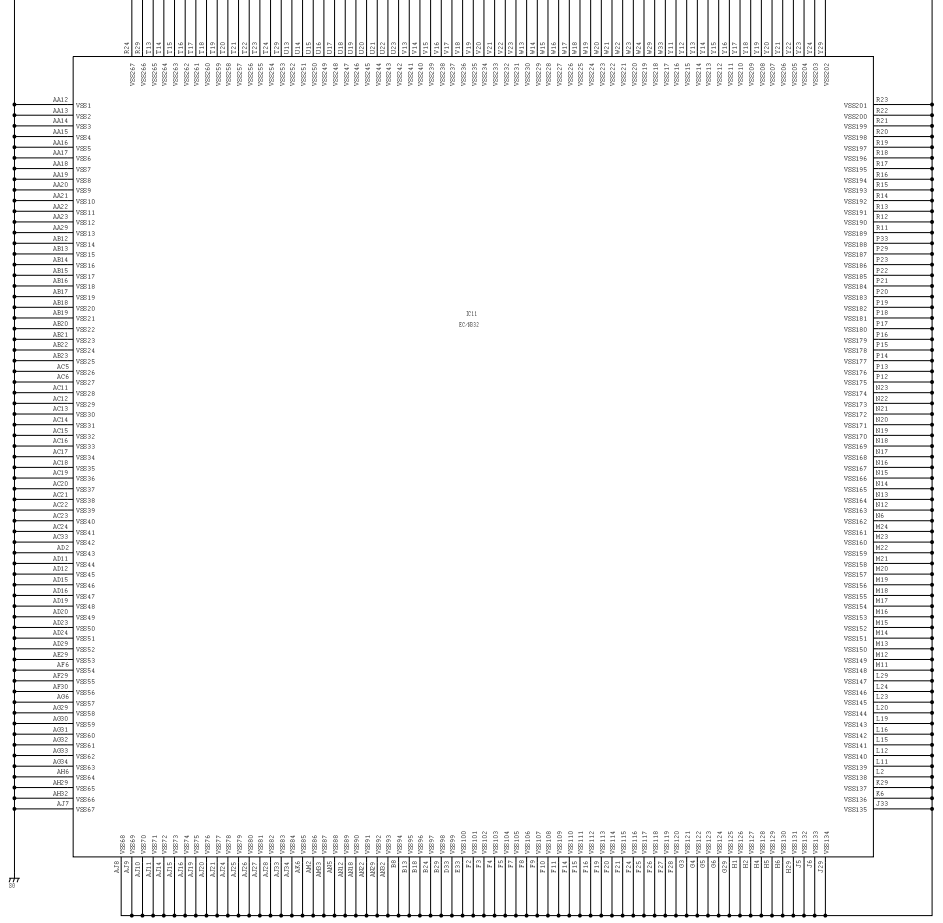
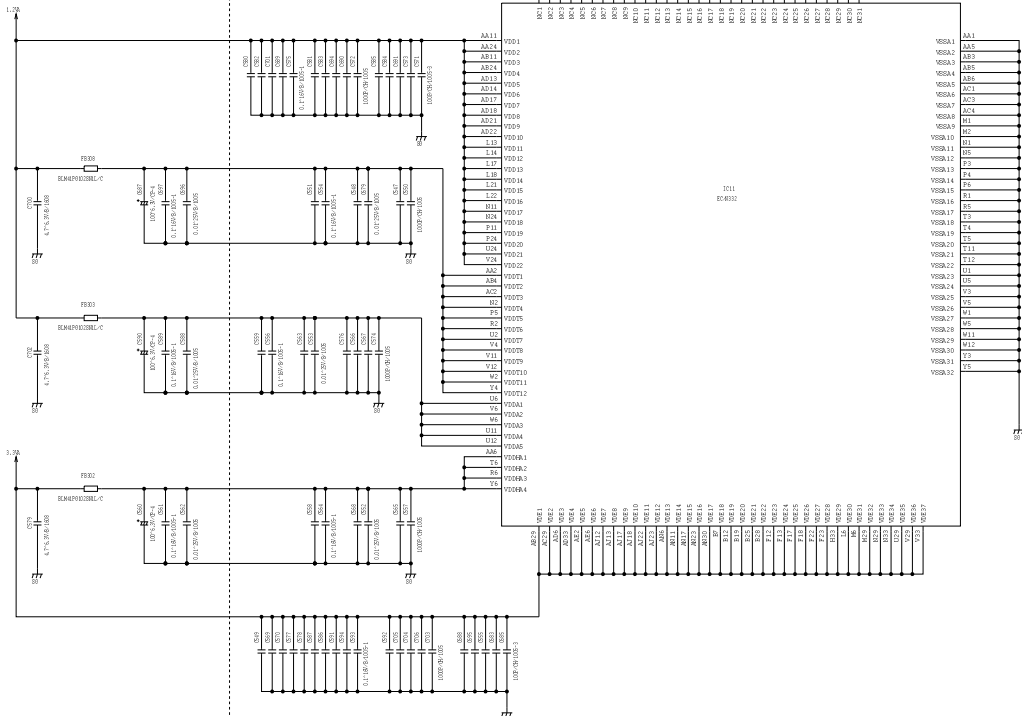


ISYS Clock input GPIO / INT



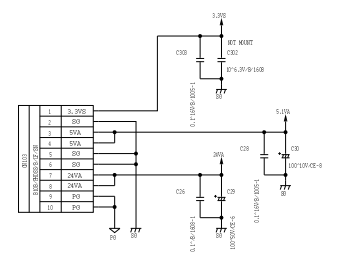
ASIC ISYS

ASIC ISYS



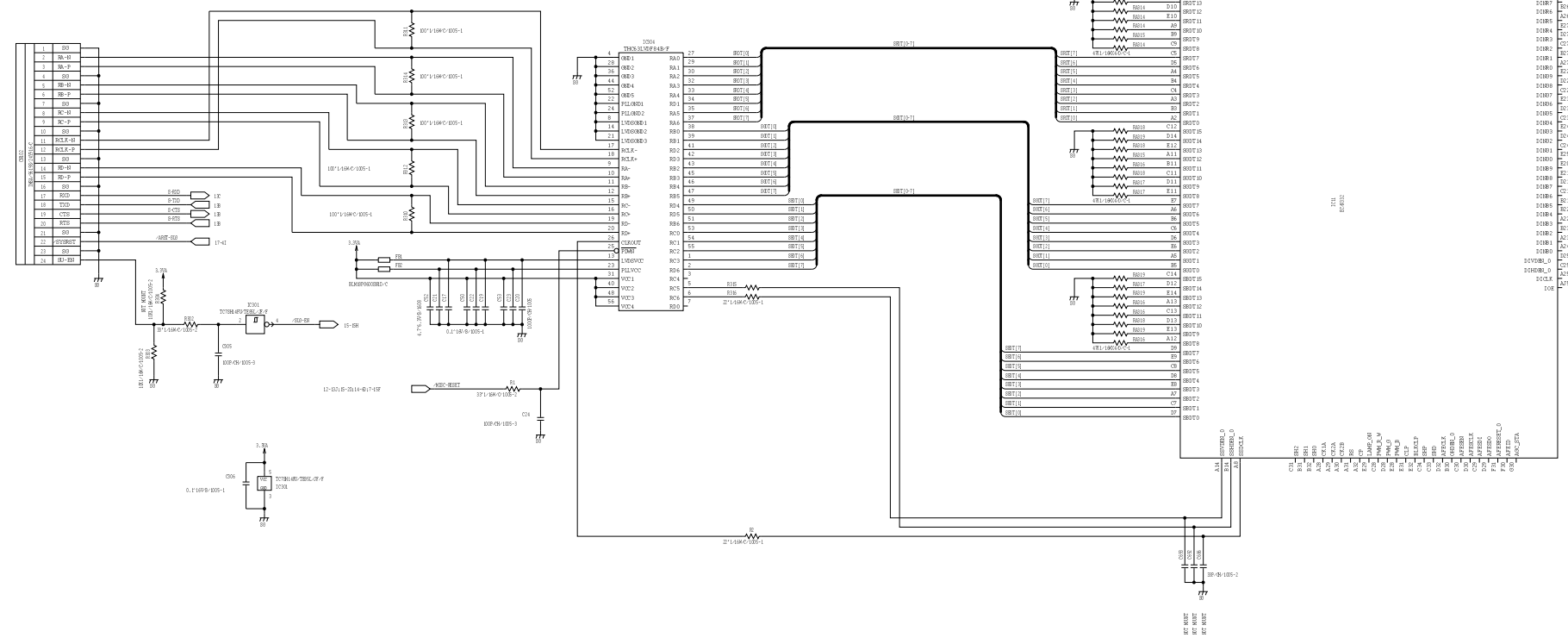
<ISYS Power Supply>
 VDDA 1.2V Analog
 VDDT 1.2V Analog SerDes TX
 VDD 1.2V Digital
 VDDHA 3.3V Analog
 VDE 3.3V Digital
 1.2V cons. current 4671[mA]
 3.3V cons. current 195[mA]

SU Power

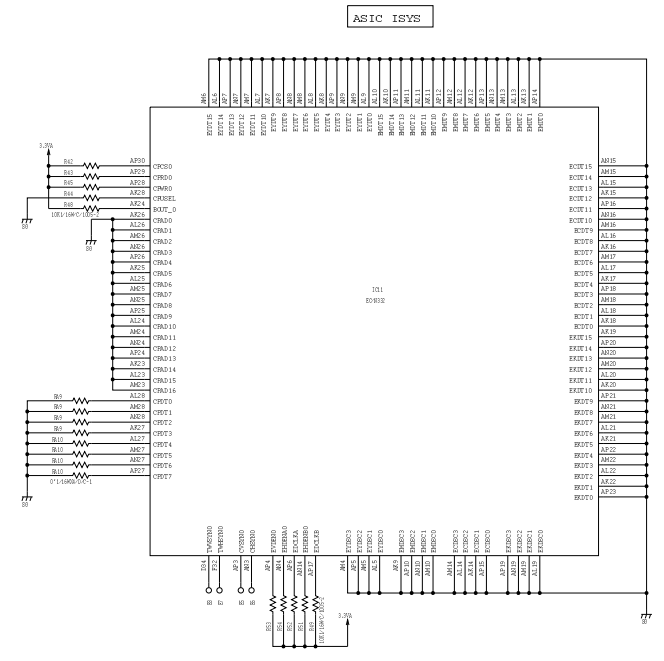


SU Power
 3.200 ± 1.0[A] (Peak 1.7[A])
 5VA ± 0.9[A] (Peak 2.7[A])
 24VA ± 1.0[A] (Peak 1.7[A])

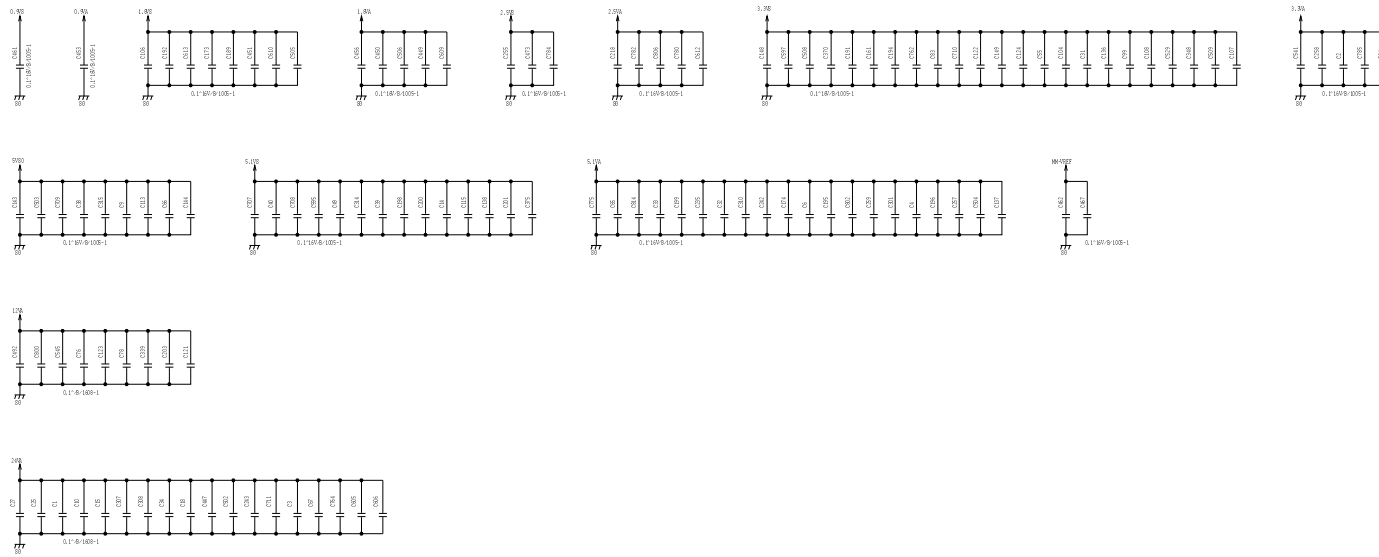
SU I/F



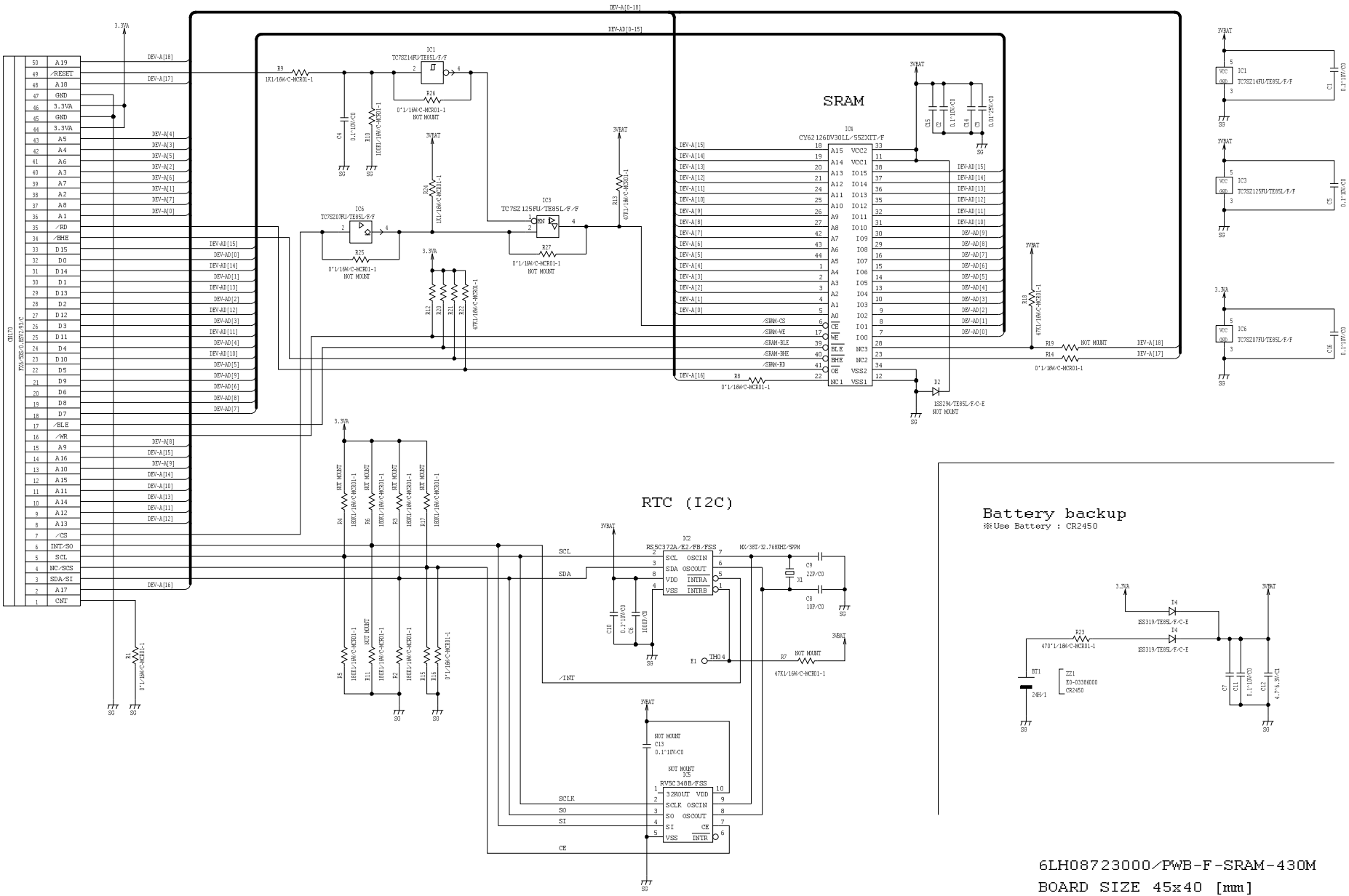
ISYS - EFI /Image processing debug



Capacitors (For Reducing The Power Plane Resonance)

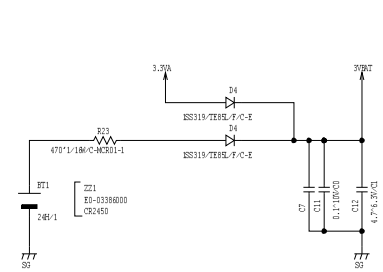


BASE-PCB-I/F



Battery backup

※Use Battery : CR2450



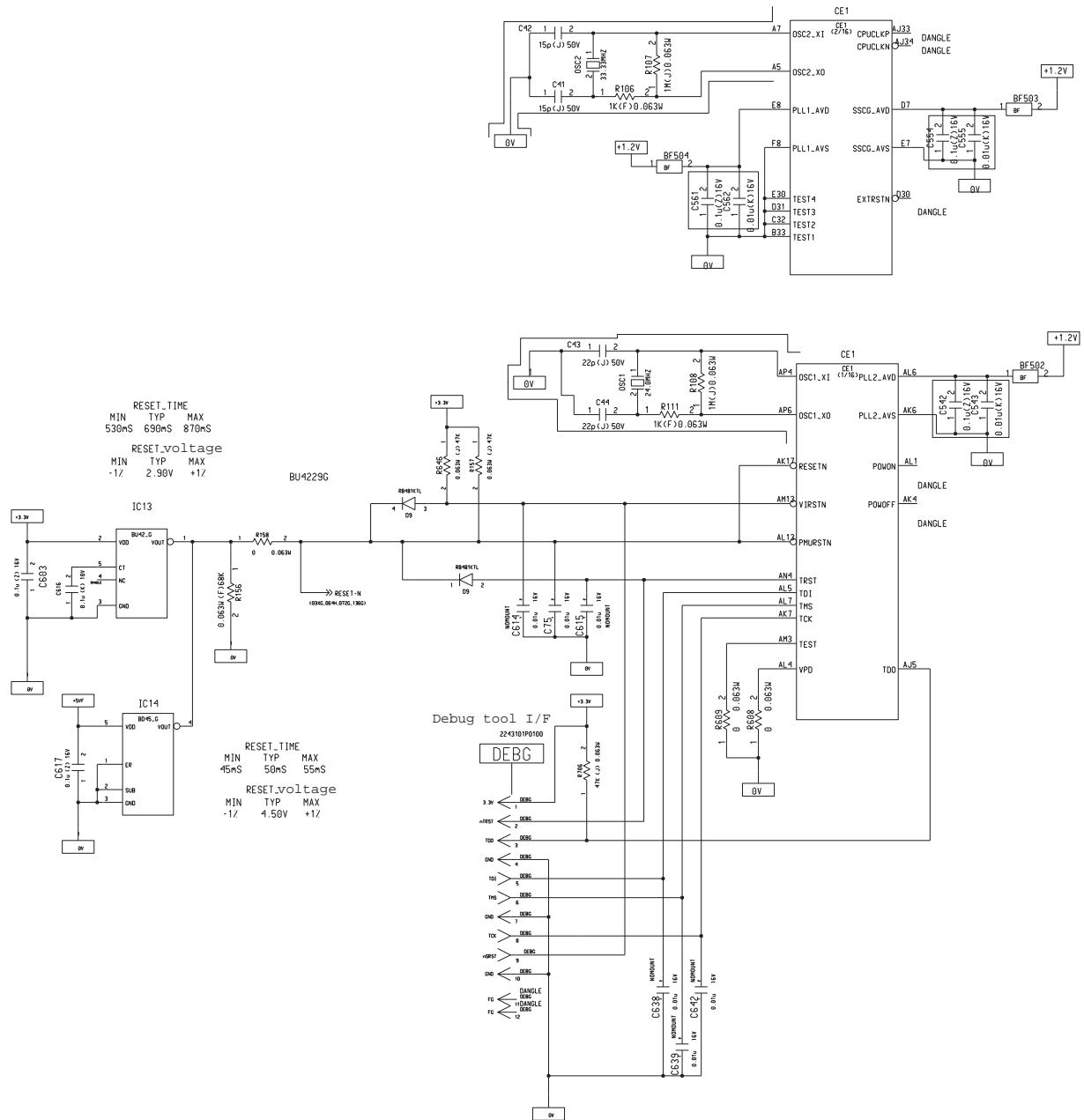
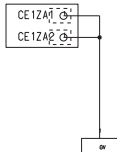
6LH08723000/PWB-F-SRAM-430M
BOARD SIZE 45x40 [mm]

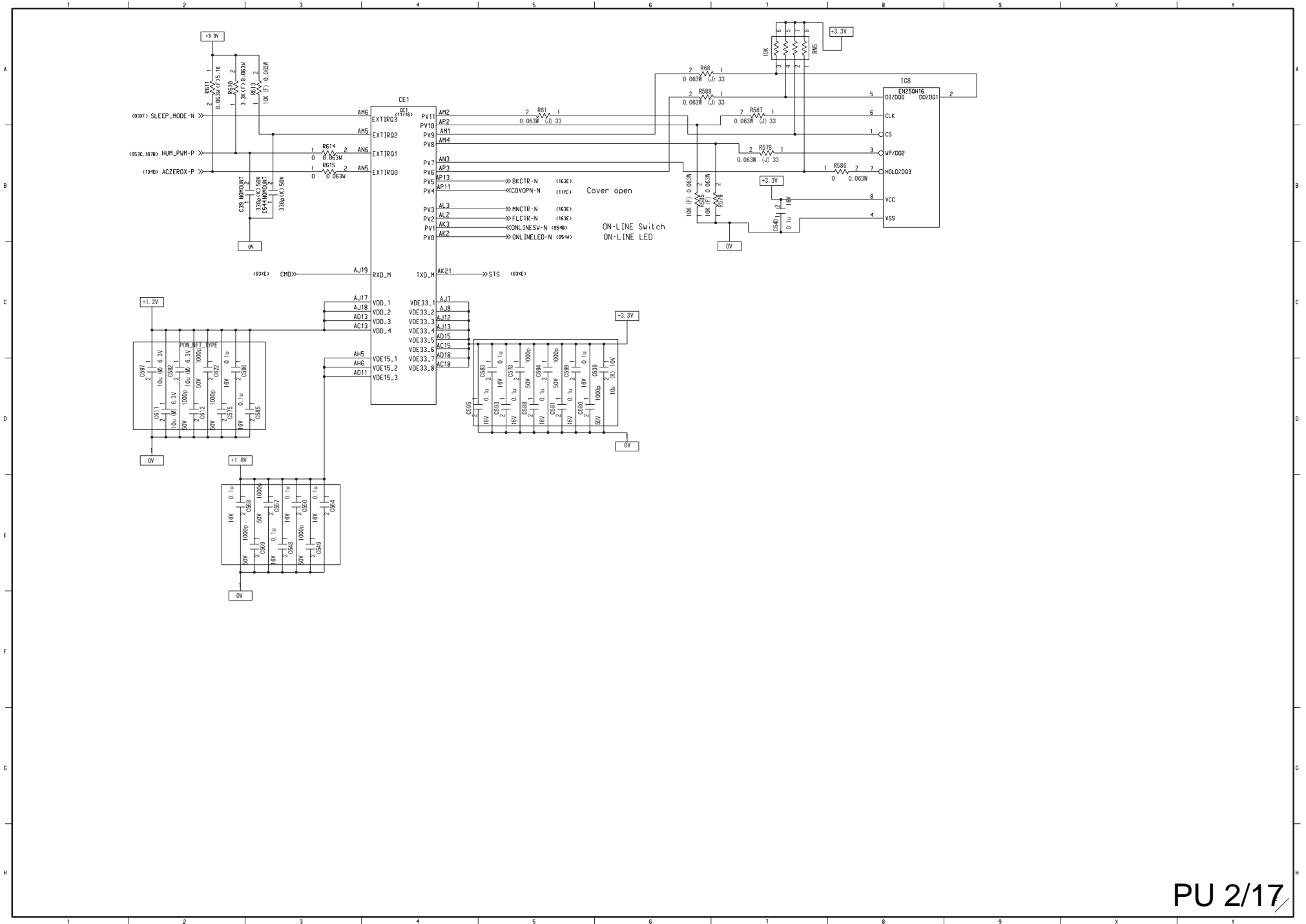
SRAM 1/1

Schematics of Board PU

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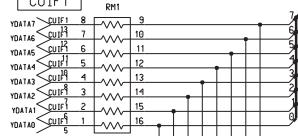
Page	Contents	Note
1	Reset , FC	
2	SPI Flash	
3	CU I/F	
4	RAM	
5	Control Panel, RFID, Env.	
6	HEAD Y, K	
7	HEAD C, M , HEAD Fuse	
8	Motor 1/2 Clutch	
9	Motor 2/2	
10	Sensor	
11	High-voltage control, FAN, DUP, 2nd	
12	Toner sensor, relay board	
13	Power supply connector, 1.2V DCDC, Fusing control	
14	1.8V DCDC, 3.3V DCDC	
15	CE1 Power pin	
16	FX757 extension, FN298 connector	
17	Boot setting	
18		



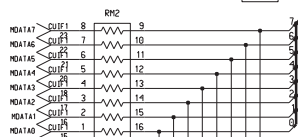


R97494011-FCT

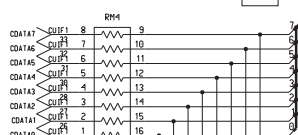
CUIF1



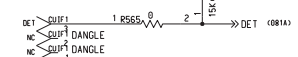
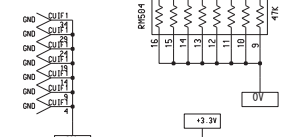
YDATA(7:0) (0344,034C,0374)



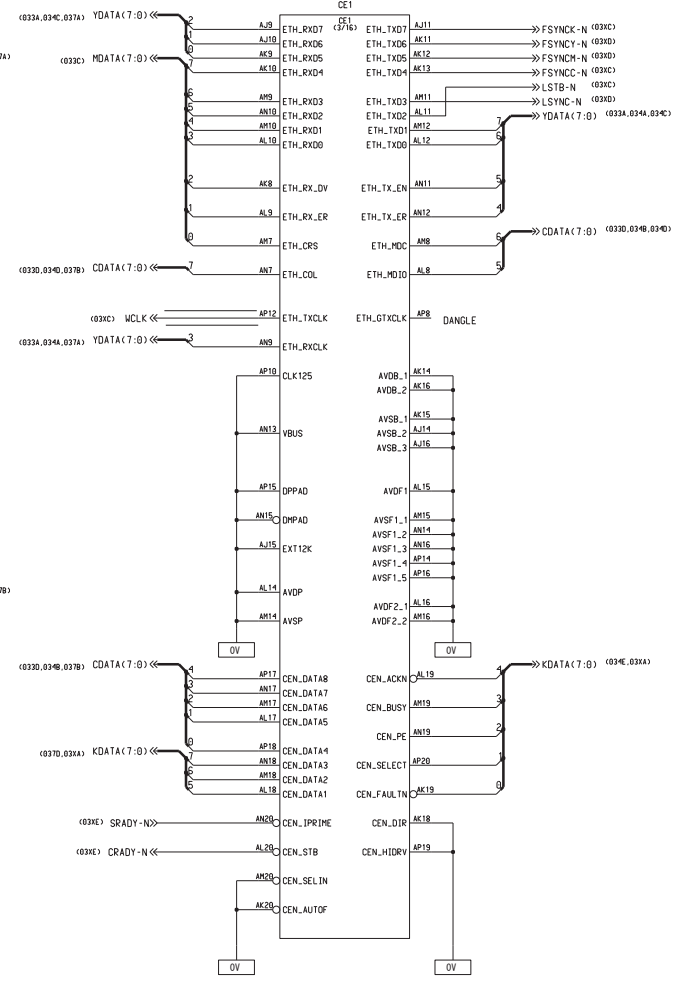
MDATA(7:0) (0344)



CDATA(7:0) (034B,034D,037B)

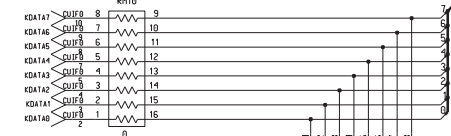


DET (081A)

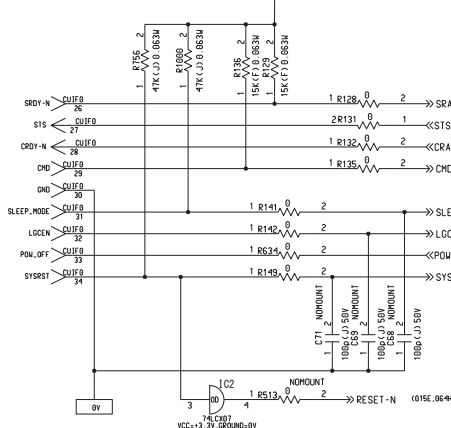
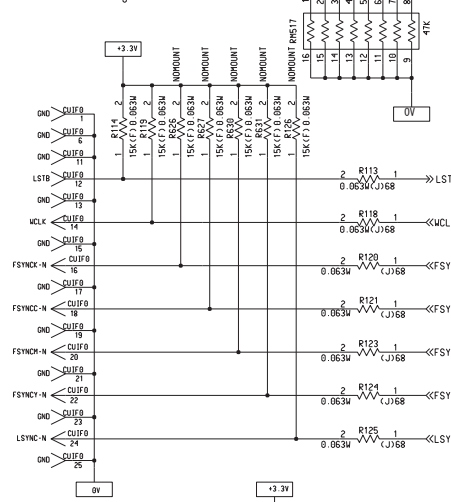


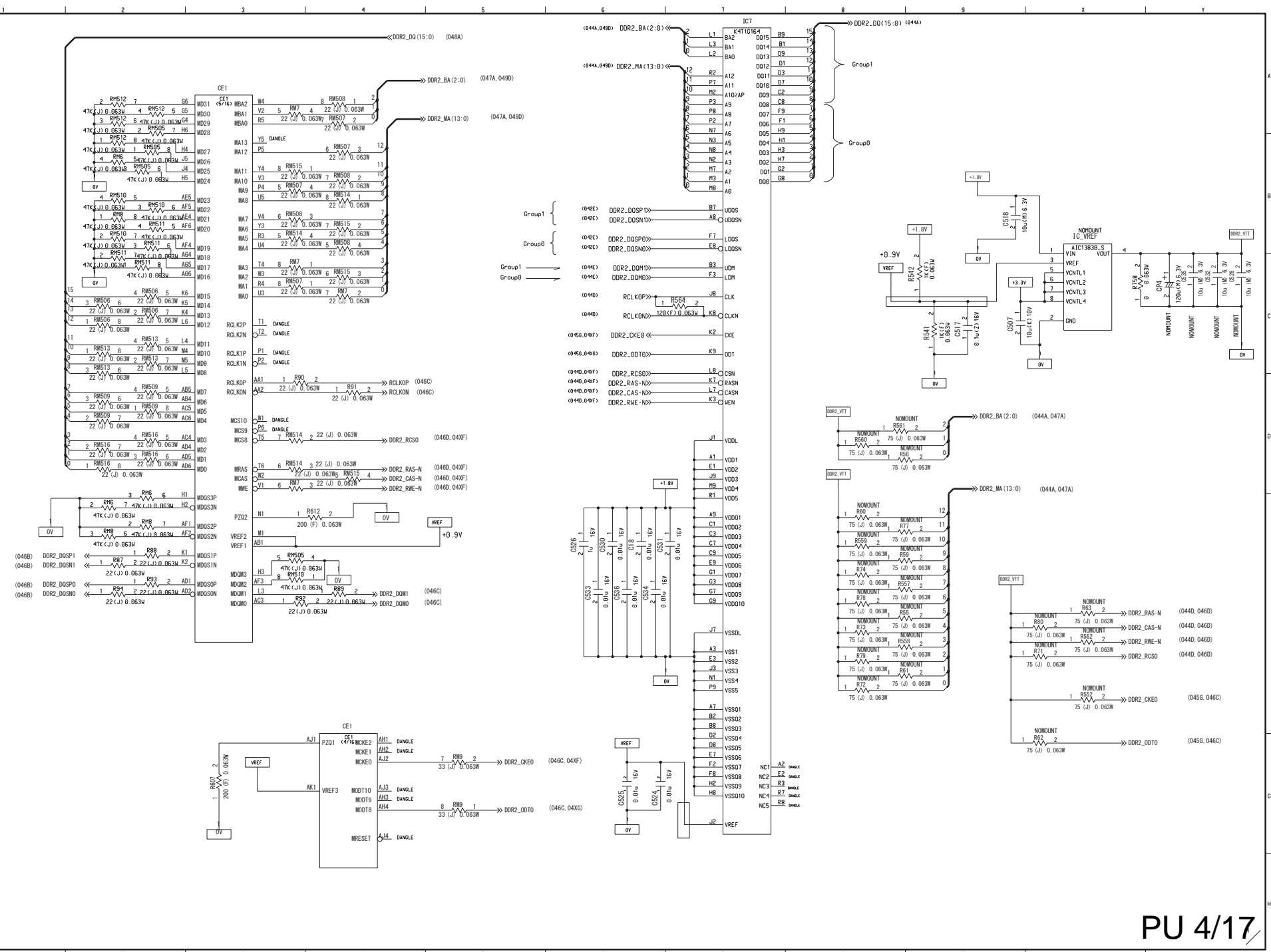
R97494011-FCT

CUIF0

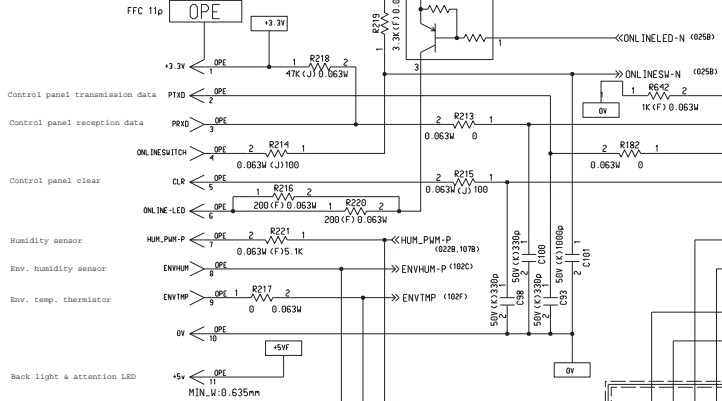


KDATA(7:0) (034E,037D)

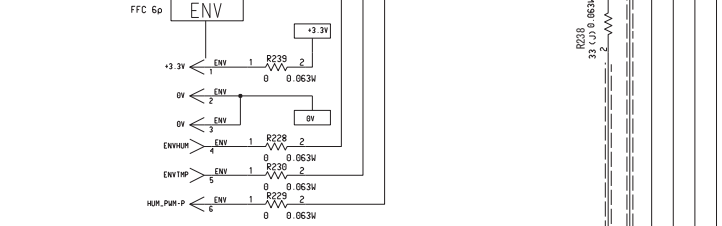




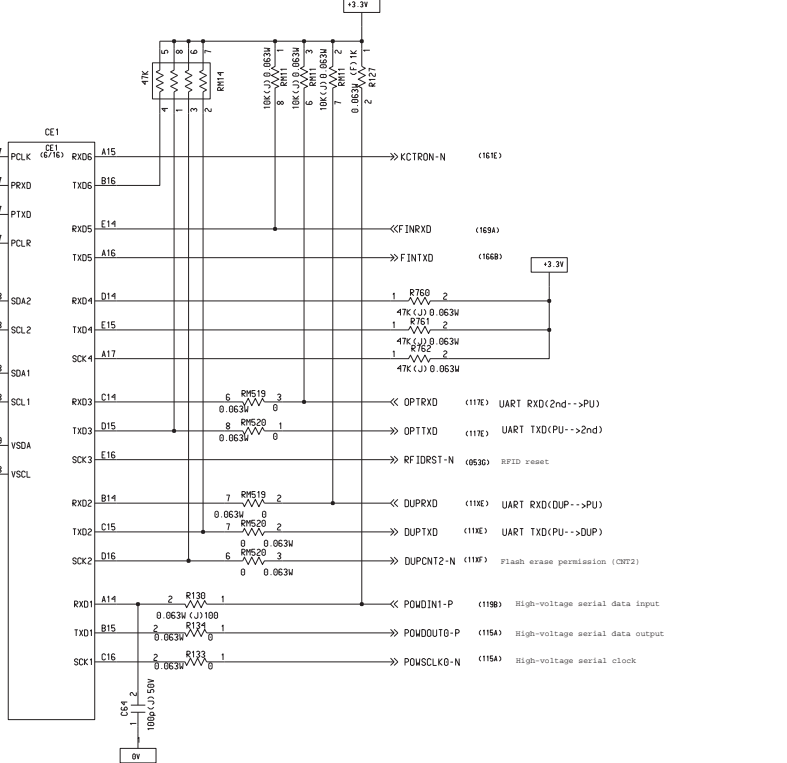
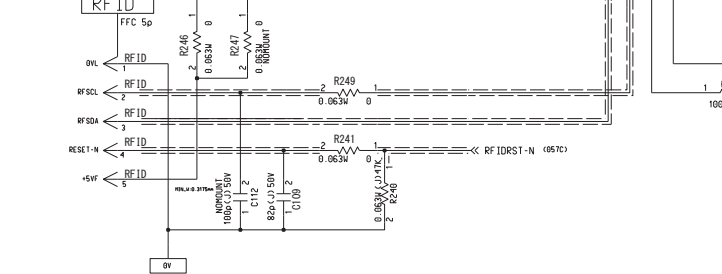
2243105P01101-FCT
Control panel I/F

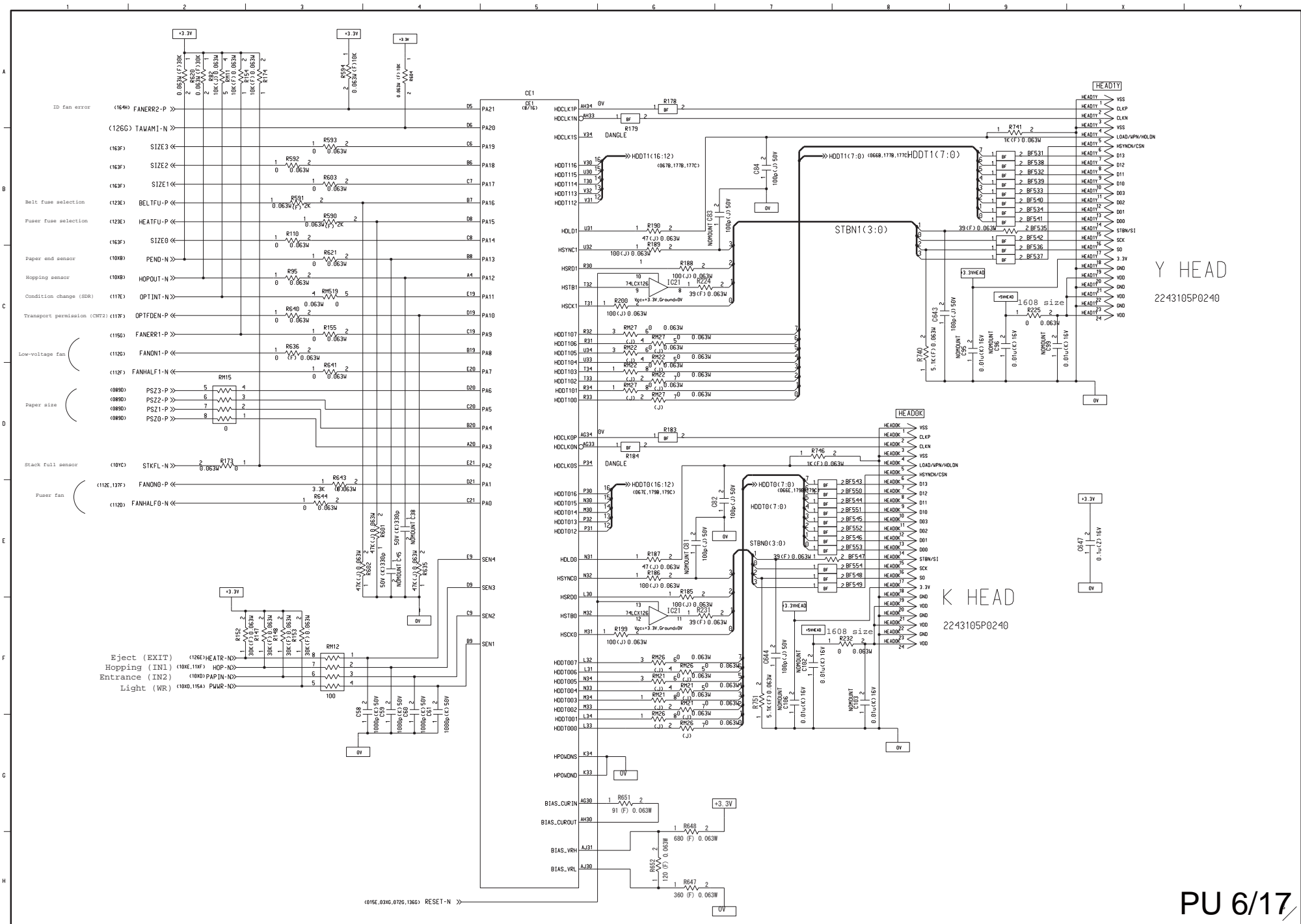


2243105P00601-FCT
Env. sensor



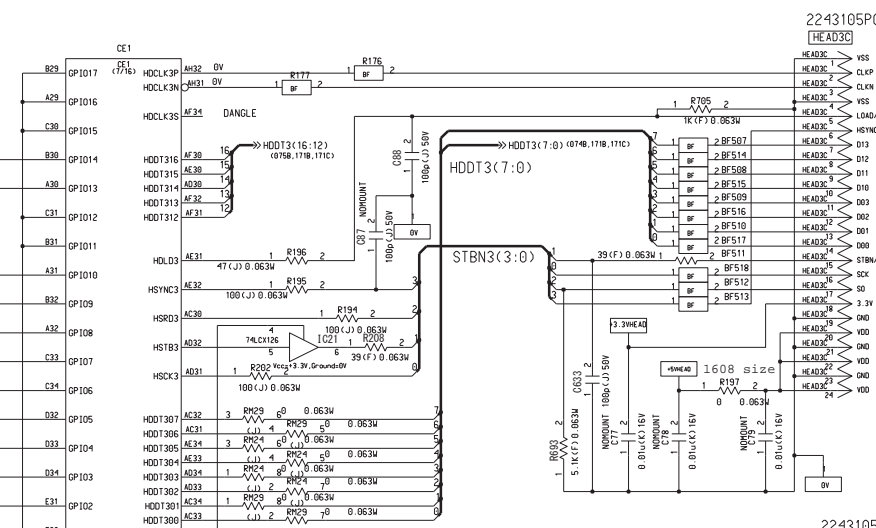
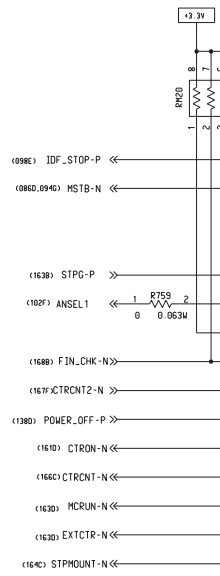
2243105P00501-FCT
RF ID





Y HEAD
2243105P0240

K HEAD
2243105P0240

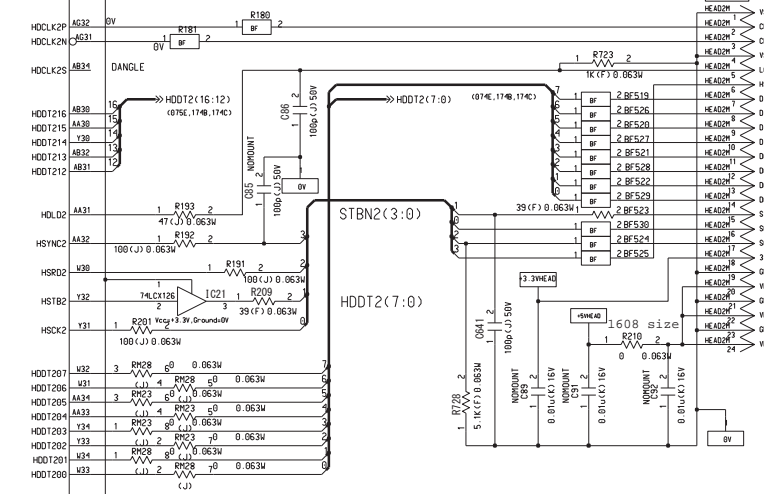
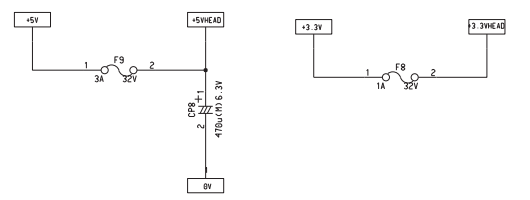


2243105P02401-FCT

C HEAD

2243105P0240

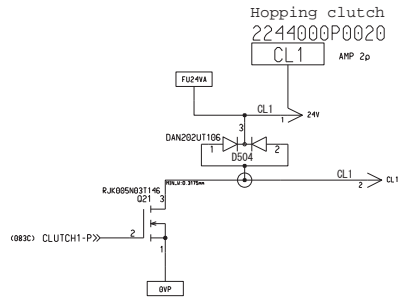
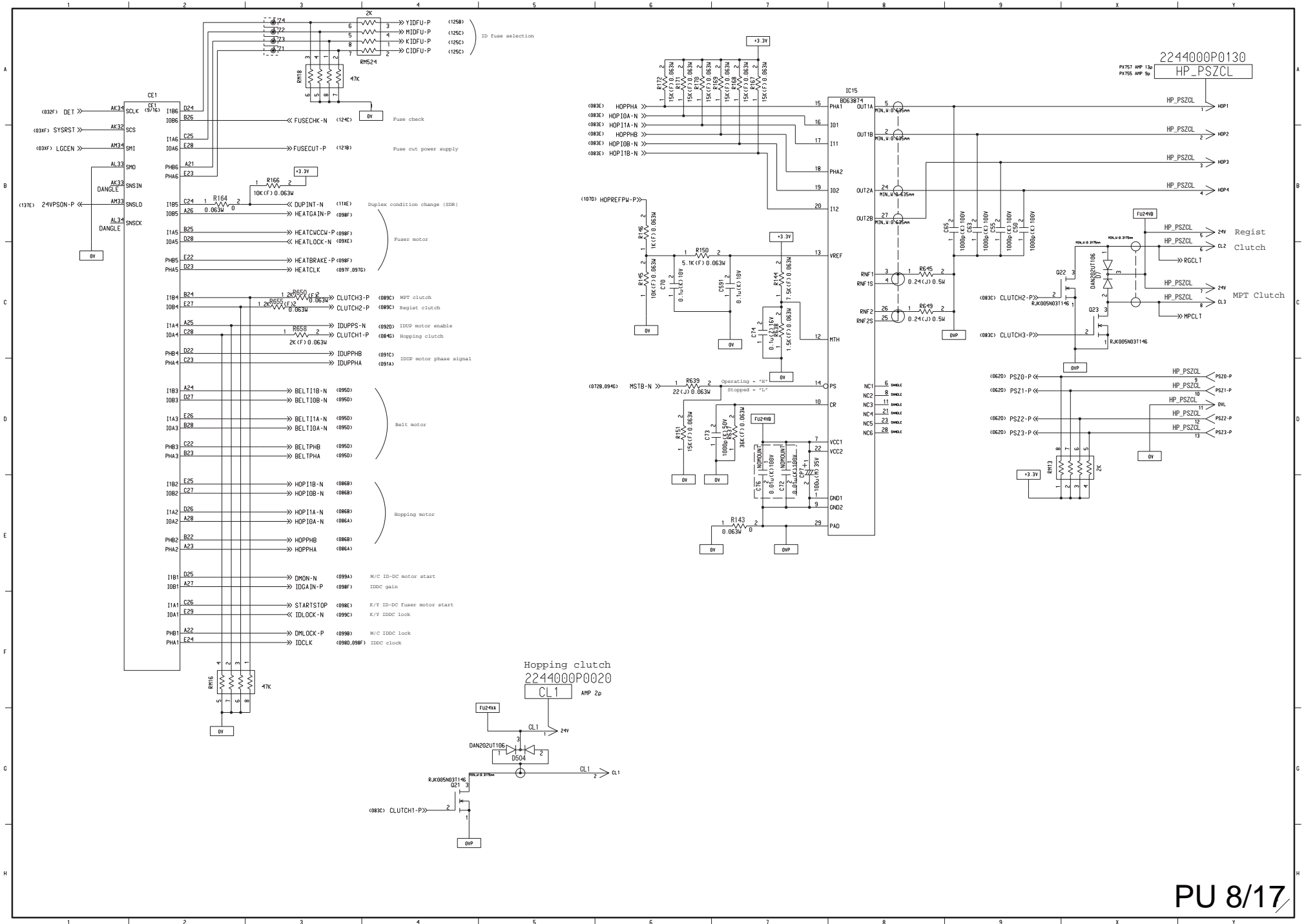
(015E,034G,064H,136G) RESET-N

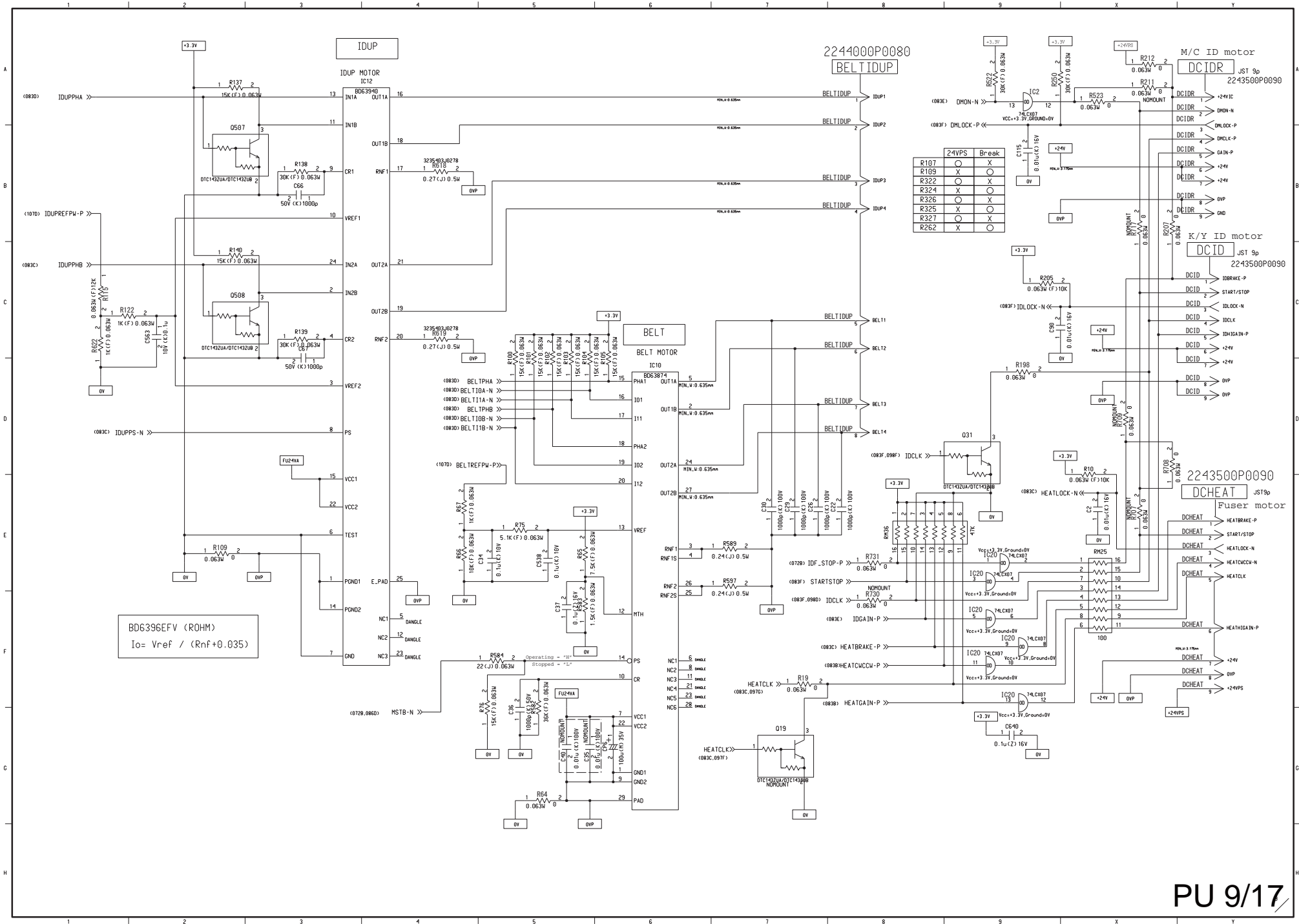


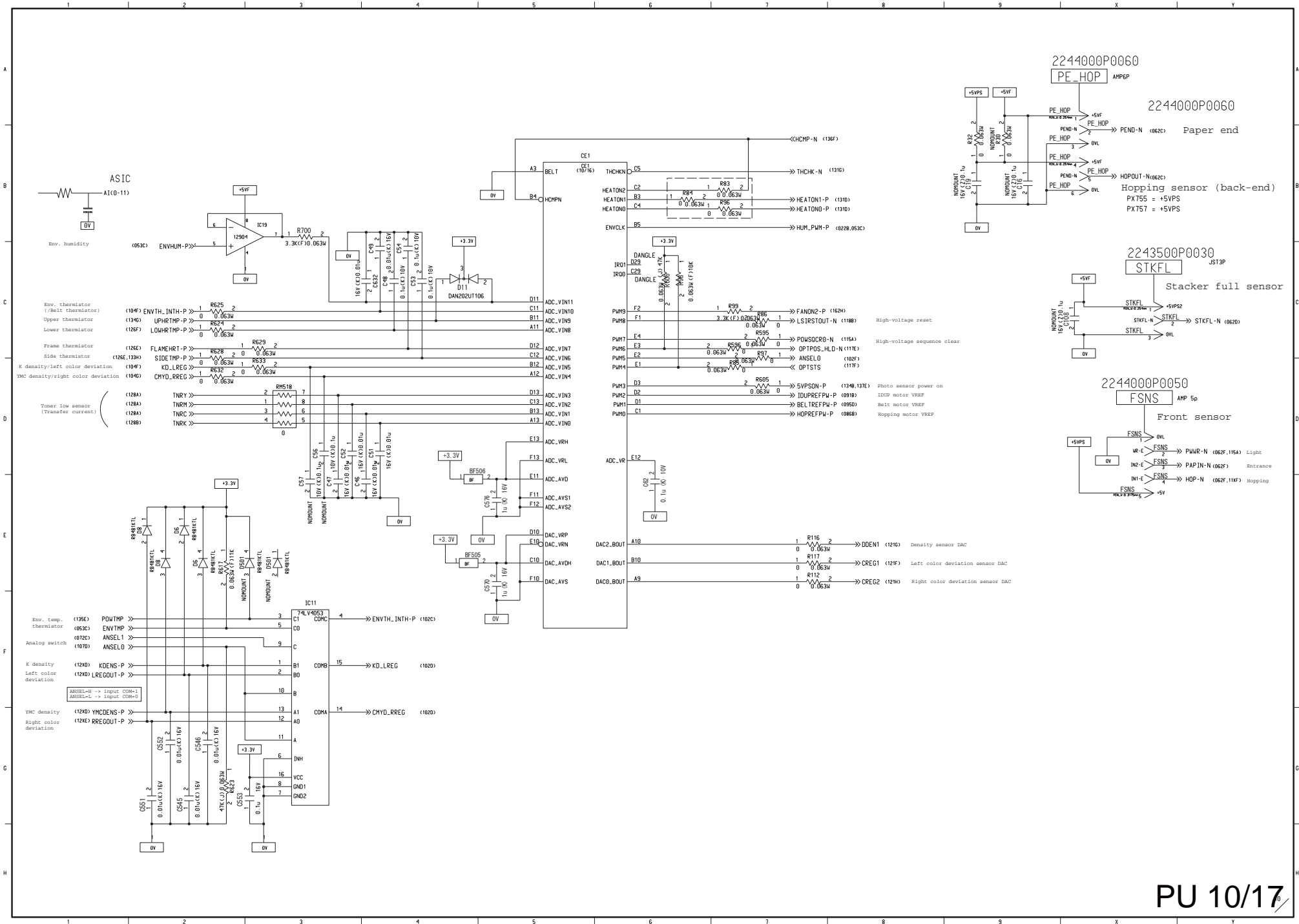
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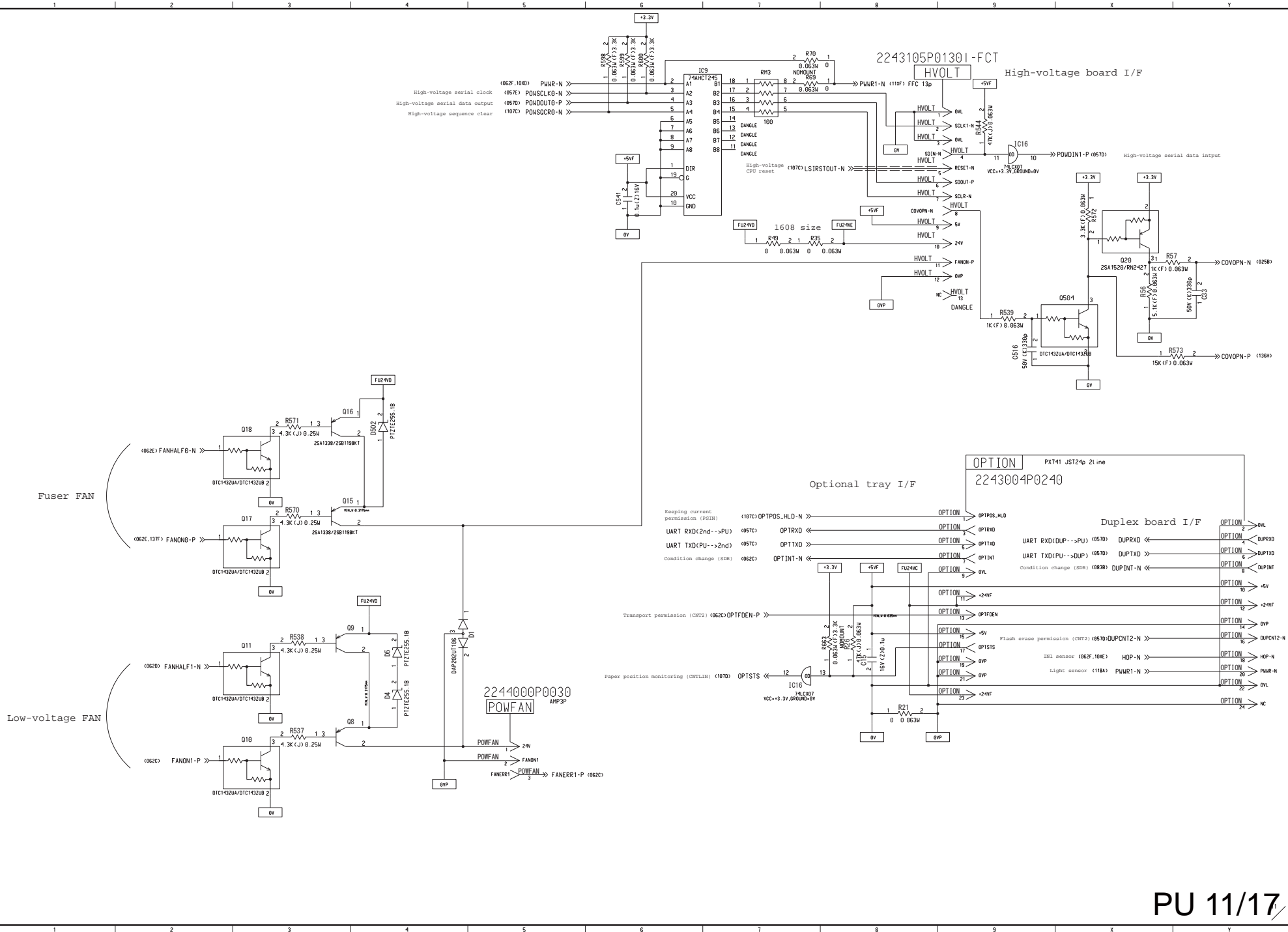
M HEAD

2243105P0240









2243105P01101 -FCT

SSNS

Toner sensor board I/F

+5VPS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

SSNS

2243105P02001 -FCT

RELAY

Relay board I/F

FFC 20p

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

RELAY

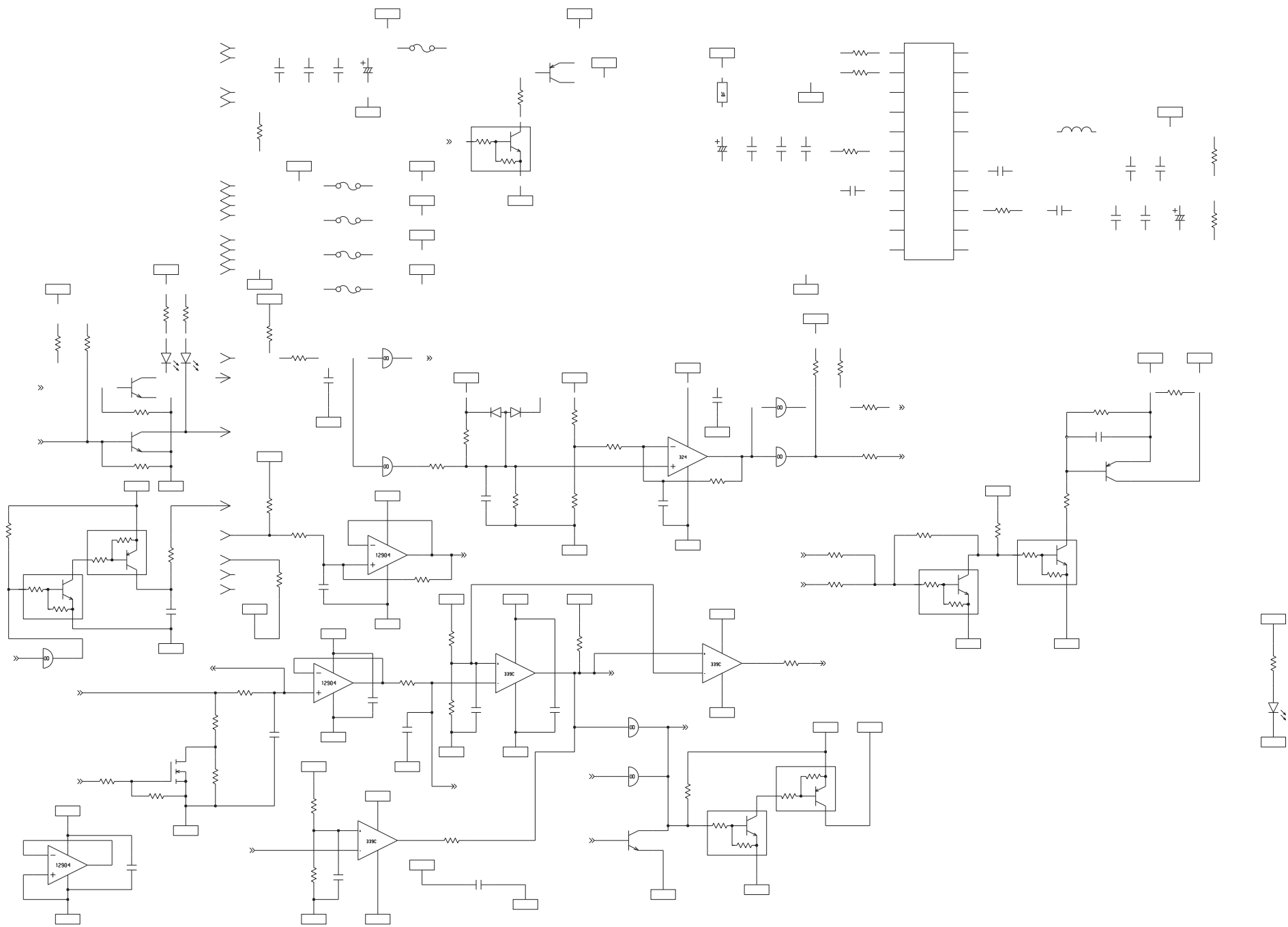
RELAY

Color density correction

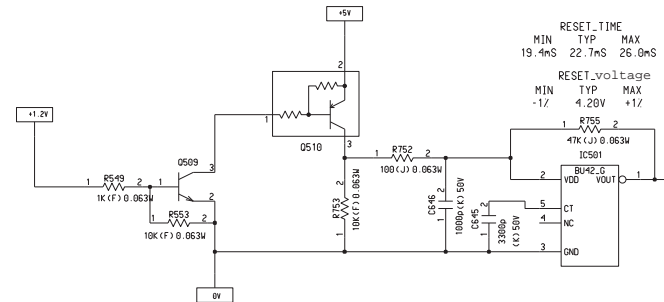
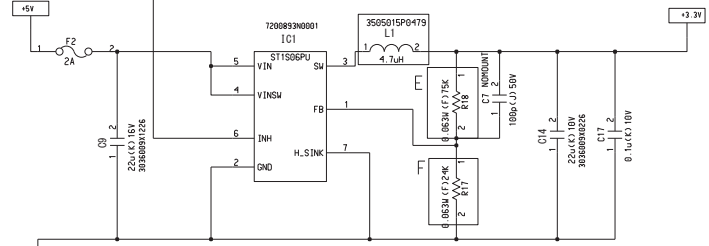
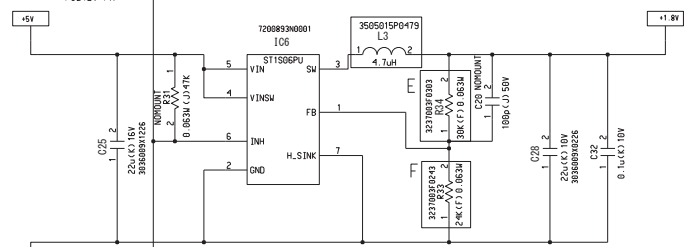
Black density correction

Color deviation correction L

Color deviation correction R

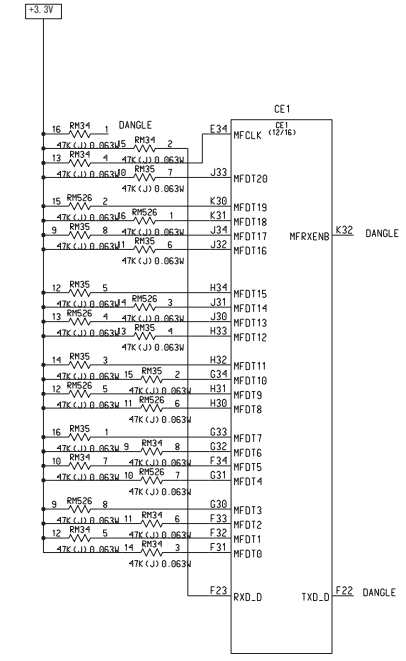
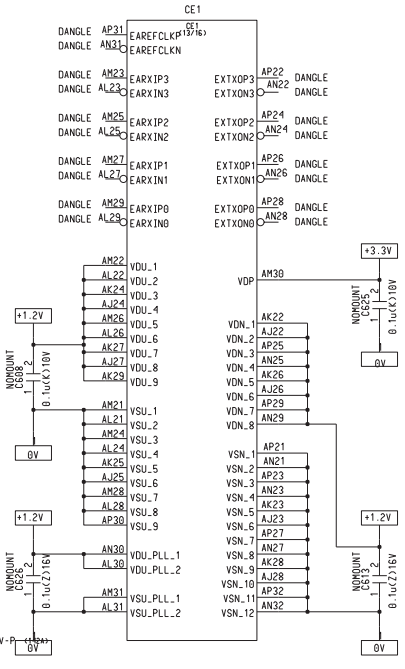


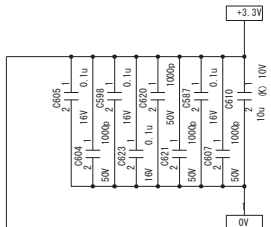
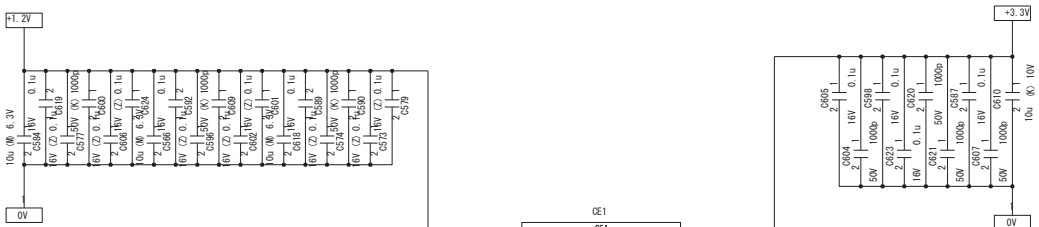
$$VO = 0.8 * (1 + E/F)$$



RESET TIME		
MIN	TYP	MAX
19.4ms	22.7ms	26.0ms

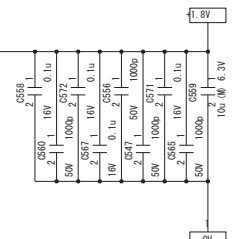
RESET voltage		
MIN	TYP	MAX
-1V	4.20V	+1V





CE1

F14	VDD_PD_1	F18	
F15	VDD_PD_2	F19	
F20	VDD_PD_3	F24	
F21	VDD_PD_4	F25	
F26	VDD_PD_5	G29	
F27	VDD_PD_6	H29	
L29	VDD_PD_7	N29	
M29	VDD_PD_8	P29	
U29	VDD_PD_9	W29	
V29	VDD_PD_10	Y29	
AC29	VDD_PD_11	AE29	
AD29	VDD_PD_12	AF29	
AA11	VDD_PD_13	L15	
AA12	VDD_PD_14	M15	
V11	VDD_PD_15	L18	
V12	VDD_PD_16	M18	
T11	VDD_PD_17	L21	
T12	VDD_PD_18	M21	
N11	VDD_PD_19	L24	
N12	VDD_PD_20	P24	
L13	VDD_PD_21	F23	
M13	VDD_PD_22	Y24	
L16	VDD_PD_23	Y23	
M16	VDD_PD_24	AD24	
L19	VDD_PD_25	AE21	
M19	VDD_PD_26	AE21	
L22	VDD_PD_27		
M22	VDD_PD_28		
N24	VDD_PD_29		
N23	VDD_PD_30		
T24	VDD_PD_31		
T23	VDD_PD_32		
V24	VDD_PD_33		
V23	VDD_PD_34		
AA24	VDD_PD_35		
AA23	VDD_PD_36		
AD22	VDD_PD_37		
AD19	VDD_PD_38		
AD18	VDD_PD_39		
AD19	VDD_PD_40		
AC19	VDD_PD_41		
AC19	VDD_PD_42		

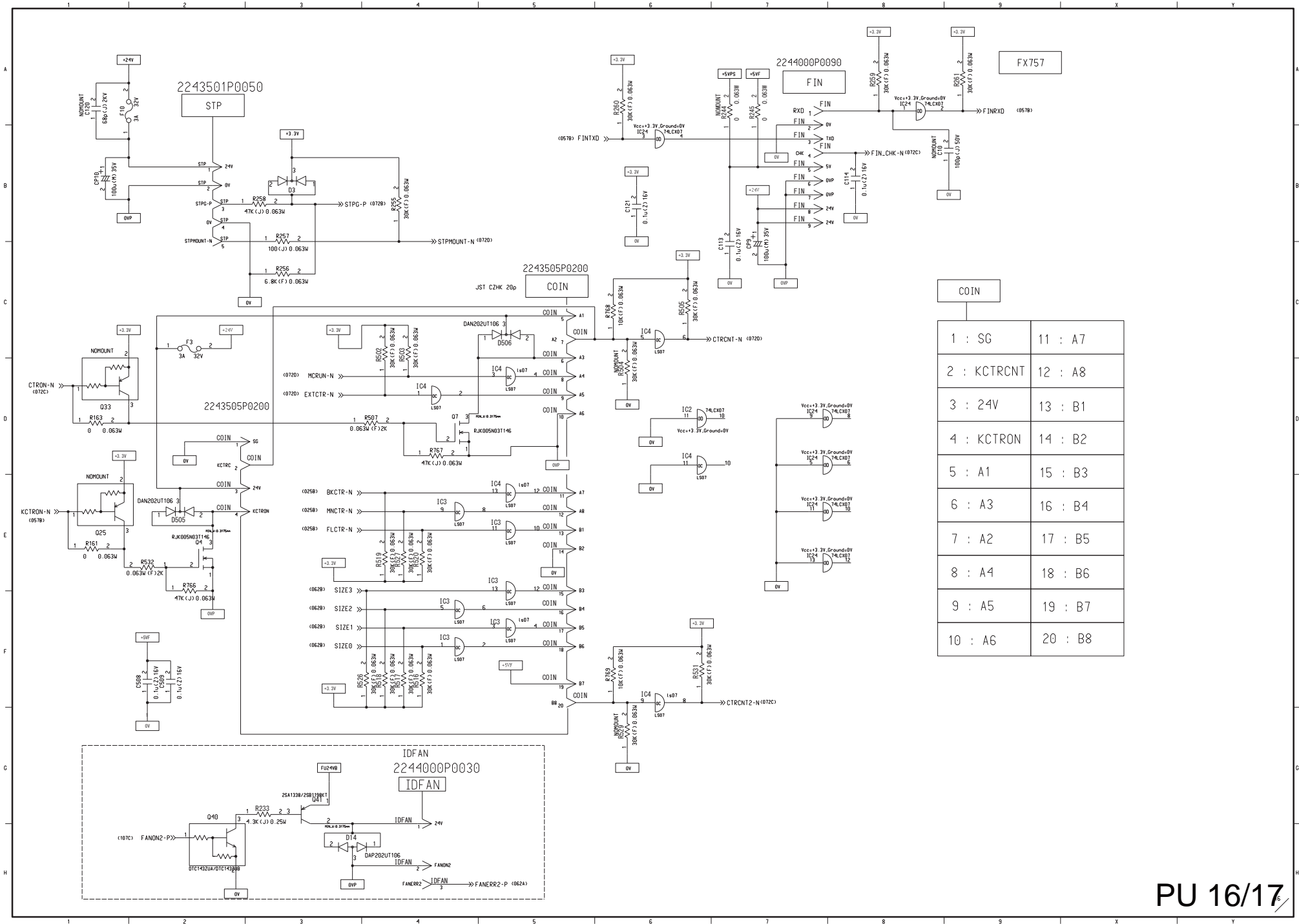


CE1

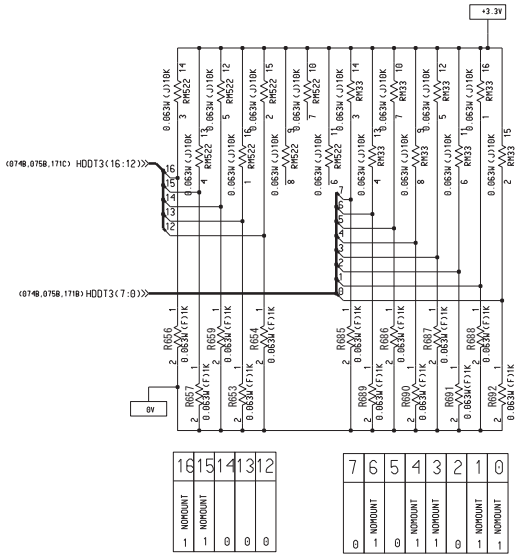
A1	GND_1	N17	
A2	GND_2	GND_50	
A6	GND_3	N19	
A8	GND_4	GND_60	
A33	GND_5	GND_61	
A34	GND_6	GND_62	
B1	GND_7	GND_64	
B2	GND_8	GND_65	
B14	GND_9	F23	
B27	GND_10	F14	
B34	GND_11	GND_67	
C3	GND_12	GND_68	
D4	GND_13	GND_69	
E5	GND_14	GND_70	
H29	GND_15	GND_71	
E33	GND_16	GND_72	
F3	GND_17	GND_73	
F4	GND_18	GND_74	
F7	GND_19	GND_75	
F9	GND_20	GND_76	
F16	GND_21	R1	
F17	GND_22	R2	
F28	GND_23	R6	
F29	GND_24	GND_78	
G1	GND_25	GND_79	
G2	GND_26	GND_80	
G3	GND_27	GND_81	
J1	GND_28	GND_82	
J2	GND_29	GND_83	
J3	GND_30	GND_84	
J6	GND_31	GND_85	
J29	GND_32	GND_86	
K3	GND_33	GND_87	
K29	GND_34	GND_88	
L1	GND_35	GND_89	
L2	GND_36	GND_90	
L12	GND_37	GND_91	
L14	GND_38	GND_92	
L17	GND_39	GND_93	
L20	GND_40	GND_94	
L23	GND_41	GND_95	
M2	GND_42	GND_96	
M3	GND_43	GND_97	
M6	GND_44	GND_98	
M11	GND_45	GND_99	
M12	GND_46	GND_100	
M14	GND_47	GND_101	
M17	GND_48	GND_102	
M20	GND_49	GND_103	
M23	GND_50	GND_104	
M24	GND_51	GND_105	
N2	GND_52	GND_106	
N3	GND_53	GND_107	
N4	GND_54	GND_108	
N13	GND_55	GND_109	
N14	GND_56	GND_110	
N15	GND_57	GND_111	
N16	GND_58	GND_112	

CE1

U18	GND_117	AB6	
U19	GND_118	AB11	
U20	GND_119	AB12	
GND_120	GND_120	AB13	
U22	GND_121	AB14	
U23	GND_122	AB15	
GND_123	GND_123	AB16	
U24	GND_124	AB17	
V5	GND_125	AB18	
V6	GND_126	AB19	
U25	GND_127	AB20	
V13	GND_128	AB21	
V14	GND_129	AB22	
V15	GND_130	AB23	
GND_131	GND_131	AB24	
V18	GND_132	AB25	
V19	GND_133	AC1	
V20	GND_134	AC2	
Y21	GND_135	AC11	
Y22	GND_136	AC12	
Y23	GND_137	AC13	
W5	GND_138	AC14	
W6	GND_139	AC17	
W11	GND_140	AC20	
R11	GND_141	AC23	
R12	GND_142	AC24	
R13	GND_143	AC3	
R14	GND_144	AD3	
R16	GND_145	AD14	
R17	GND_146	AD17	
R18	GND_147	AD20	
R19	GND_148	AD23	
W20	GND_149	AE1	
W21	GND_150	AE2	
W22	GND_151	AE3	
W23	GND_152	AE6	
Y1	GND_153	AE33	
Y2	GND_154	AE52	
Y6	GND_155	AE53	
Y14	GND_156	AE29	
Y15	GND_157	AE29	
Y16	GND_158	AE5	
Y17	GND_159	AE6	
Y18	GND_160	AE20	
Y19	GND_161	AE29	
Y20	GND_162	AE32	
Y21	GND_163	AE5	
Y22	GND_164	AE30	
Y23	GND_165	AE31	
Y24	GND_166	AE32	
AA3	GND_167	AE33	
AA4	GND_168	AE34	
AA13	GND_169	AN1	
AA14	GND_170	AN2	
AA15	GND_171	AN8	
AA16	GND_172	AN3	
AA17	GND_173	AN4	
AA18	GND_174	AP1	
AA19	GND_175	AP5	
AA20	GND_176	AP7	
AA21	GND_177	AP9	
AA22	GND_178	AP3	
AA29	GND_179	AP4	
AB2	GND_180	AP24	
AB3			



1 : SG	11 : A7
2 : KCTRCNT	12 : A8
3 : 24V	13 : B1
4 : KCTRON	14 : B2
5 : A1	15 : B3
6 : A3	16 : B4
7 : A2	17 : B5
8 : A4	18 : B6
9 : A5	19 : B7
10 : A6	20 : B8



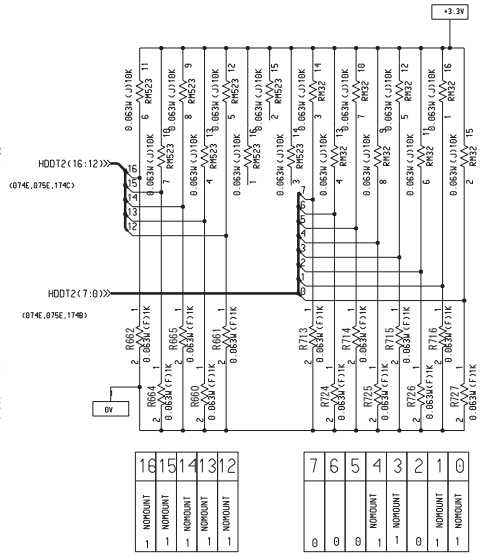
FH setting

PCIe non 1:PCIe out/0:normal
 Clk non 1:clk out/0:normal
 ext armored 1:use/0:inner ARM

user logic test 1:test/0:normal
 ARM boot 1:ARM/0:PCIe
 PIM initial 1:Low/0:Hi-z

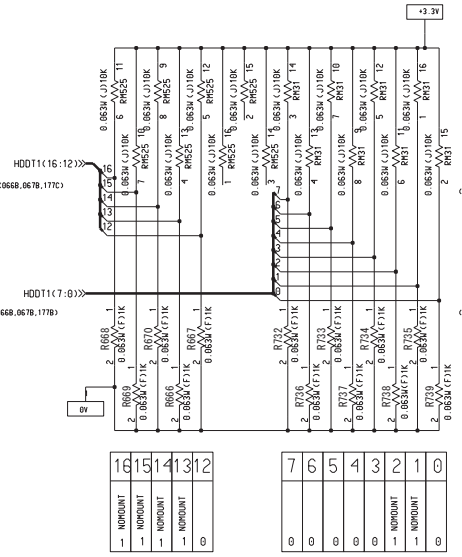
FH setting

multi use 1:multi/0:mono



FH setting

CE1 mem size:128Mbyte
 PCIe mem get en 1:non/0:get
 PCIe base 1:32bit/0:64bit
 Mem type 1:DDR3/0:DDR2
 DQS 1:different/al/0:single end
 Mem width 1:16bit/0:32bit



FH setting

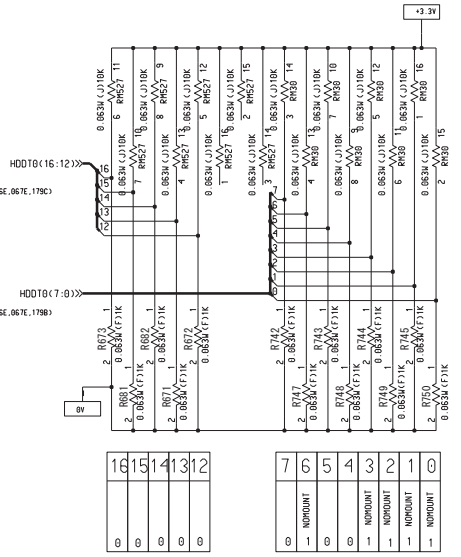
SSCC 1:Active/0:Non
 1:/2048/71024

param_sscc_div:x1

param_sscc_div:x16

SSCC 0:0.5/1:1/2:2/(3:3)

param_pll1_div:x1

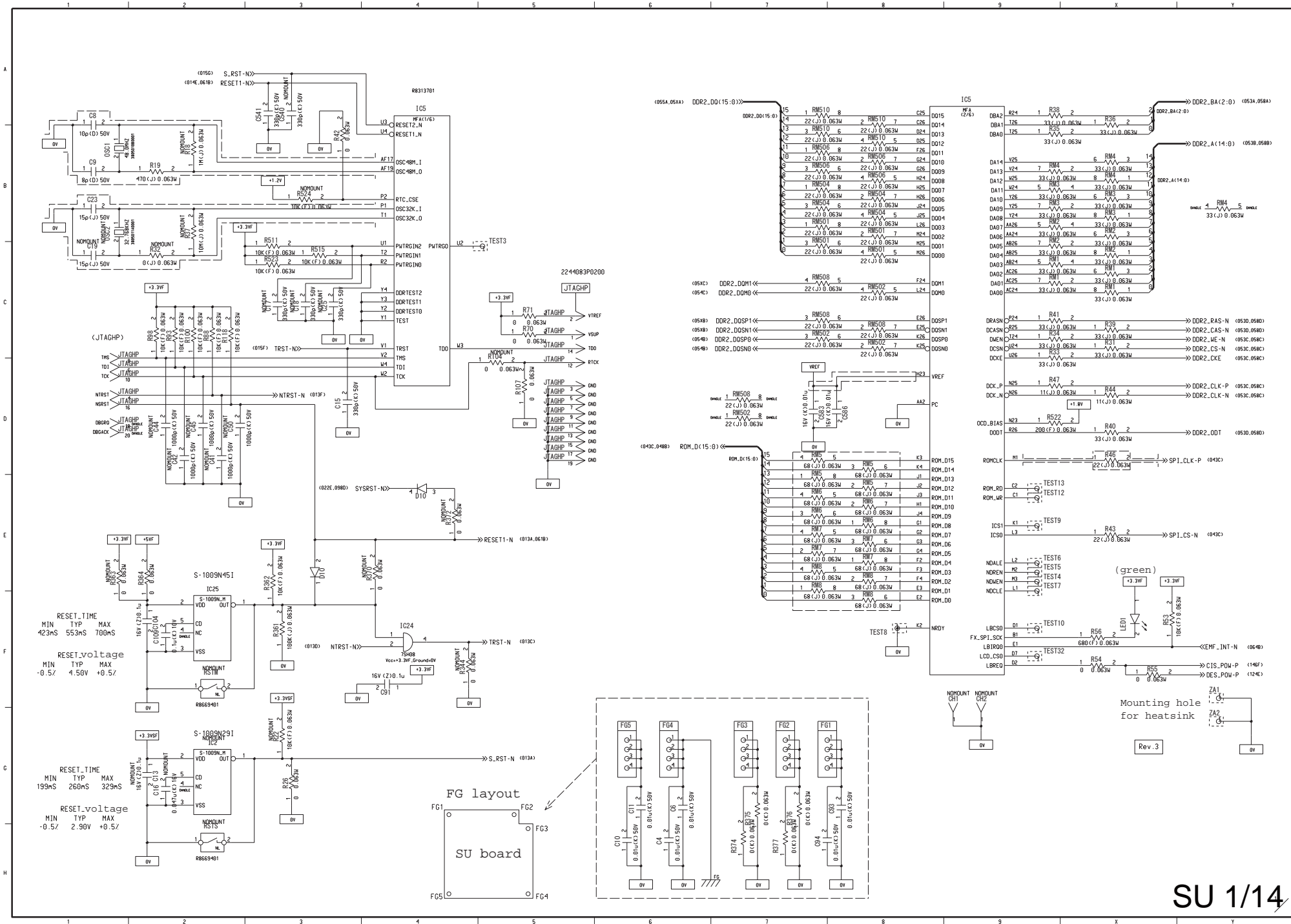


div setting

1:user logic sync/0:async

Fvco=33MHz*(param_pll1_mul(14:0)+16)>2
 Fcvo=33MHz*40=132MHz

1:0SC2/0:0SC1x1/2
 1:Main chip/0:sub chip
 1:Le:us/0:PCIe



SU 1/14

Mounting hole for heatsink

Rev. 3

FG layout

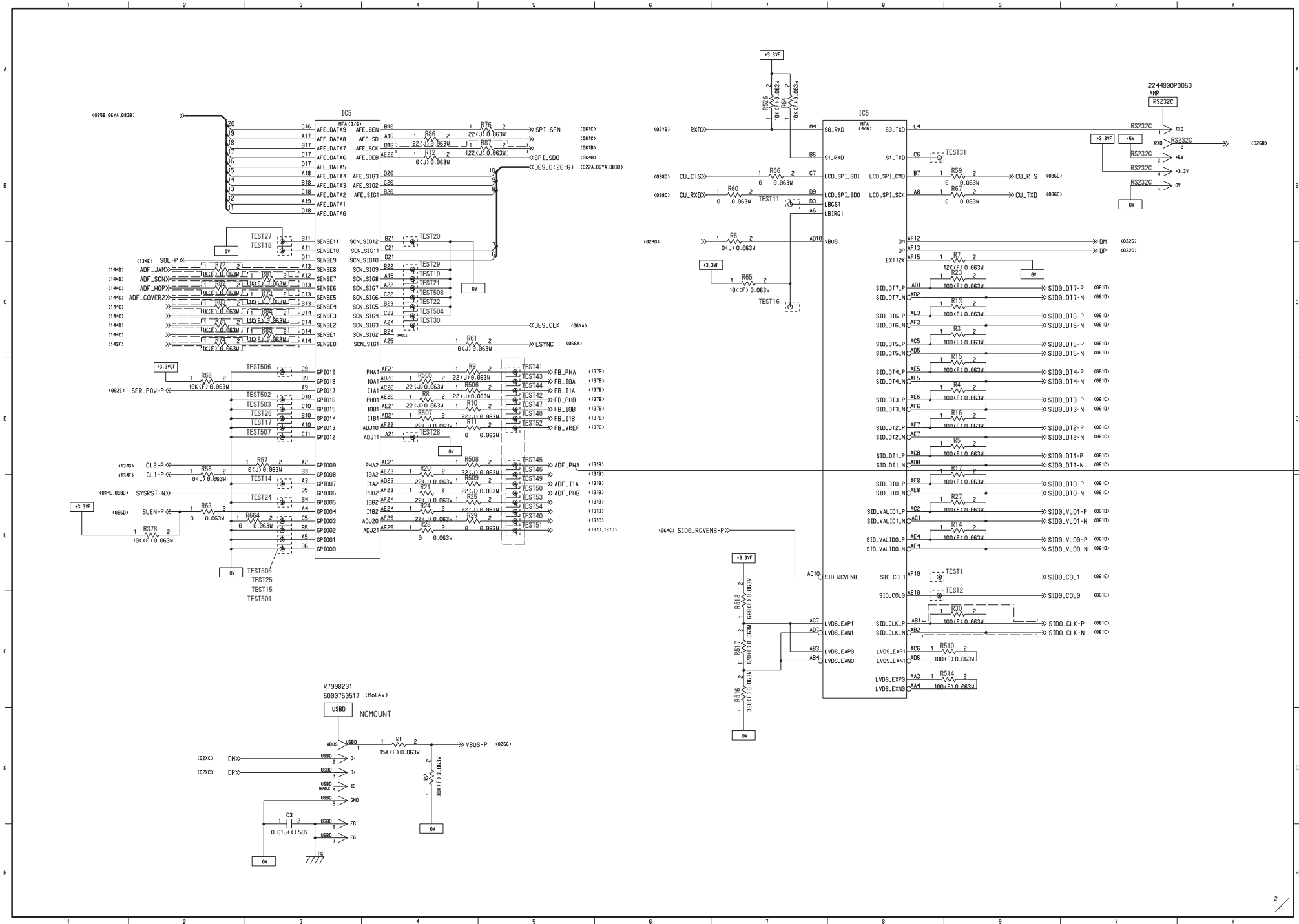
SU board

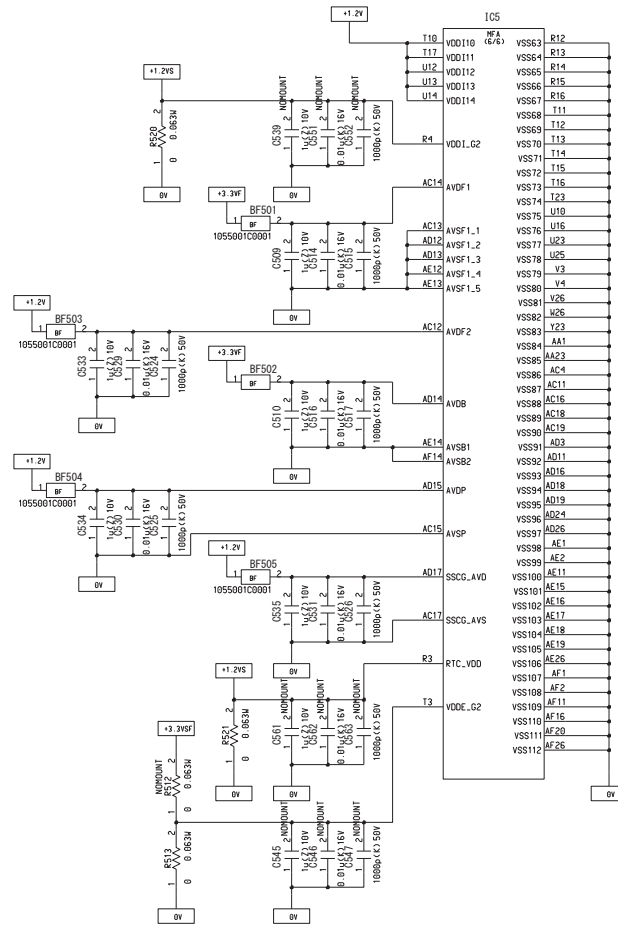
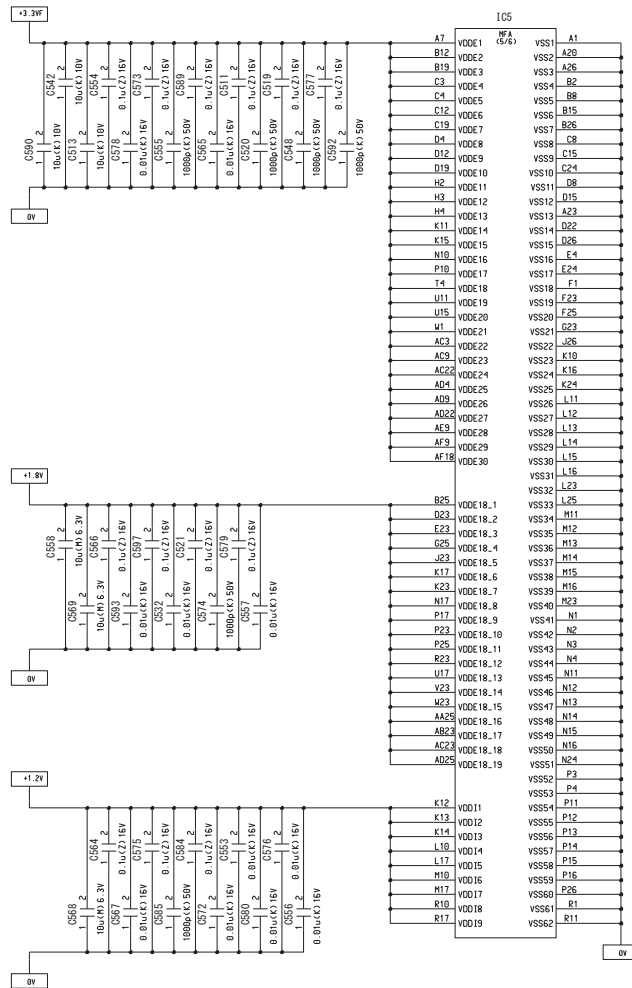
RESET TIME
MIN TYP MAX
423mS 553mS 700mS

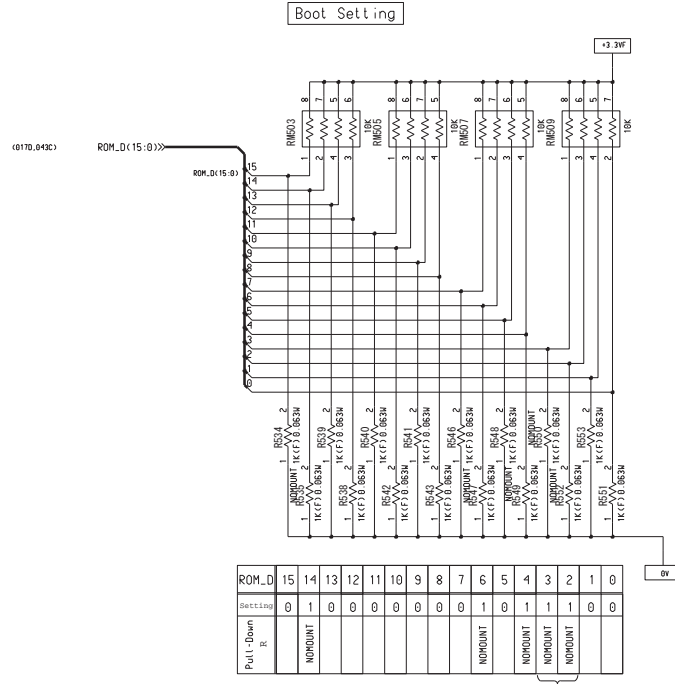
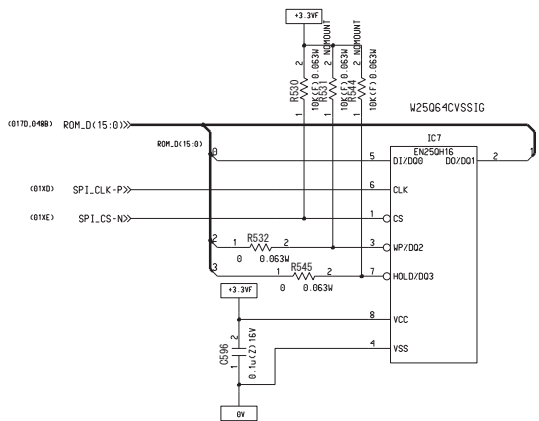
RESET voltage
MIN TYP MAX
-0.5/ 4.50V +0.5/

RESET TIME
MIN TYP MAX
199mS 260mS 329mS

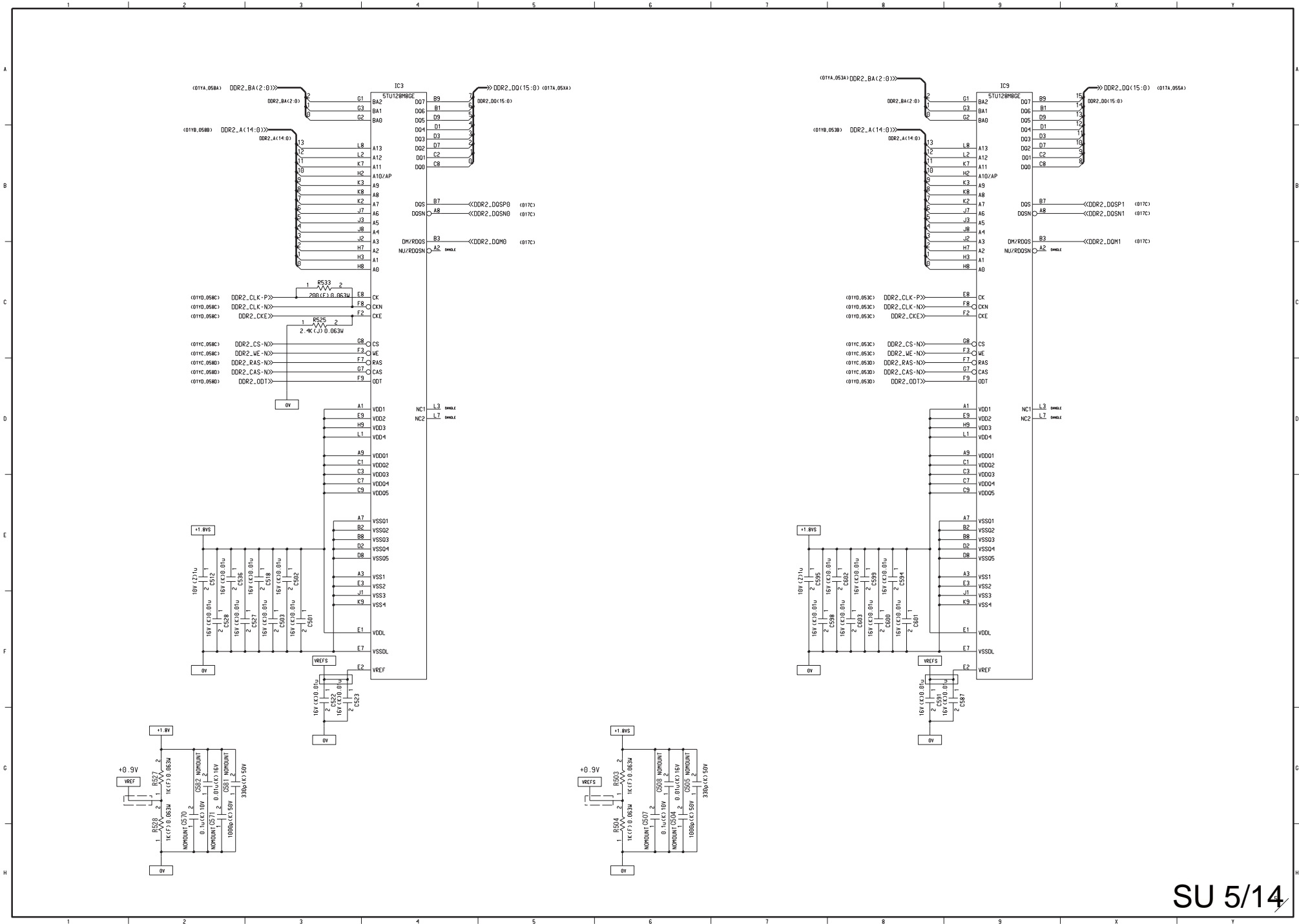
RESET voltage
MIN TYP MAX
-0.5/ 2.90V +0.5/

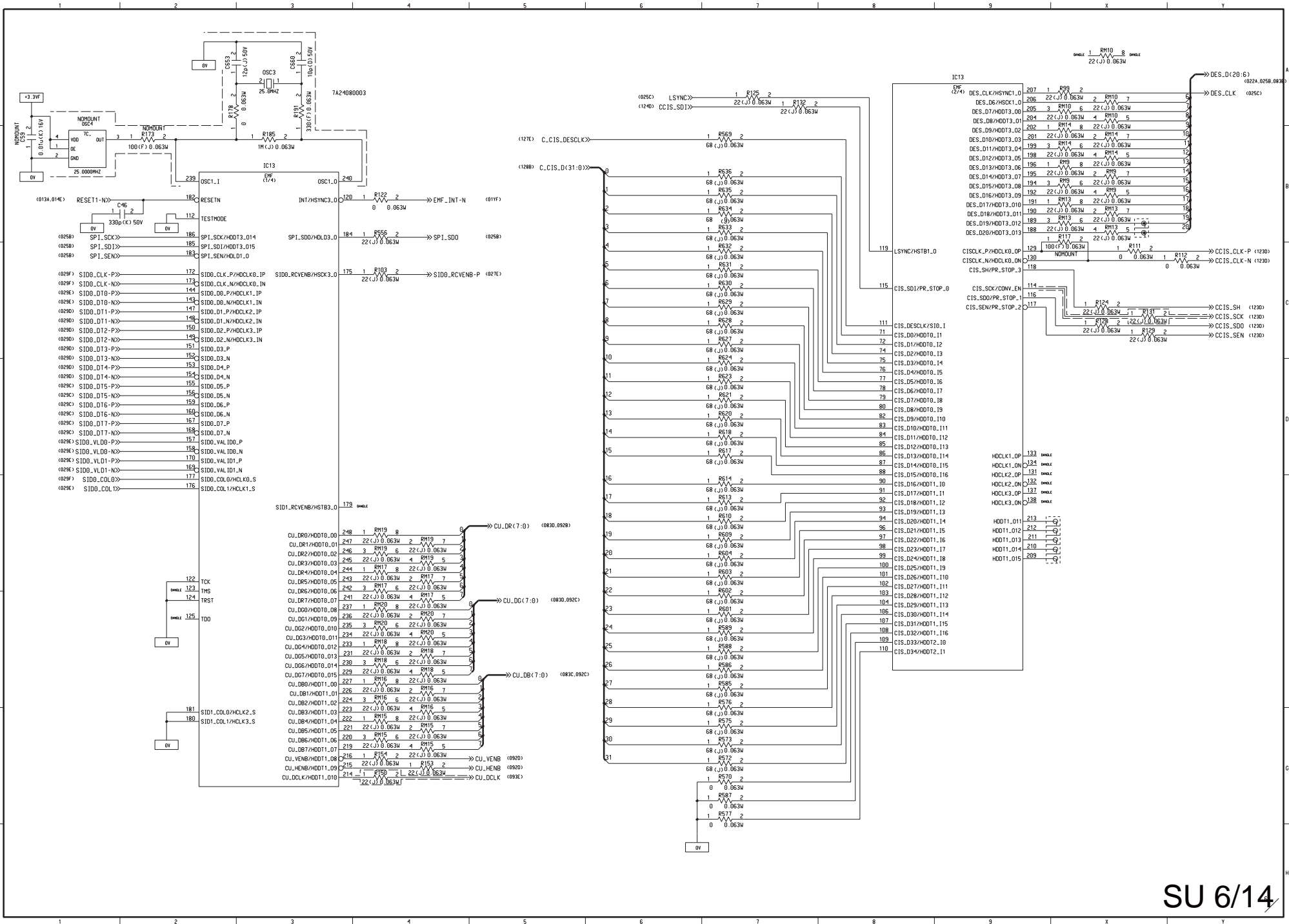






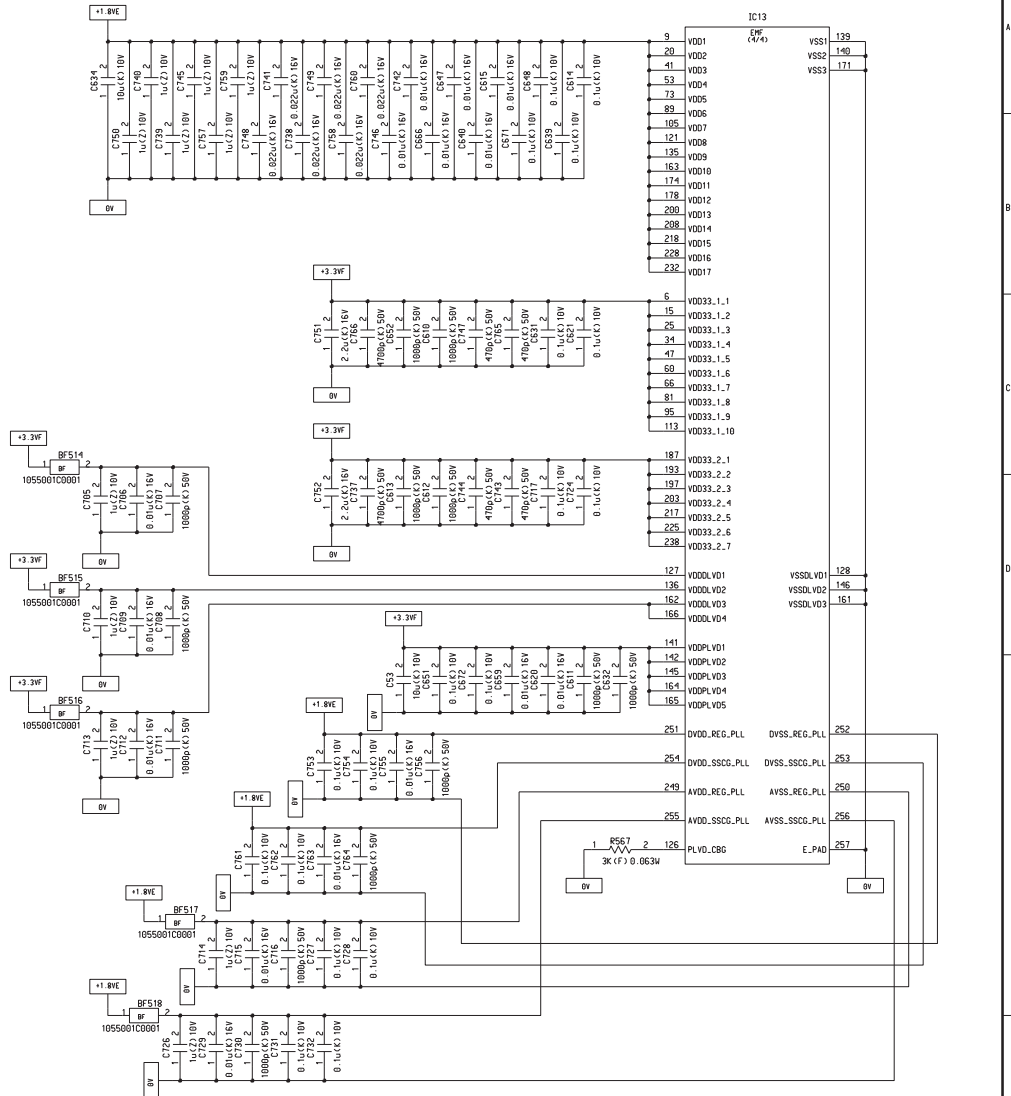
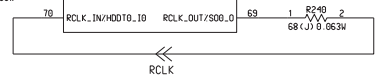
ROM_D	Setting	Pull-Up Res.
15	0	
14	1	NPOINT
13	0	
12	0	
11	0	
10	0	
9	0	
8	0	
7	0	
6	1	NPOINT
5	0	
4	1	NPOINT
3	1	NPOINT
2	1	NPOINT
1	0	
0	0	



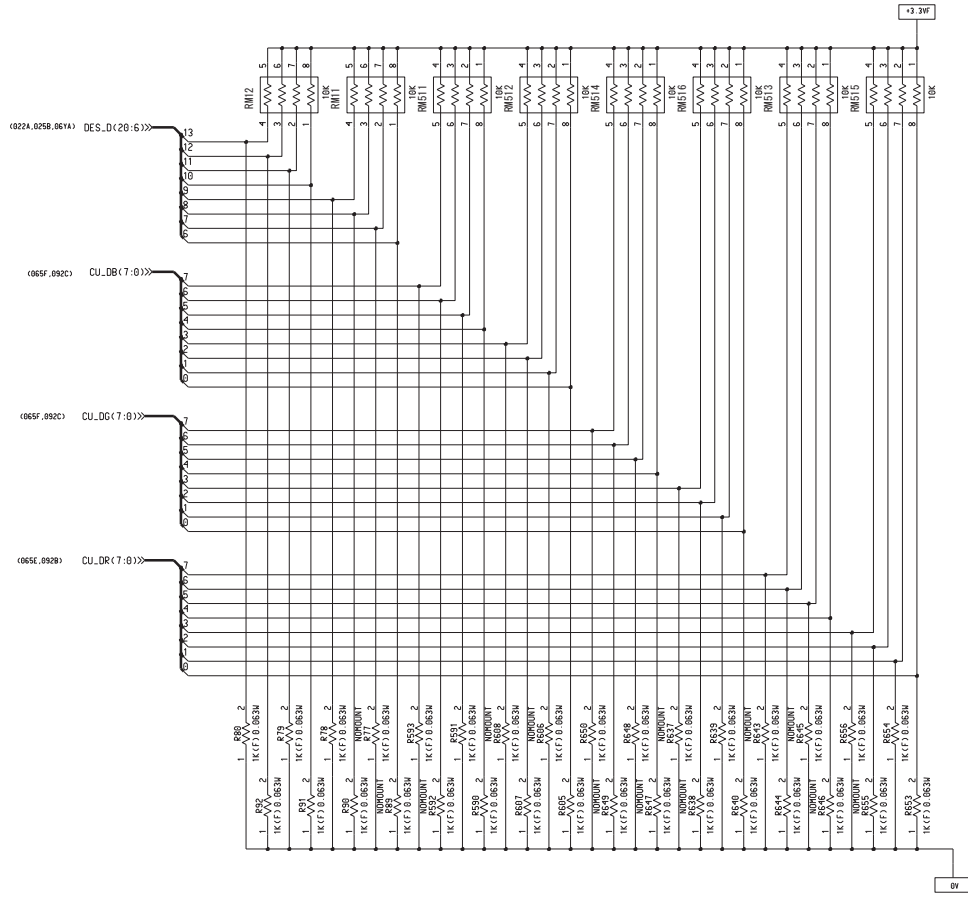


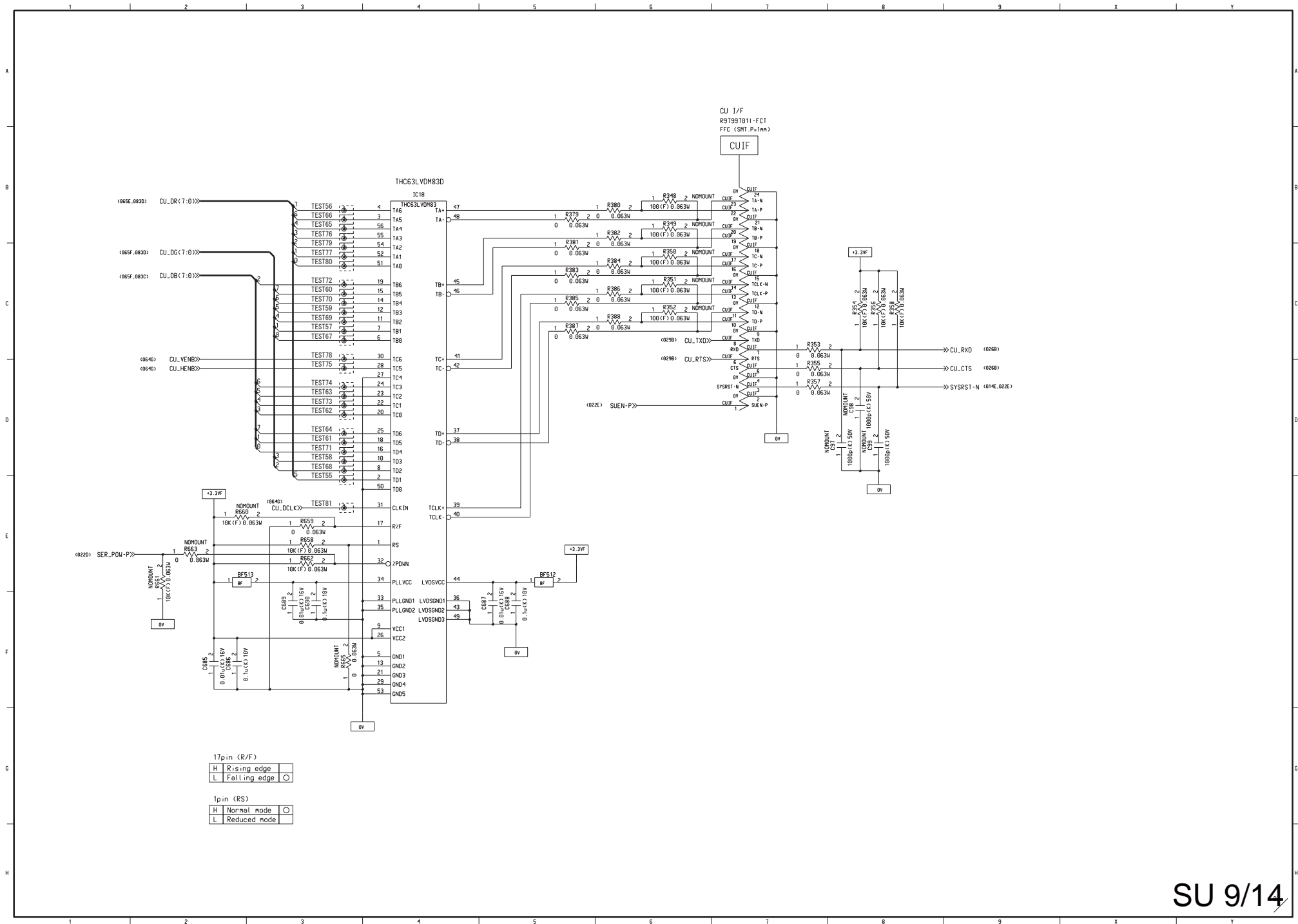
(1019) DD(31:0)

Pin	Device	Value	Device	Value	Device	Value	Device	Value							
31	5	RM22	4	48	00_31/HDDT3.10	EPH	00H_3/HSCK2.0	67	1	R241	2				
30	68(J)	0.063W	6	RM22	3	49	00_30/HDDT2.12	DDM_2/HSTR2.0	68	68(J)	0.063W	1	R254	2	
29	7	RM22	2	68(J)	0.063W	50	00_29/HDDT2.13	DDM_1/HDDT2.00	21	1	R247	2	68(J)	0.063W	2
28	68(J)	0.063W	8	RM22	1	51	00_28/HDDT2.14	DDM_0/HDDT2.01	22	68(J)	0.063W	1	R253	2	
27	5	RM27	4	68(J)	0.063W	52	00_27/HDDT2.15	DBA_1/HDDT2.02	23	1	R246	2	68(J)	0.063W	2
26	68(J)	0.063W	6	RM27	3	54	00_26/HDDT2.16	DBA_0/HDDT2.03	24	68(J)	0.063W	1	R250	2	
25	7	RM27	2	68(J)	0.063W	55	00_25/HDDT2.17	DA_12/HDDT2.04	26	1	R245	2	68(J)	0.063W	2
24	68(J)	0.063W	8	RM27	1	56	00_24/HDDT2.18	DA_11/HDDT2.05	27	68(J)	0.063W	4	RM29	5	
23	5	RM27	4	68(J)	0.063W	57	00_23/HDDT2.19	DA_10/HDDT2.06	28	3	RM29	5	68(J)	0.063W	5
22	68(J)	0.063W	6	RM21	3	58	00_22/HDDT2.10	DA_09/HDDT2.07	29	68(J)	0.063W	2	RM29	1	
21	7	RM21	2	68(J)	0.063W	59	00_21/HDDT2.11	DA_08/HDDT2.08	30	1	RM29	8	68(J)	0.063W	8
20	68(J)	0.063W	8	RM21	1	61	00_20/HDDT2.112	DA_07/HDDT2.09	31	68(J)	0.063W	4	RM29	5	
19	5	RM26	4	68(J)	0.063W	62	00_19/HDDT2.113	DA_06/HDDT2.10	32	3	RM26	3	68(J)	0.063W	3
18	68(J)	0.063W	6	RM26	3	63	00_18/HDDT2.114	DA_05/HDDT2.01	33	68(J)	0.063W	2	RM26	7	
17	7	RM26	2	68(J)	0.063W	64	00_17/HDDT2.115	DA_04/HDDT2.02	35	1	RM26	8	68(J)	0.063W	8
16	68(J)	0.063W	8	RM26	1	65	00_16/HDDT2.116	DA_03/HDDT2.03	36	68(J)	0.063W	4	RM28	5	
15	5	RM25	4	68(J)	0.063W	1	00_15/HDDT3.11	DA_02/HDDT2.014	37	3	RM28	8	68(J)	0.063W	8
14	68(J)	0.063W	6	RM25	3	2	00_14/HDDT3.12	DA_01/HDDT2.015	38	68(J)	0.063W	2	RM28	7	
13	7	RM25	2	68(J)	0.063W	3	00_13/HDDT3.13	DA_00/HDL2.0	40	1	RM28	8	68(J)	0.063W	8
12	68(J)	0.063W	8	RM25	1	4	00_12/HDDT3.14	DCASN/HSCK2.0	42	68(J)	0.063W	1	R247	2	
11	5	RM31	4	68(J)	0.063W	5	00_11/HDDT3.15	DCASN/HSCK2.0	43	1	R243	2	68(J)	0.063W	2
10	68(J)	0.063W	6	RM31	3	7	00_10/HDDT3.16	DWEN/HSTR8.0	44	68(J)	0.063W	1	R256	2	
9	7	RM31	2	68(J)	0.063W	8	00_09/HDDT3.17	DCSN/HSCK0.0	45	1	R242	2	68(J)	0.063W	2
8	68(J)	0.063W	8	RM31	1	10	00_08/HDDT3.18	DCKE/HDR0.0	46	68(J)	0.063W	1	R255	2	
7	5	RM24	4	68(J)	0.063W	11	00_07/HDDT2.19	DCKE/HDR0.0	39	1	R244	2	68(J)	0.063W	2
6	68(J)	0.063W	6	RM24	3	12	00_06/HDDT3.110	DCKE/HDR0.0	39	1	R244	2	68(J)	0.063W	2
5	7	RM24	2	68(J)	0.063W	13	00_05/HDDT3.111								
4	68(J)	0.063W	8	RM24	1	14	00_04/HDDT3.112								
3	5	RM30	4	68(J)	0.063W	16	00_03/HDDT3.113								
2	68(J)	0.063W	6	RM30	3	17	00_02/HDDT3.114								
1	7	RM30	2	68(J)	0.063W	18	00_01/HDDT3.115								
0	68(J)	0.063W	8	RM30	1	19	00_00/HDDT3.116								



Boot Setting



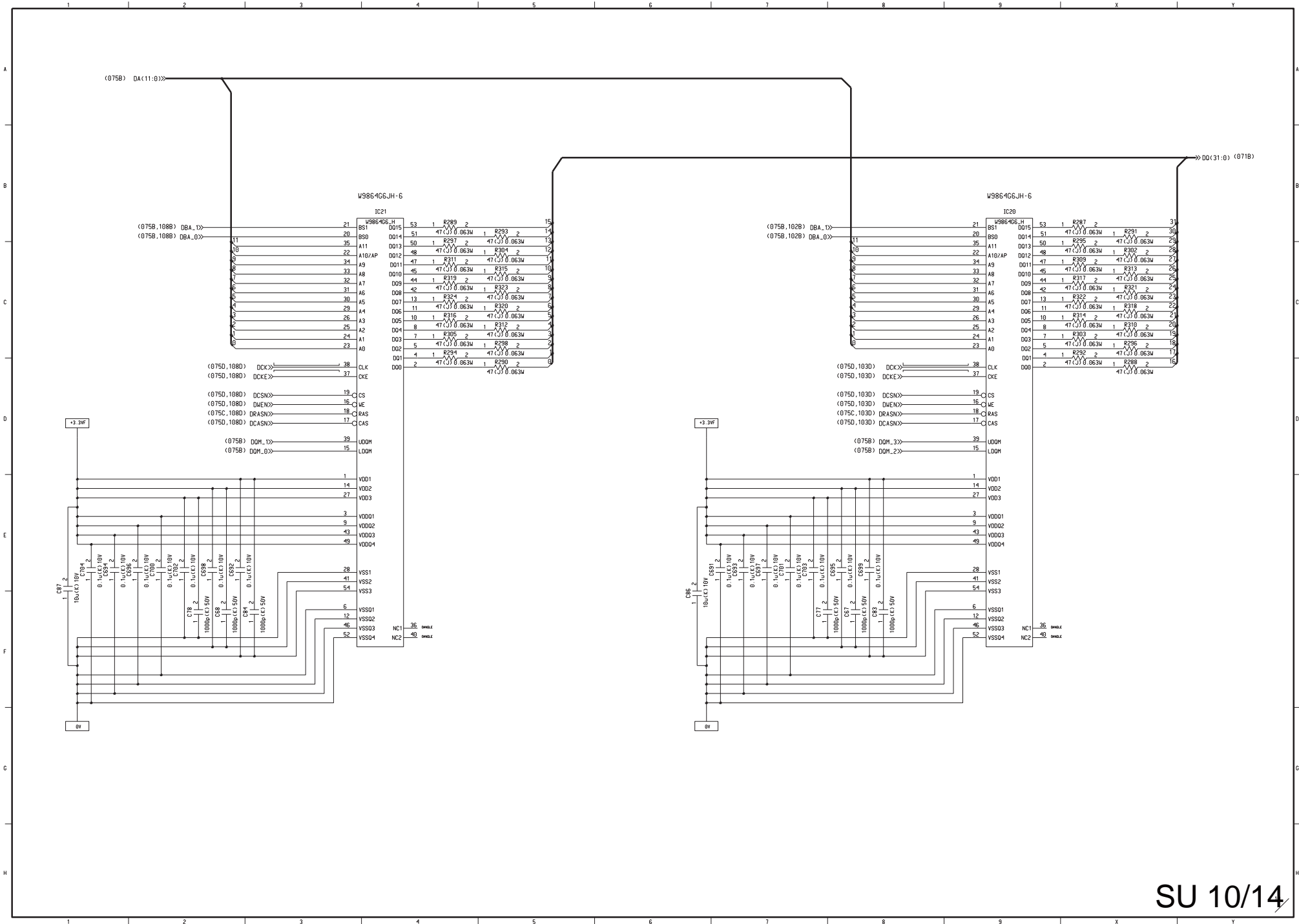


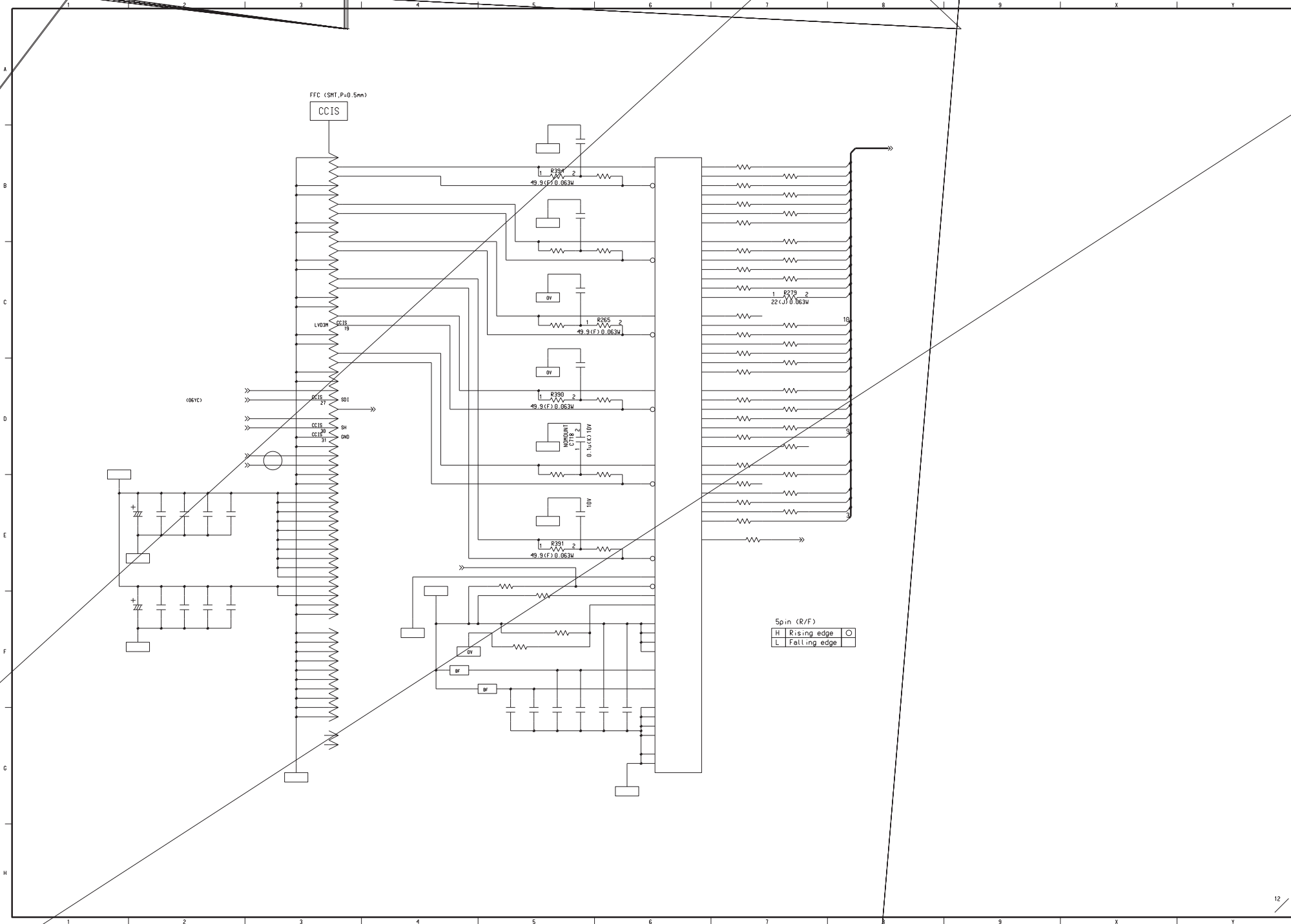
17pin (R/F)

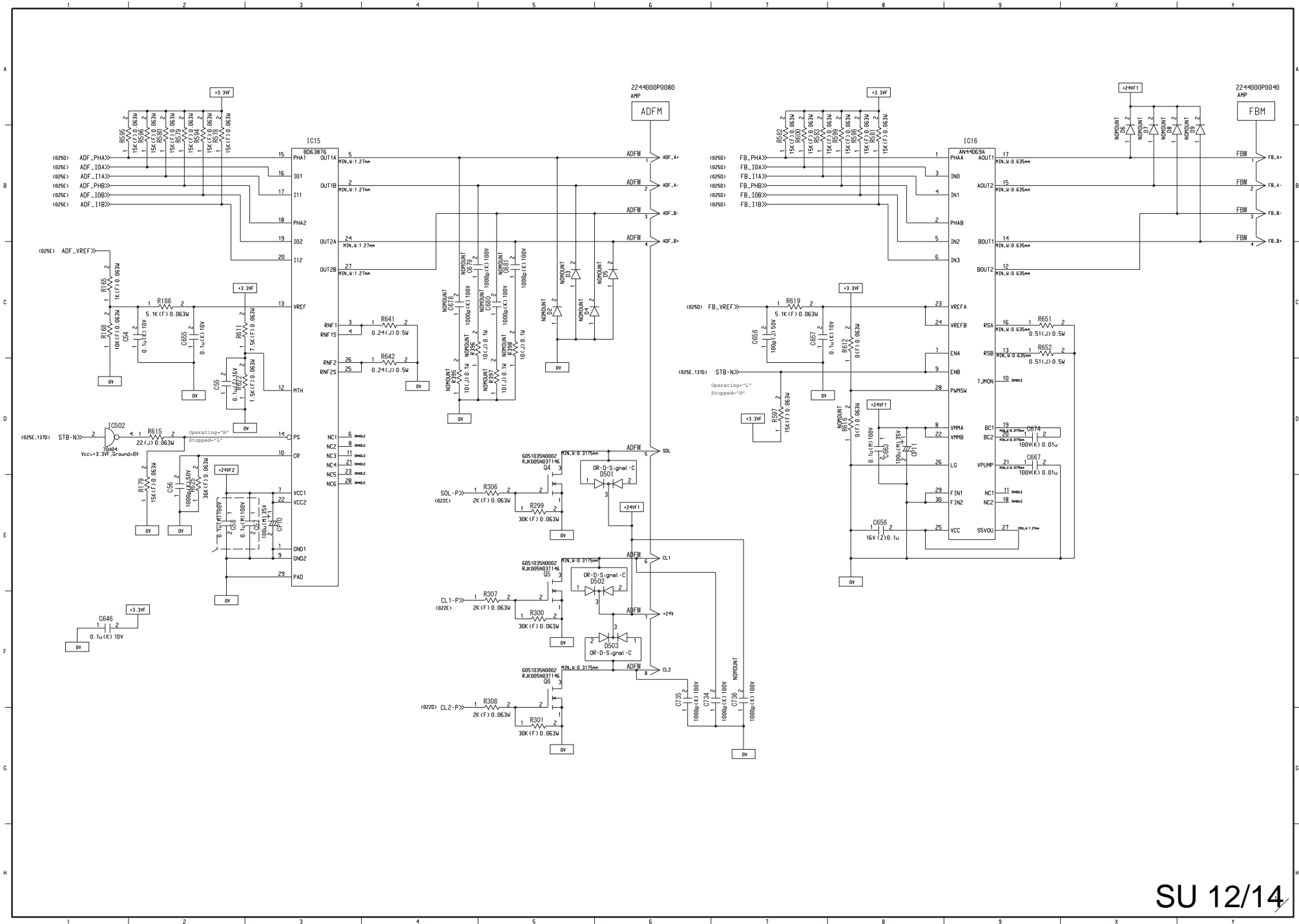
H	Rising edge
L	Falling edge

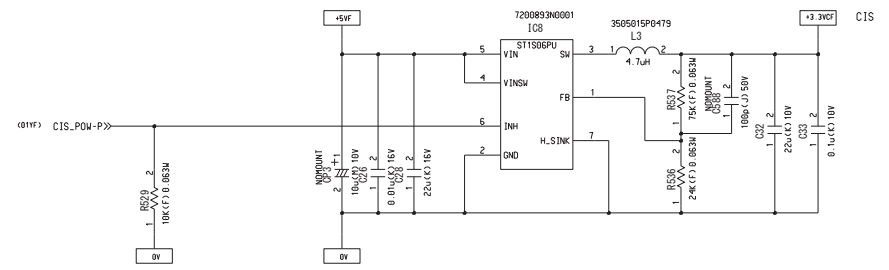
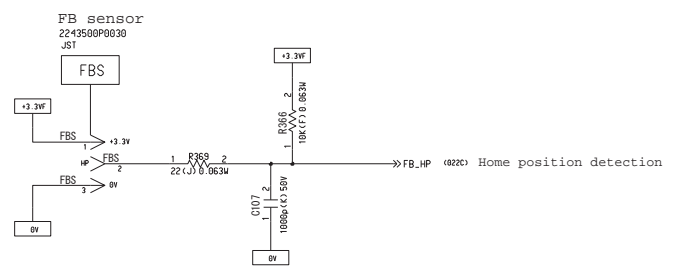
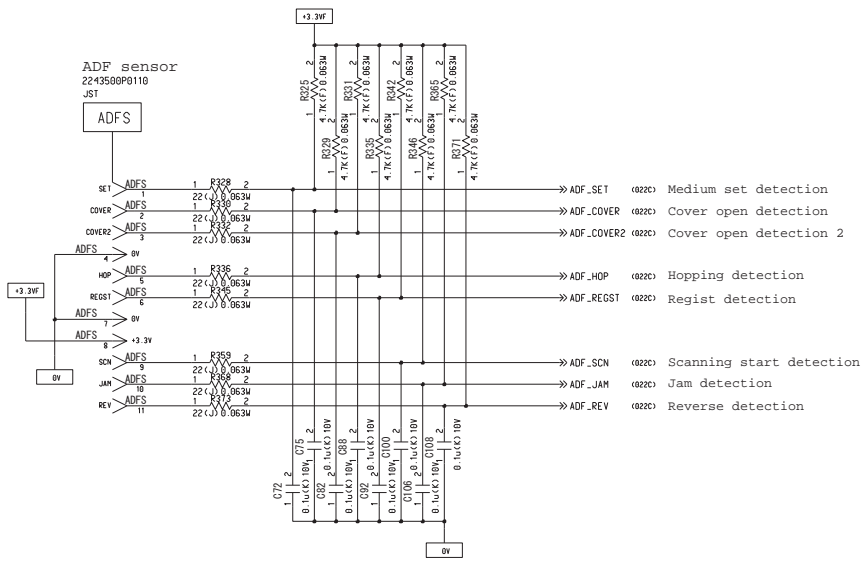
1pin (RS)

H	Normal mode
L	Reduced mode

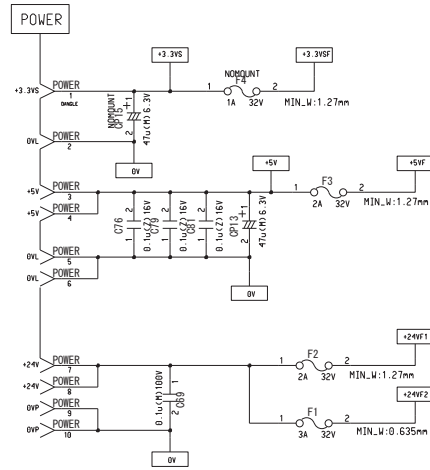








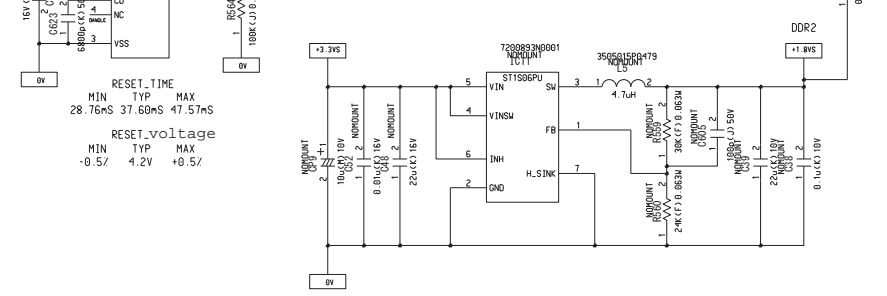
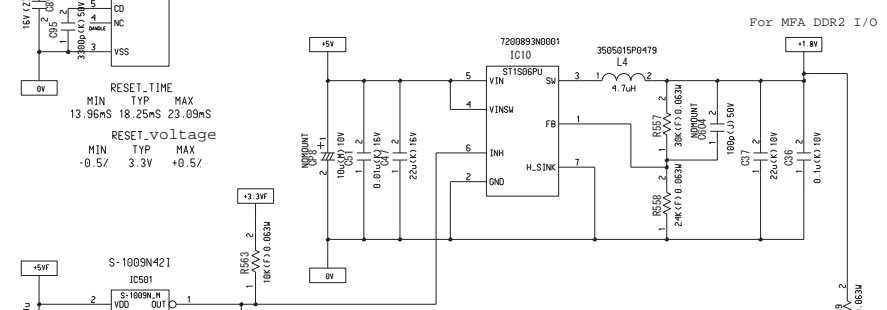
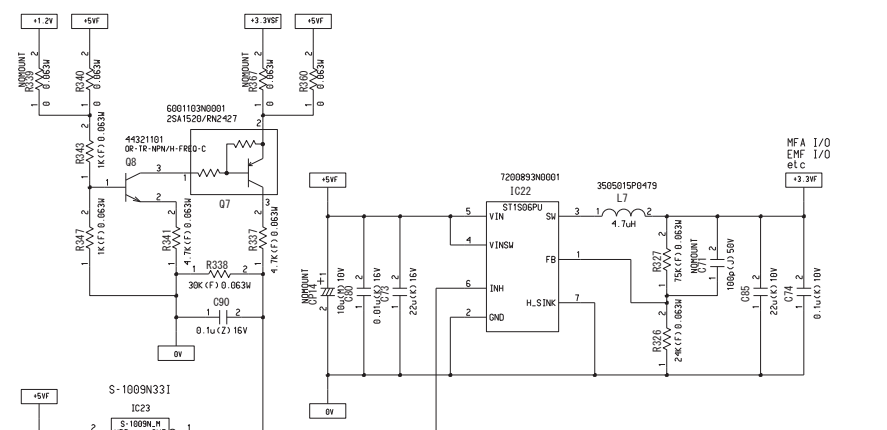
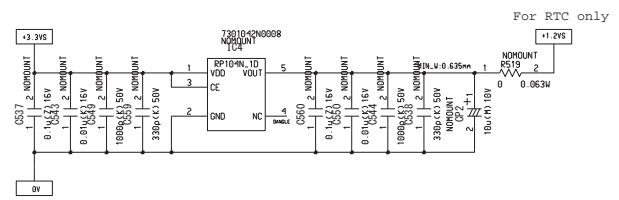
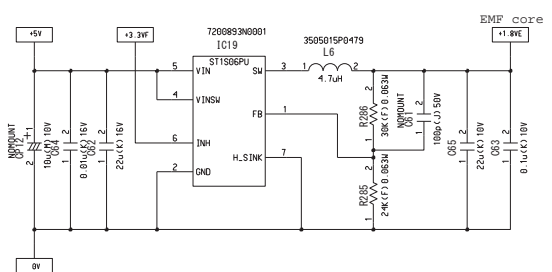
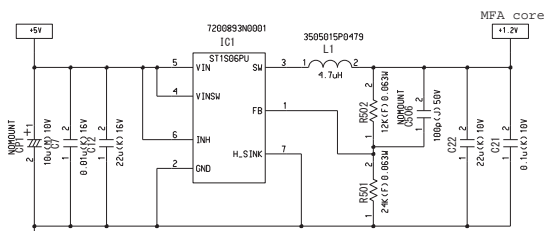
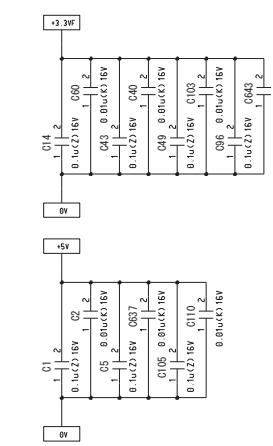
2243804P0160

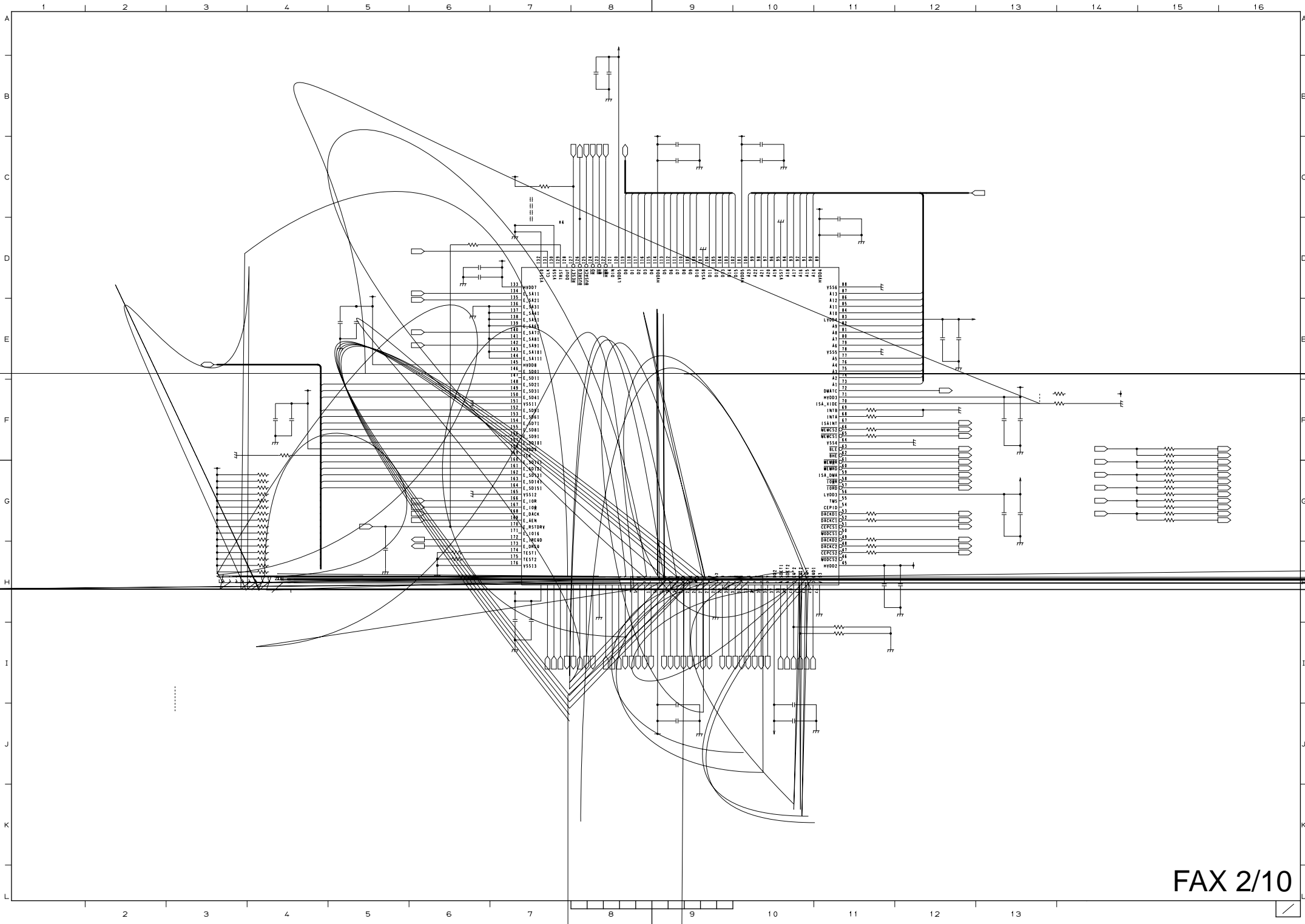


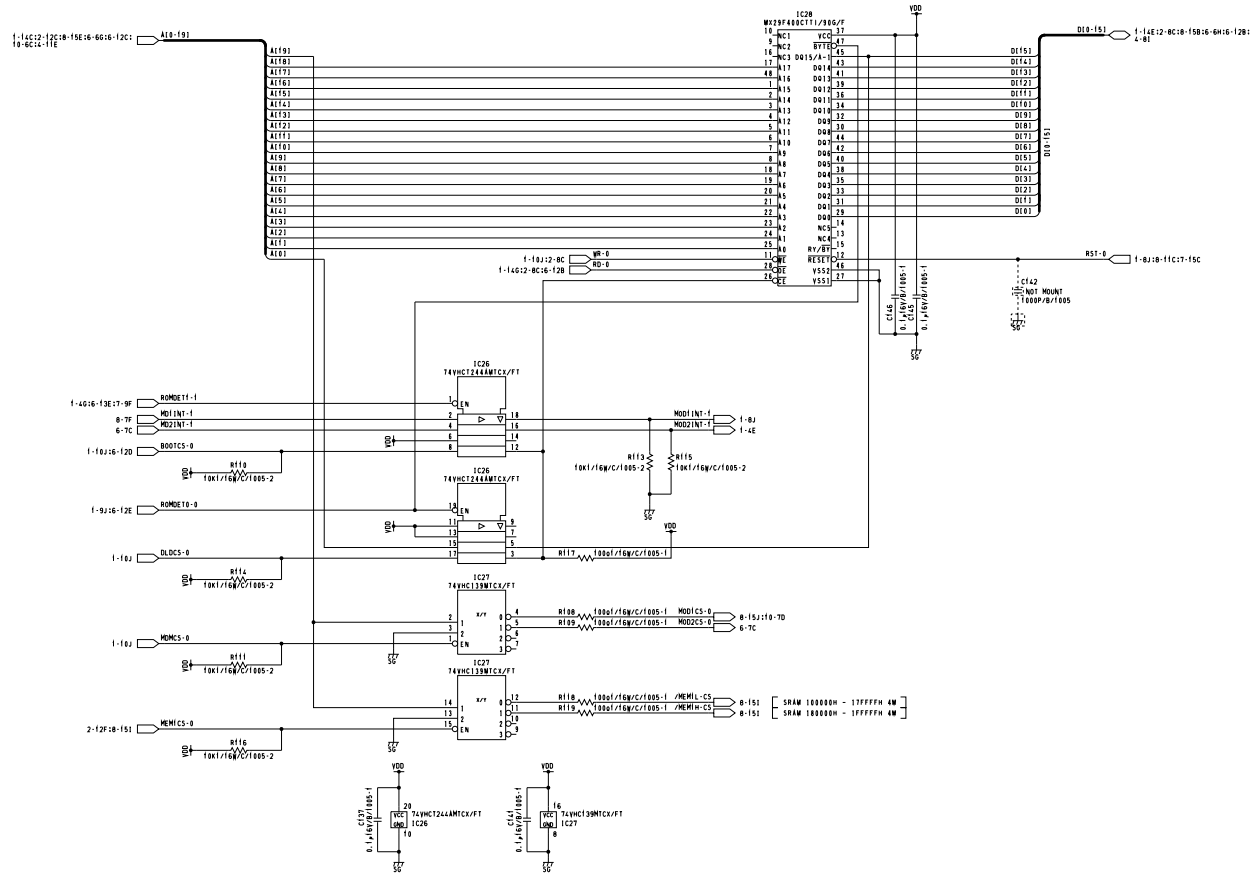
F1	+3.3V	MFA, RST-IC
F2	+5V	RST-IC, +3.3V_OCDC(sensor, MFA, etc)
F3	+24V1	FB motor, clutch, solenoid
F4	+24V2	ADF motor

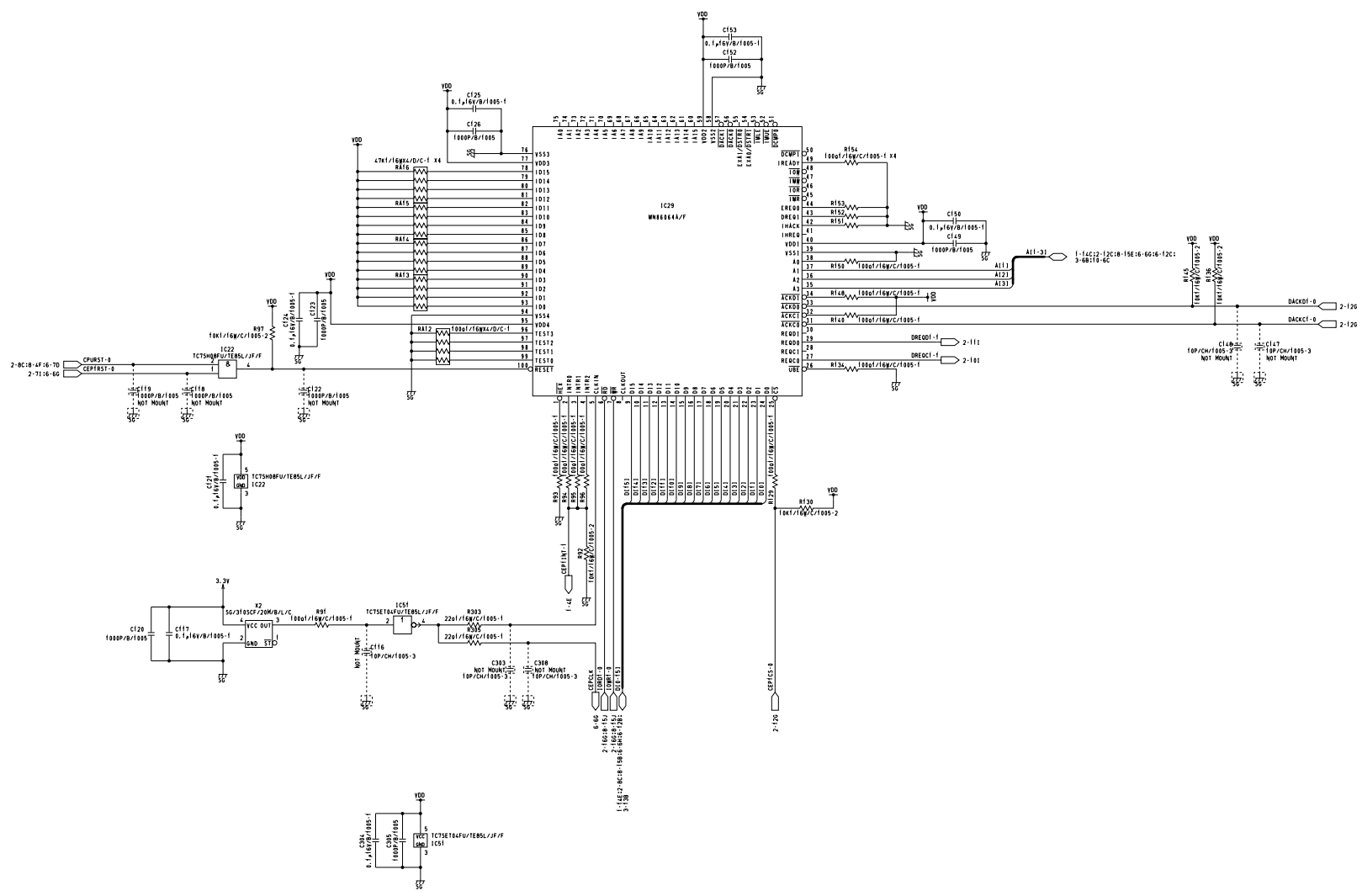
$V_o = 0.8 \cdot (1 + R1/R2)$

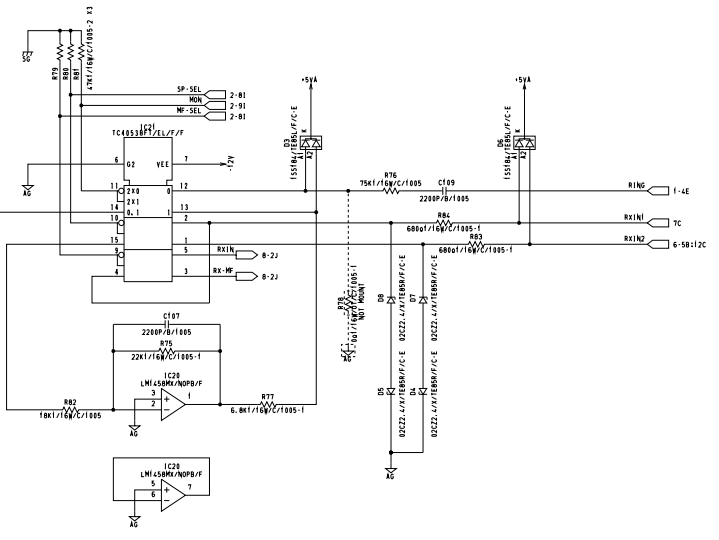
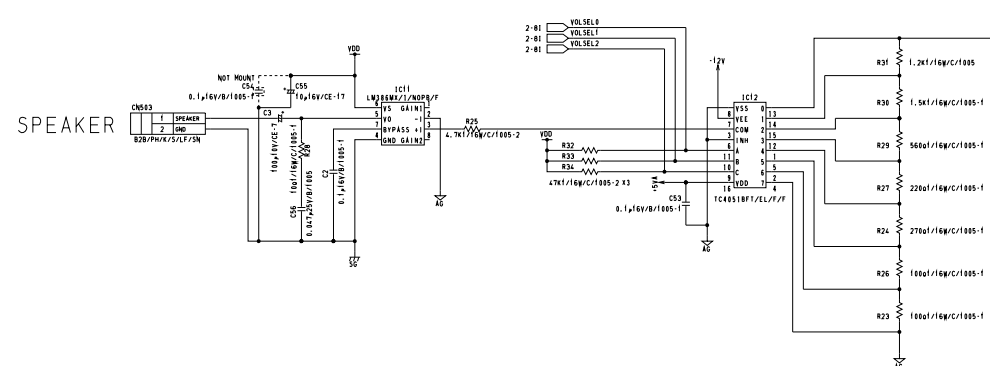
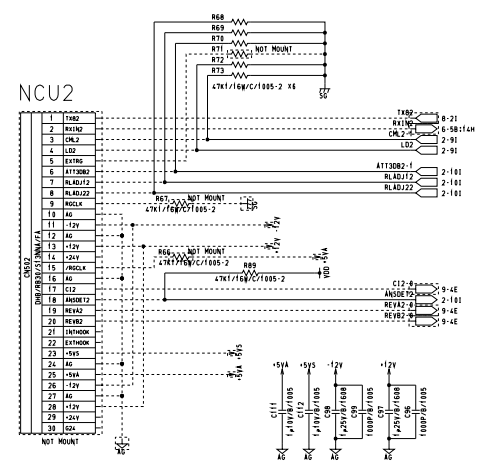
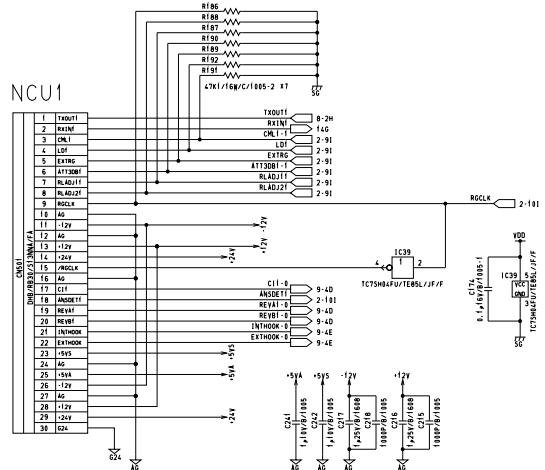
R1	1.2V	1.8V	3.3V
R2	12k	30k	75k
	24k	24k	24k



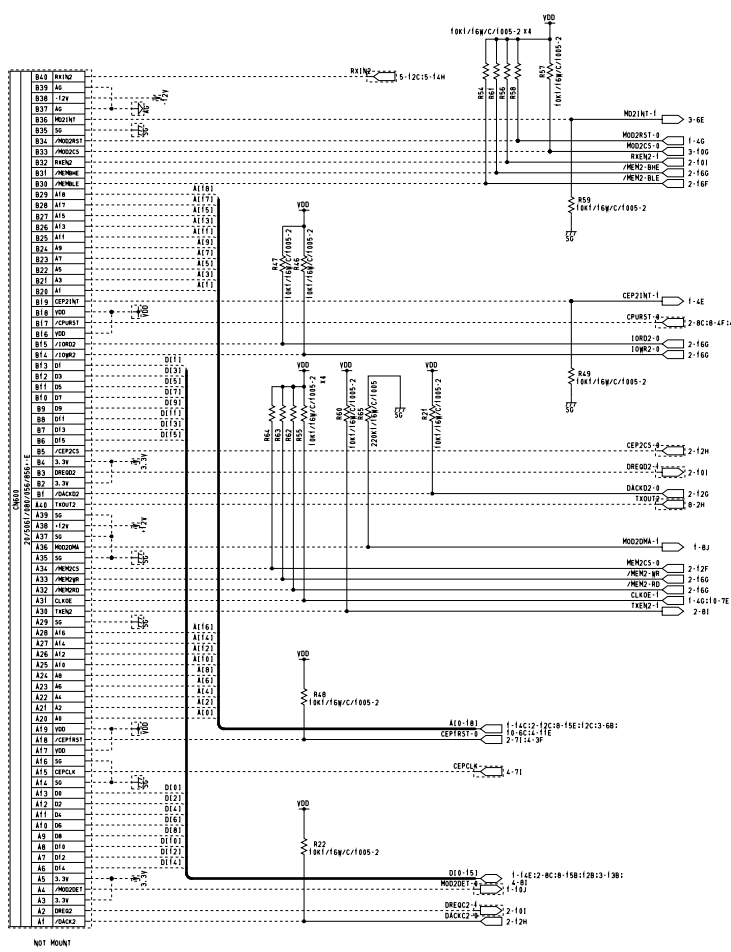




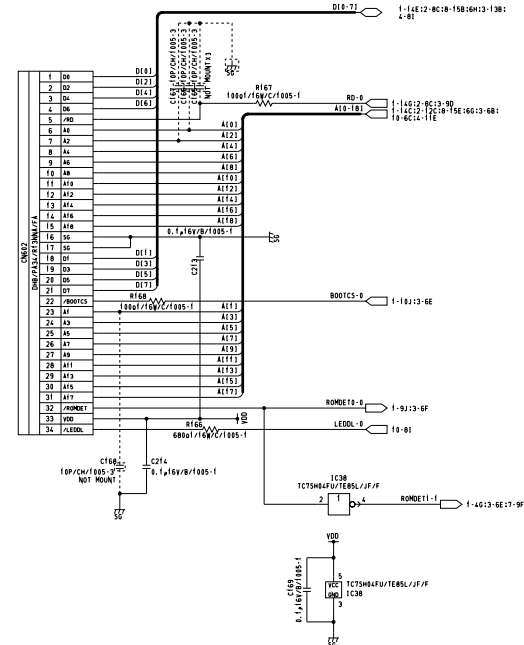




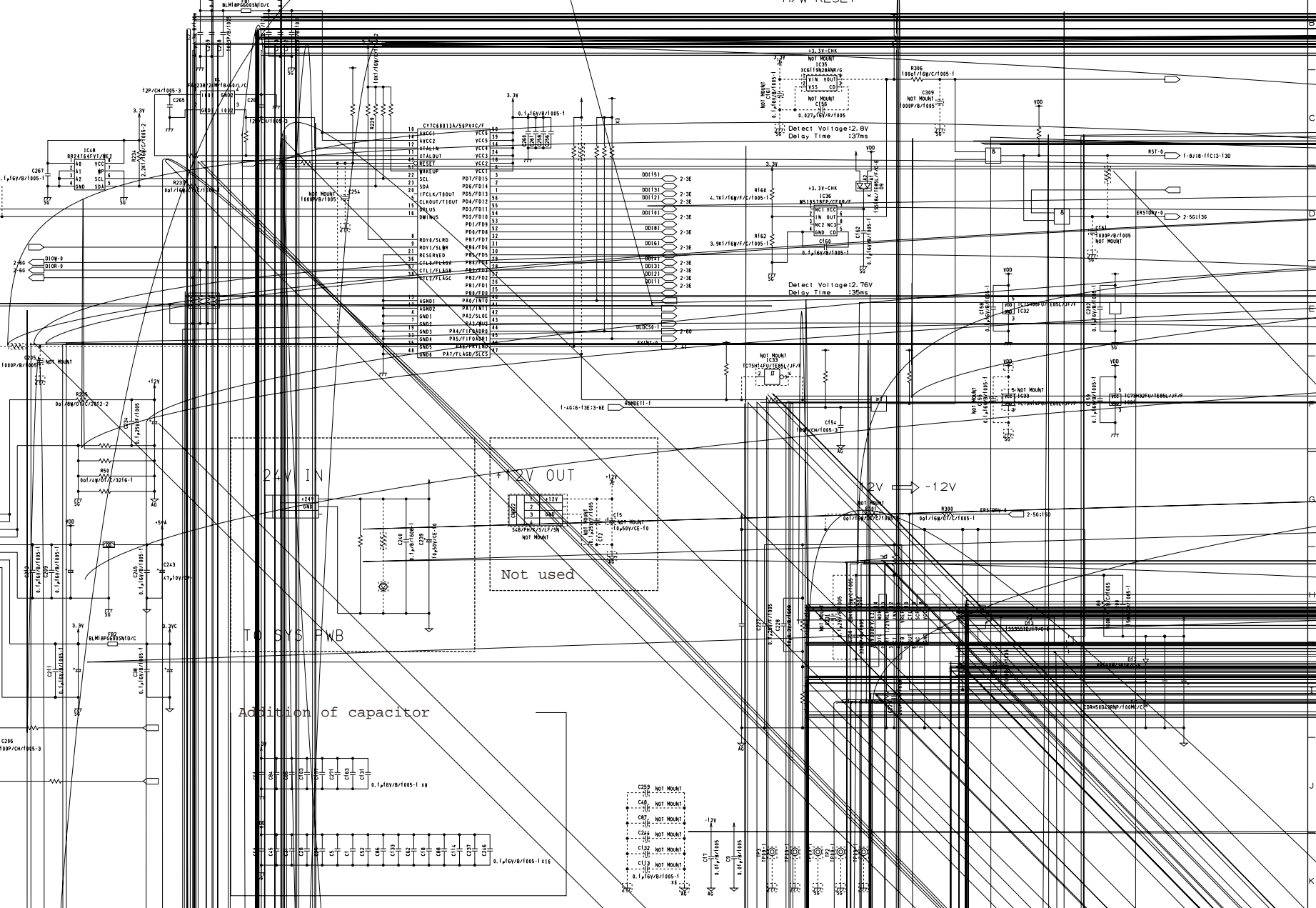
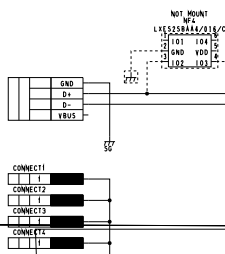
MODEM I/F

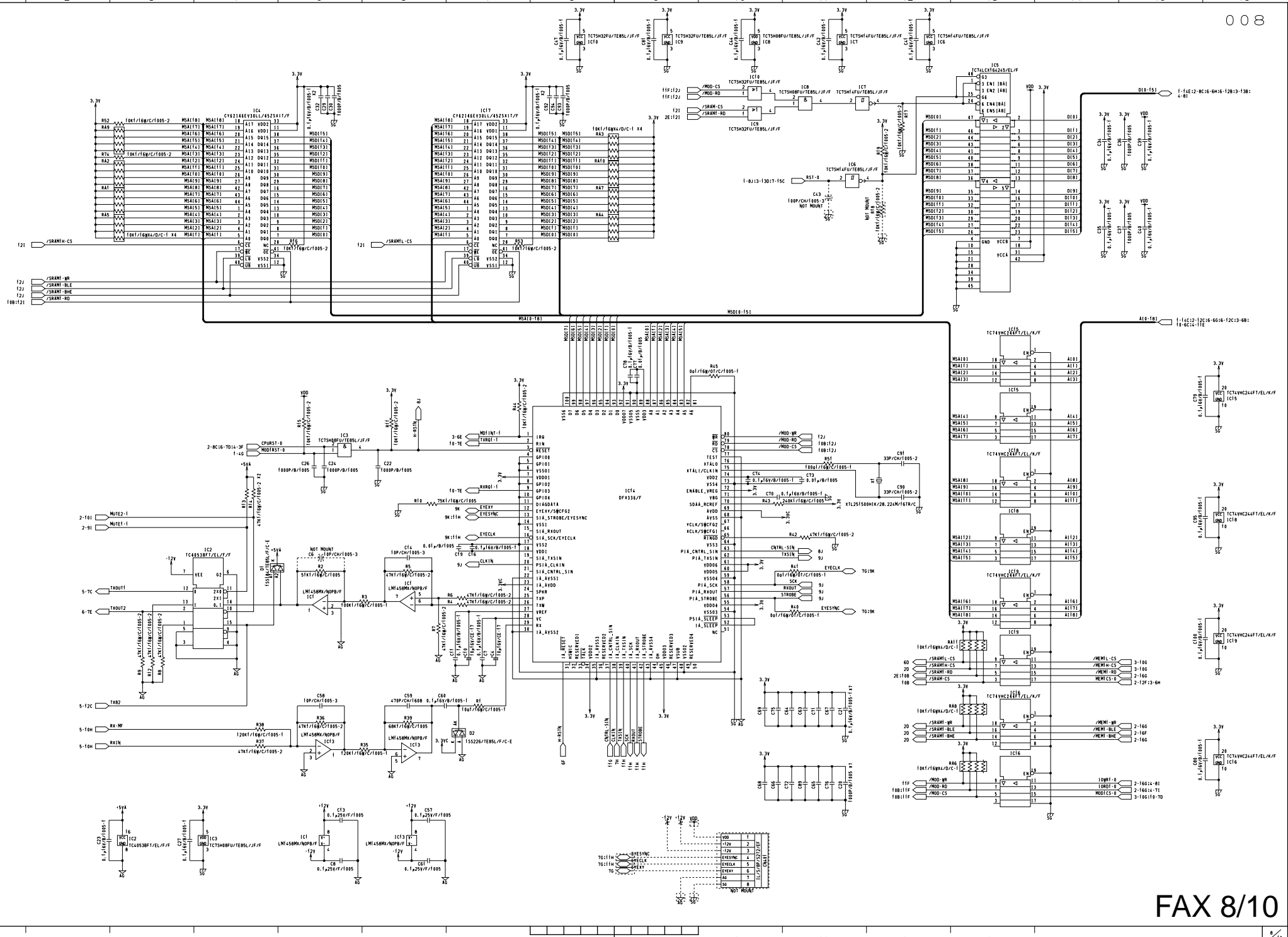


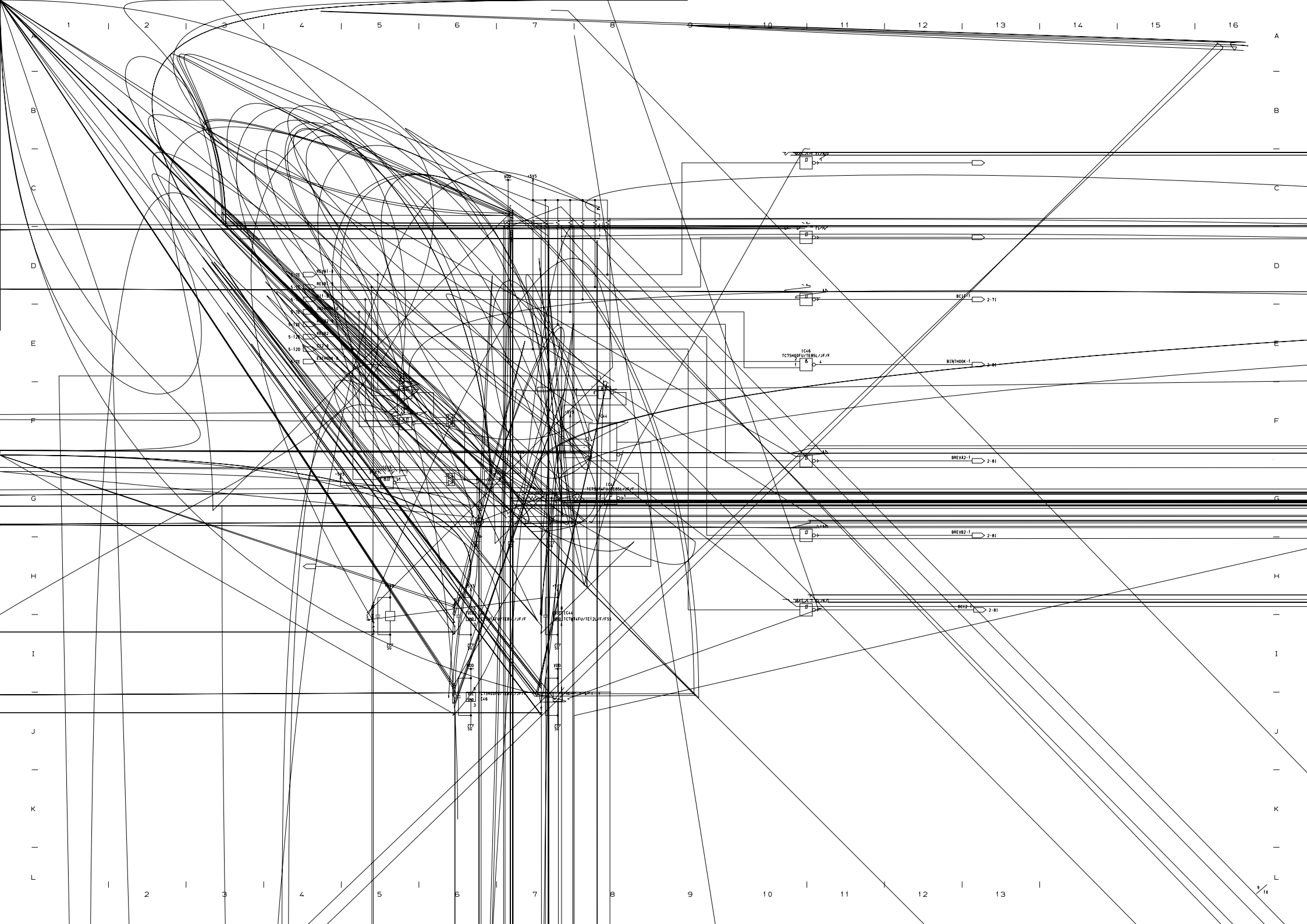
DOWN LOAD

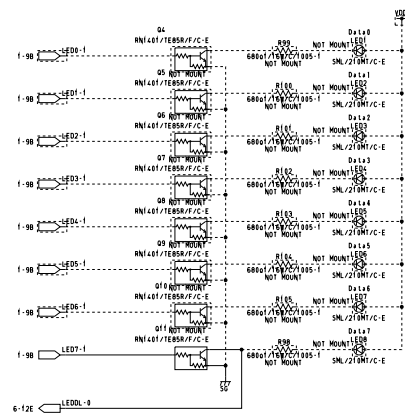
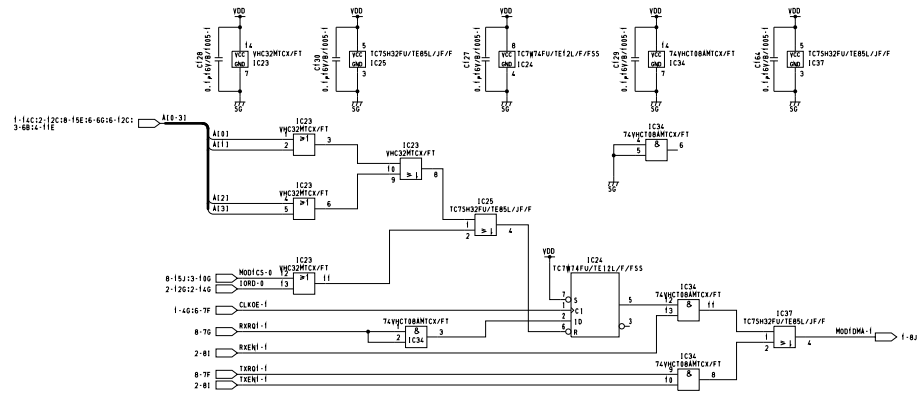


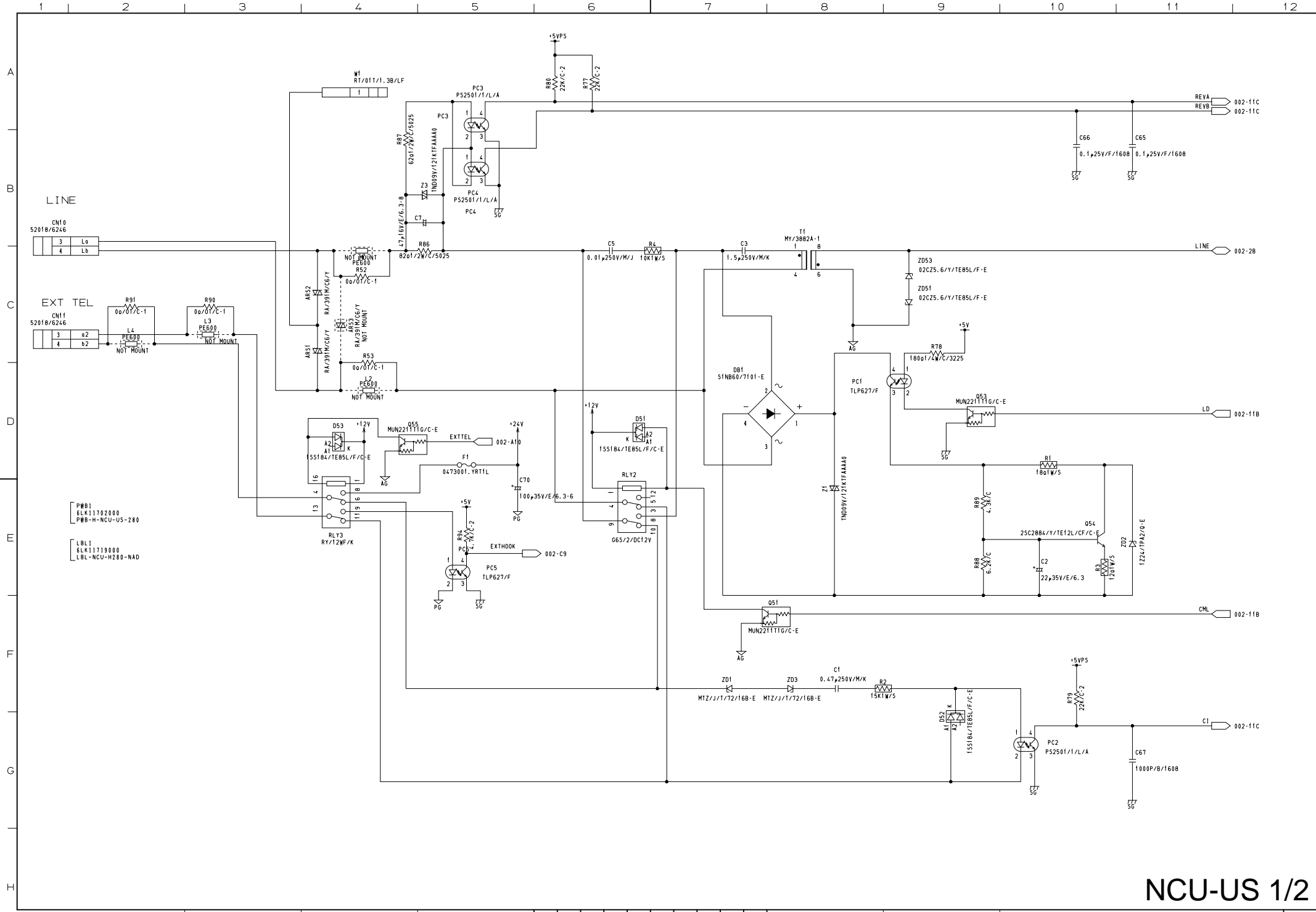
H/W RESET











LINE

CM10
52018/6246

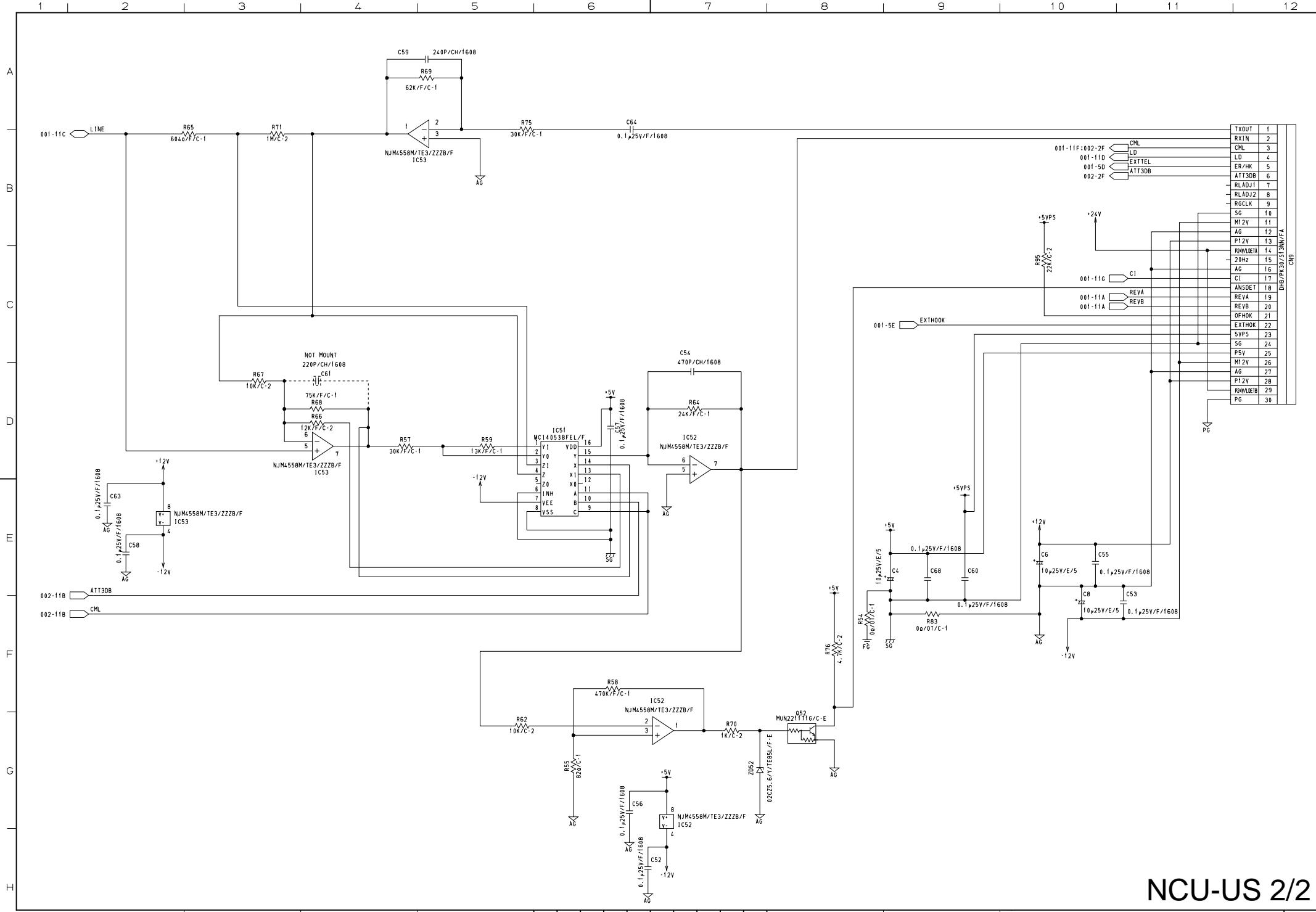
EXT TEL

CM11
52018/6246

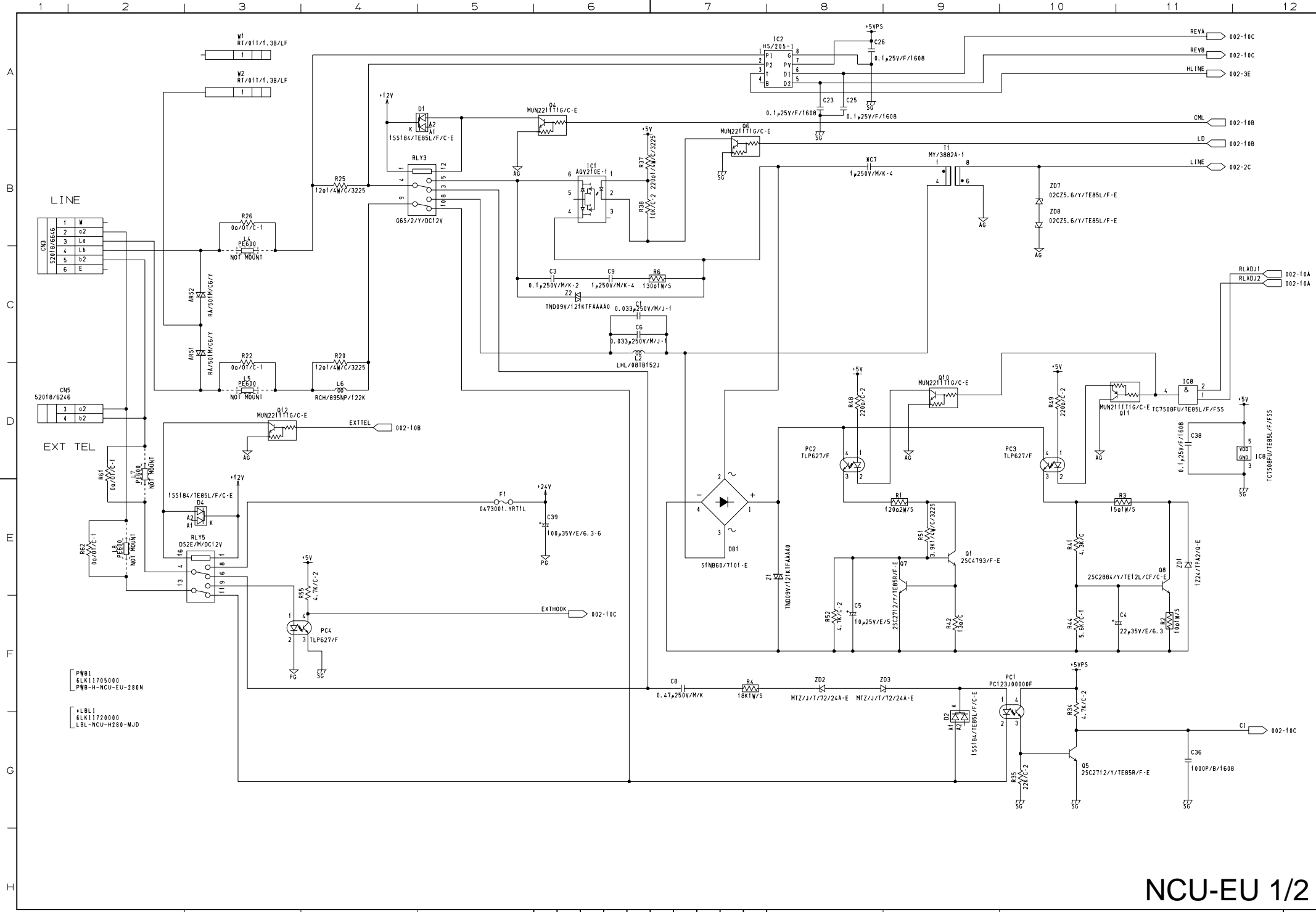
PWB1
6LK11702000
PWB-H-NCU-US-280

LBL1
6LK1119000
LBL-NCU-H280-NAD

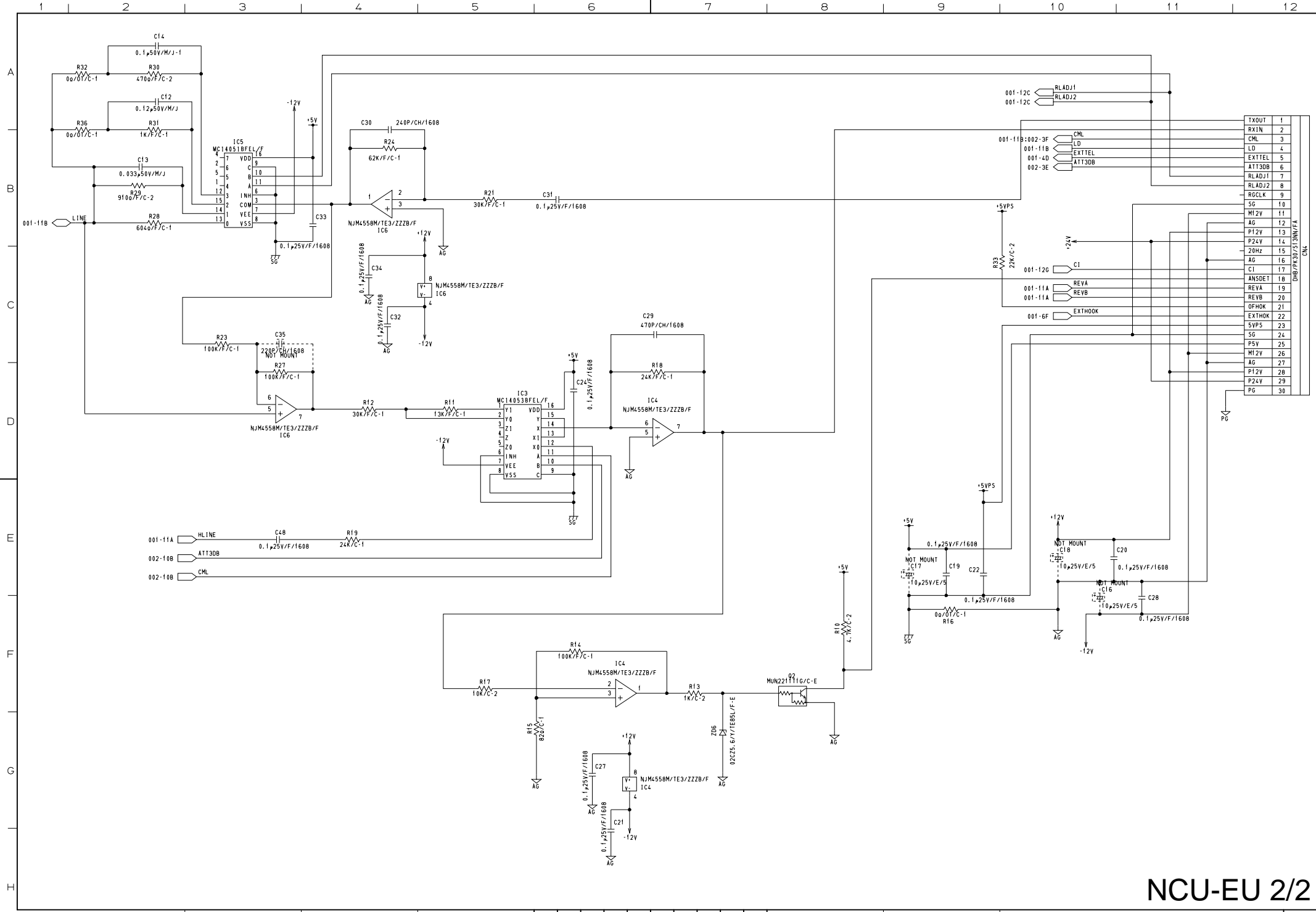
NCU-US 1/2



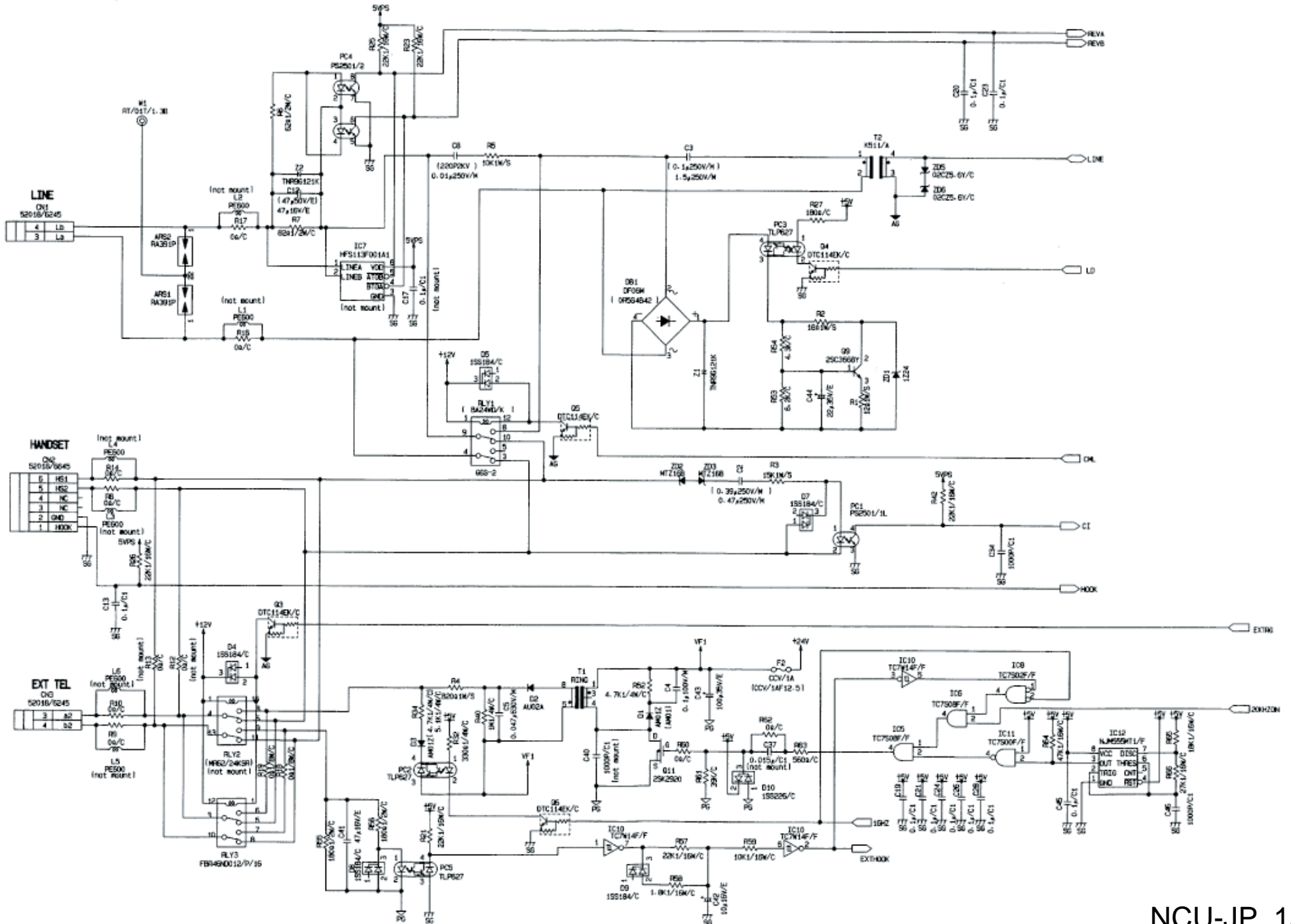
NCU-US 2/2

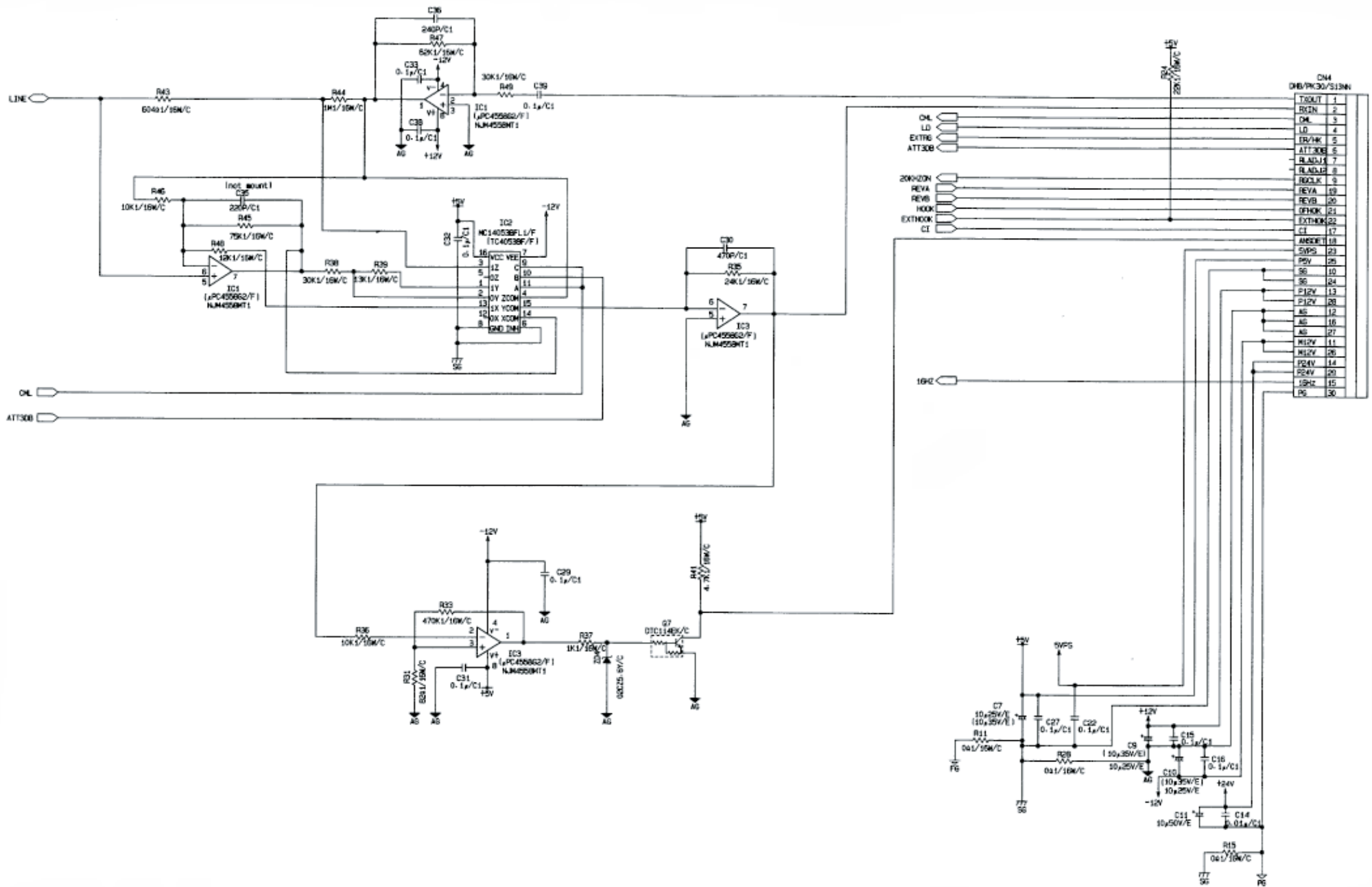


NCU-EU 1/2



TXOUT	1
RXIN	2
CML	3
LD	4
EXTTEL	5
ATT3DB	6
RLADJ1	7
RLADJ2	8
RGCLK	9
SG	10
M12V	11
AG	12
P12V	13
P24V	14
20Hz	15
AG	16
C1	17
ANSDET	18
REVA	19
REVB	20
OFHOK	21
EXTHOK	22
5VPS	23
SG	24
PSY	25
M12V	26
AG	27
P12V	28
P24V	29
PG	30





PU Connector List (Signal functions)

*P: Power supply system signal

No.	Name of Connector	Pin No.	Name of Signal	I/O Type	Connected to	Signal function
		1	GND	P		Logic system ground
		2	CLKP	O		Direct connection head clock output (differential)
		3	CLKN	O		Direct connection head clock output (differential)
		4	GND	P		Logic system ground
		5	LOAD/WPN/HOLDN	O		load output
		6	HSYNCN/CSN	O		hsync output
		7	D13	O		Head data output
		8	D12	O		Head data output
		9	D11	O		Head data output
		10	D10	O		Head data output
		11	D03	O		Head data output
		12	D02	O		Head data output
		13	D01	O		Head data output
		14	D00	O		Head data output
		15	STBN/SI	O		stb output
		16	SCK	O		sck output
		17	SO	I		Head EEPROM read data input
		18	3.3V	P		Head 3.3V output via chip fuse F8
		19	GND	P		Logic system ground
		20	5V	P		Head 5V output via chip fuse F9
		21	GND	P		Logic system ground
		22	5V	P		Head 5V output via chip fuse F9
		23	GND	P		Logic system ground
		24	5V	P		Head 5V output via chip fuse F9
		1	GND	P		Logic system ground
		2	CLKP	O		Direct connection head clock output (differential)
		3	CLKN	O		Direct connection head clock output (differential)
		4	GND	P		Logic system ground
		5	LOAD/WPN/HOLDN	O		load output
		6	HSYNCN/CSN	O		hsync output
		7	D13	O		Head data output
		8	D12	O		Head data output
		9	D11	O		Head data output
		10	D10	O		Head data output
		11	D03	O		Head data output
		12	D02	O		Head data output
		13	D01	O		Head data output
		14	D00	O		Head data output
		15	STBN/SI	O		stb output
		16	SCK	O		sck output
		17	SO	I		Head EEPROM read data input
		18	3.3V	P		Head 3.3V output via chip fuse F8
		19	GND	P		Logic s

No.	Name of Connector	Pin No.	Name of Signal	I/O Type	Connected to	Signal function
3	HEAD2M	1	GND	P	M LED Head	Logic system ground
		2	CLKP	O		Direct connection head clock output (differential)
		3	CLKN	O		Direct connection head clock output (differential)
		4	GND	P		Logic system ground
		5	LOAD/WPN/HOLDN	O		load output
		6	HSYNCN/CSN	O		hsync output
		7	D13	O		Head data output
		8	D12	O		Head data output
		9	D11	O		Head data output
		10	D10	O		Head data output
		11	D03	O		Head data output
		12	D02	O		Head data output
		13	D01	O		Head data output
		14	D00	O		Head data output
		15	STBN/SI	O		stb output
		16	SCK	O		sck output
		17	SO	I		Head EEPROM read data input
		18	3.3V	P		Head 3.3V output via chip fuse F8
		19	GND	P		Logic system ground
		20	5V	P		Head 5V output via chip fuse F9
		21	GND	P		Logic system ground
		22	5V	P		Head 5V output via chip fuse F9
		23	GND	P		Logic system ground
		24	5V	P		Head 5V output via chip fuse F9
4	HEAD3C	1	GND	P	C LED Head	Logic system ground
		2	CLKP	O		Direct connection head clock output (differential)
		3	CLKN	O		Direct connection head clock output (differential)
		4	GND	P		Logic system ground
		5	LOAD/WPN/HOLDN	O		load output
		6	HSYNCN/CSN	O		hsync output
		7	D13	O		Head data output
		8	D12	O		Head data output
		9	D11	O		Head data output
		10	D10	O		Head data output
		11	D03	O		Head data output
		12	D02	O		Head data output
		13	D01	O		Head data output
		14	D00	O		Head data output
		15	STBN/SI	O		stb output
		16	SCK	O		sck output
		17	SO	I		Head EEPROM read data input
		18	3.3V	P		Head 3.3V output via chip fuse F8
		19	GND	P		Logic system ground
		20	5V	P		Head 5V output via chip fuse F9
		21	GND	P		Logic system ground
		22	5V	P		Head 5V output via chip fuse F9
		23	GND	P		Logic system ground
		24	5V	P		Head 5V output via chip fuse F9
5	RFID	1	GND	P	RFID PCB	Logic system ground
		2	RFSCS	I/O		I2C clock input/output
		3	RFSDA	I/O		I2C data input/output
		4	RESET-N	O		Hardware reset output (0: Reset, 1: Not reset)
		5	5VPS	P		5V when OFF at power save
6	IDFAN	1	24V-IDFAN	P	Image Drum FAN	Fan ON output (Off: Open, On: 24V output)
		2	PG	O		Power system ground
		3	FANERR2	I		Error input (0: Normal, 1: Error)
7	STKFL	1	5V	P	Stacker Full Sensor	5V via chip fuse F4
		2	STKFL-N	I		Stack full sensor input (0: Paper exists, 1: No paper)
		3	GND	P		Logic system ground

No.	Name of Connector	Pin No.	Name of Signal	I/O Type	Connected to	Signal function
8	DCIDR	1	24VPS	P	CM_Image Drum Motor	Logic system via chip fuse F5, and 24V when OFF at power save
		2	DMON-N	O		Motor START/STOP output (0: START, 1: STOP)
		3	DMLOCK-P	I		Motor lock input (0: Within the lock area, 1: Out of the lock area)
		4	DMCLK-P	O		Clock output
		5	GAIN-P	O		GAIN switching output (0: Low speed, 1: High speed)
		6	24V	P		Power system 24V
		7	24V	P		Power system 24V
		8	PG	P		Power system ground
		9	PG	P		Power system ground
9	STP	1	24V	P	Offline Stapler (Option)	24V via chip fuse F10
		2	PG	P		Power system ground
		3	STPG-P	I		Stapler good signal (0: No STP or abnormal, 1: STP exists and normal)
		4	GND	P		Logic system ground
		5	STPMOUNT-N	I		Stapler mount status signal (0: Mounted, 1: Not mounted)
10	FIN	1	RXD	I	Finisher Unit (Option)	Data input
		2	GND	P		Logic system ground
		3	TXD	O		Data output
		4	CHK	I		Finisher mount check input signal (0: Mounted, 1: Not mounted)
		5	5V	P		5V via chip fuse F4
		6	PG	P		Power system ground
		7	PG	P		Power system ground
		8	24V	P		Power system 24V
		9	24V	P		Power system 24V
11	ENV	1	3.3V	P	Environment sensor PCB	Logic system 3.3V
		2	GND	P		Logic system ground
		3	GND	P		Logic system ground
		4	ENVHUM	I		Environment humidity sensor
		5	ENVTMP	I		Environment temperature thermistor
		6	HUM_PWM-P	O		Humidity sensor read timing output
12	SSNS	1	TNRM	I	Toner Sensor PCB	Toner sensor M input
		2	TNRY	I		Toner sensor Y input
		3	TNRC	I		Toner sensor C input
		4	TNRK	I		Toner sensor K input
		5	GND	P		Logic system ground
		6	FUSECUT	O		Electricity-removing light ON output (used in common with fuse cut) (0: Normal, 1: Cut)
		7	5VPS	P		5V when OFF at power save
		8	YIDFU	O		YID fuse cut output
		9	MIDFU	O		MID fuse cut output
		10	KIDFU	O		KID fuse cut output
		11	CIDFU	O		CID fuse cut output
13	DCID	1	IDBRAKE-P	P	YK_Image Drum Motor	Logic system 24V via chip fuse F5
		2	START/STOP	O		Motor START/STOP output (0: START, 1: STOP)
		3	IDLOCK-N	I		Motor lock input (0: Within the lock range, 1: Out of the lock range)
		4	IDCLK	O		Clock output
		5	IDHIGAIN-P	O		GAIN switch output (0: Low speed, 1: High speed)
		6	24V	P		Power system 24V
		7	24V	P		Power system 24V
		8	PG	P		Power system ground
		9	PG	P		Power system ground
14	FSNS	1	GND	P	Front Sensor PCB (WR, IN1, IN2)	Logic system ground
		2	PWWR-N	I		Write sensor input (0: Paper exists, 1: No paper)
		3	PAPIN-N	I		IN2 sensor input (0: Paper exists, 1: No paper)
		4	HOP-N	I		IN1 sensor input (hopping) (0: Paper exists, 1: No paper)
		5	5VPS	P		5V when OFF at power save

No.	Name of Connector	Pin No.	Name of Signal	I/O Type	Connected to	Signal function
15	PE_HOP	1	5VPS	P	1st Paper Empty Sensor	5V when OFF at power save
		2	PEND-N	I		Paper end input (0: Paper exists, 1: No paper)
		3	GND	P		Logic system ground
		4	5VPS	P	Hopping Sensor	5V when OFF at power save
		5	HOPOUT-N	I		Hopping sensor input (trailing edge detection) (0: Paper exists, 1: No paper)
		6	GND	P		Logic system ground
16	CL1	1	24V	P	Hopping Clutch	24V via chip fuse F6
		2	CL1	O		ON signal output (0: Off, 1: On)
17	HP_PSZCL	1	HOP1	O	Hopping Motor	Hopping motor 1A output
		2	HOP2	O		Hopping motor 1B output
		3	HOP3	O		Hopping motor 2B output
		4	HOP4	O		Hopping motor 2A output
		5	24V	P	Regist Clutch	24V via chip fuse F7
		6	CL2	O		ON signal output (0: Off, 1: On)
		7	24V	P	MPT Clutch	24V via chip fuse F7
		8	CL3	O		ON signal output (0: Off, 1: On)
		9	PSZ0-P	I	Paper Size SW	Paper size detection bit0 input
		10	PSZ1-P	I		Paper size detection bit1 input
		11	GND	P		Logic system ground
		12	PSZ2-P	I		Paper size detection bit2 input
		13	PSZ3-P	I		Paper size detection bit3 input
18	BELTIDUP	1	IDUP1	O	Image Drum Up Motor	ID Up motor 1A output
		2	IDUP2	O		ID Up motor 1B output
		3	IDUP3	O		ID Up motor 2A output
		4	IDUP4	O		ID Up motor 2B output
		5	BELT1	O	Belt Motor	Belt motor 1A output
		6	BELT2	O		Belt motor 1B output
		7	BELT3	O		Belt motor 2A output
		8	BELT4	O		Belt motor 2B output
19	OPTION	1	OPTPOS_HLD	O	Odd number pins: PFU PCB (Option) Even number pins: Duplex Unit PCB	Tray retention current direction output (0: Enable, 1: Disable)
		2	GND	P		Logic system ground
		3	OPTRXD	I		Option Tray data input
		4	DUPRSD	I		Duplex data input
		5	OPPTXD	O		Option Tray data output
		6	DUPTXD	O		Duplex data output
		7	OPTINT	I		Option Tray status change input (SDR) (0: Changed, 1 No change)
		8	DUPINT	I		Duplex status change input (SDR) (0: Changed, 1 No change)
		9	GND	P		Logic system ground
		10	5V	P		5V via chip fuse F4
		11	24V	P		24V via chip fuse F1
		12	24V	P		24V via chip fuse F1
		13	OPTFDEN	O		Option Tray transfer permission direction output (CONT2) (0: Permitted, 1: Stop)
		14	PG	P		Power system ground
		15	5V	P		5V via chip fuse F4
		16	DUPCNT2-N	O		Duplex flash erase direction output
		17	OPTSTS	I		Option Tray paper position monitoring input (0: L level output, 1: H level output)
		18	HOP-N	O		IN1 sensor output (hopping)
		19	PG	P		Power system ground
		20	PWWR-N	O		Write sensor output
		21	PG	P		Power system ground
		22	GND	P		Logic system ground
		23	24V	P		24V via chip fuse F1
		24	NC	-		Not connected
20	POWFAN	1	24V-POWFAN	P	Low-voltage FAN	Fan ON output (Off: Open, On: 24V output)
		2	PG	O		Power system ground
		3	FANERR1-P	I		Error input (0: Normal, 1: Error)

No.	Name of Connector	Pin No.	Name of Signal	I/O Type	Connected to	Signal function
21	HVOLT	1	GND	P	High Voltage Power Supply Unit PCB	Logic system ground
		2	SCLK1-N	O		High voltage serial clock
		3	GND	P		Logic system ground
		4	SDIN-N	I		High voltage serial data input
		5	RESET-N	O		High voltage CPU reset (0: Reset, 1: Not reset)
		6	SDOUT-P	O		High voltage serial data output
		7	SCLR-N	O		High voltage sequence clear (0: Assert, 1: De-assert)
		8	COVOPN-N	I		Upper cover open monitoring input (0: Close, 1: Open)
		9	5V	P		5V via chip fuse F4
		10	24V	P		24V via chip fuse F5
		11	FANON-P	O		Fan ON output (0: Off, 1: On)
		12	PG	P		Power system ground
		13	NC	-		Not connected
22	RELAY	1	FUSECUT-P	O	Relay PCB	Fuse cut power supply output (0: Normal, 1: Cut)
		2	HEATFU-P	O		Fuser unit fuse cut output (0: Off, 1: On)
		3	BELTFU-P	O		Belt fuse cut output (0: Off, 1: On)
		4	GND	P		Logic system ground
		5	LLEDK	O		LED current value output for left color registration sensor
		6	FLAMETMP-P	I		UPPER roller temperature (for compensation) input
		7	LCREG	I		Color registration correction L
		8	SIDETMP-P	I		SIDE roller temperature input
		9	HEATR-N	I		Exit sensor input (0: Paper exists, 1: No paper)
		10	UPHRTMP-P	I		UPPER roller temperature input
		11	GND	P		Logic system ground
		12	3.3V	I		Logic system 3.3V
		13	KDEN	I		BLACK density correction
		14	LWHRTMP-P	I		LOWER roller temperature input
		15	YMCDEN	I		COLOR density correction
		16	RCREG	I		Color registration R
		17	DENLED	O		LED current value output for the density sensor
		18	RLEDK	O		LED current value output for right color registration
		19	5VPS	P		5V when OFF at power save
		20	TAWAMI	I		Face Up cover open detection input (0: Open, 1: Close)
23	POWER	1	24V	P	Low Voltage Power Supply Unit PCB	24V generated by low-voltage power supply
		2	24V	P		24V generated by low-voltage power supply
		3	24V	P		24V generated by low-voltage power supply
		4	24V	P		24V generated by low-voltage power supply
		5	PG	P		Power system ground
		6	PG	P		Power system ground
		7	PG	P		Power system ground
		8	PG	P		Power system ground
		9	GND	P		Logic system ground
		10	GND	P		Logic system ground
		11	5V	P		5V generated by low-voltage power supply
		12	HARD GUARD	O		Hard guard signal output
		13	5V	P		5V generated by low-voltage power supply
		14	ACONG-N	O		Main heater ON output (0: Off, 1: On)
		15	ACZEROX	I		AC zero-cross signal input
		16	ACON1-N	O		Sub heater ON output (0: Off, 1: On)
		17	POWEROVER	I		Notification signal input of power supply overloading to PU (1: Normal load, 0: Overload)
		18	PULLUP	I		Pull up (5V return)
		19	NC	-		Not connected
		20	NC	-		Not connected

No.	Name of Connector	Pin No.	Name of Signal	I/O Type	Connected to	Signal function
24	DCHEAT	1	HEATBRAKE-P	O	Fuser Motor	ON/OFF (brake) output (0: Release, 1: Brake)
		2	START/STOP	O		START/STOP output (0: START, 1: STOP)
		3	HEATLOCK-N	I		Lock input (0: Within the lock range, 1: Out of the lock range)
		4	HEATCWCCW-N	O		CW/CCW switch output (0: Forward rotation, 1: Reverse rotation)
		5	HEATCLK	O		Clock output
		6	HEATHIGAIN-P	O		GAIN switch output (0: Low speed, 1: High speed)
		7	24V	P		Power system 24V
		8	PG	P		Power system ground
		9	24VPS	P		Logic system via chip fuse F5, and 24V when OFF at power save
25	COIN	1	GND	P	COIN Controller	Logic system ground
		2	KCTRCNT-N	I		Key counter connection signal input
		3	24V	P		24V via chip fuse F3
		4	KCTRON-N	O		Key counter ON signal output
		5	24V	P		24V via chip fuse F3
		6	CTRON-N	O		Total counter ON signal output
		7	CTRCNT-N	I		Copy permission signal
		8	MCRUN-N	O		Copying operation signal output
		9	EXCTR-N	O		Exit sensor ON signal output
		10	PG	P		Power system ground
		11	BKCTR-N	O		Black mode counter signal output
		12	MNCTR-N	O		Mono color mode counter ON signal output
		13	FLCTR-N	O		Full color mode counter ON signal output
		14	GND	P		Logic system ground
		15	SIZE3	O		Paper size output
		16	SIZE2	O		Paper size output
		17	SIZE1	O		Paper size output
		18	SIZE0	O		Paper size output
		19	5V	P		5V via chip fuse F4
		20	CTRCNT2-N	I		Reserved

No.	Name of Connector	Pin No.	Name of Signal	I/O Type	Connected to	Signal function
26	CUIF0	1	GND	P	SYS PCB - 0	Logic system ground
		2	KDATA0	I		K data signal input
		3	KDATA1	I		K data signal input
		4	KDATA2	I		K data signal input
		5	KDATA3	I		K data signal input
		6	GND	P		Logic system ground
		7	KDATA4	I		K data signal input
		8	KDATA5	I		K data signal input
		9	KDATA6	I		K data signal input
		10	KDATA7	I		K data signal input
		11	GND	P		Logic system ground
		12	LSTB	I		Strobe signal input
		13	GND	P		Logic system ground
		14	WCLK	I		Image data transmission CLK input
		15	GND	P		Logic system ground
		16	FSYNCK-N	O		VSYNC-K output
		17	GND	P		Logic system ground
		18	FSYNCC-N	O		VSYNC-C output
		19	GND	P		Logic system ground
		20	FSYNCM-N	O		VSYNC-M output
		21	GND	P		Logic system ground
		22	FSYNCY-N	O		VSYNC-Y output
		23	GND	P		Logic system ground
		24	LSYNC-N	O		HSYNC output
		25	GND	P		Logic system ground
		26	SRDY-N	I		Serial communication_SRDY input (CTS#)
		27	STS	O		Serial communication_STS output (TXD)
		28	CRDY-N	O		Serial communication_CRDY output (RTS#)
		29	CMD	I		Serial communication_CMD input (RXD)
		30	GND	P		Logic system ground
		31	SLEEP_MODE	I		Signal that notifies whether recovery is from SLEEP or power ON (from CU to PU) (0: From SLEEP, 1: Power ON)
		32	LGREN	O		PU communication Ready output (0: Not ready, 1: Ready)
		33	POW_OFF	O		AC OFF detection signal output (1: AC OFF, 0: AC ON)
		34	SYRST	I		Reset input

No.	Name of Connector	Pin No.	Name of Signal	I/O Type	Connected to	Signal function
27	CUIF1	1	NC	-	SYS PCB - 1	Not connected
		2	NC	-		Not connected
		3	DET	-		Not used (Reserved)
		4	GND	P		Logic system ground
		5	YDATA0	I		Y data signal input
		6	YDATA1	I		Y data signal input
		7	YDATA2	I		Y data signal input
		8	YDATA3	I		Y data signal input
		9	GND	P		Logic system ground
		10	YDATA4	I		Y data signal input
		11	YDATA5	I		Y data signal input
		12	YDATA6	I		Y data signal input
		13	YDATA7	I		Y data signal input
		14	GND	P		Logic system ground
		15	MDATA0	I		M data signal input
		16	MDATA1	I		M data signal input
		17	MDATA2	I		M data signal input
		18	MDATA3	I		M data signal input
		19	GND	P		Logic system ground
		20	MDATA4	I		M data signal input
		21	MDATA5	I		M data signal input
		22	MDATA6	I		M data signal input
		23	MDATA7	I		M data signal input
		24	GND	P		Logic system ground
		25	CDATA0	I		C data signal input
		26	CDATA1	I		C data signal input
		27	CDATA2	I		C data signal input
		28	CDATA3	I		C data signal input
		29	GND	P		Logic system ground
		30	CDATA4	I		C data signal input
		31	CDATA5	I		C data signal input
		32	CDATA6	I		C data signal input
		33	CDATA7	I		C data signal input
		34	GND	P		Logic system ground