TOSHIBA

PC BOARD REPAIR MANUAL

MULTIFUNCTIONAL DIGITAL COLOR SYSTEMS

e-STUDIO2500c/3500c/3510c

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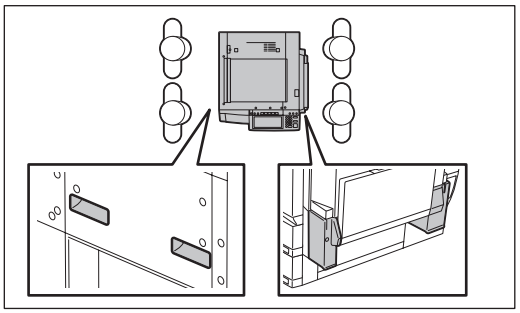
GENERAL PRECAUTIONS REGARDING THE SERVICE FOR e-STUDIO2500c/3500c/3510c

The installation and service should be done by a qualified service technician.

1) **Transportation/Installation**
   - When transporting/installing the equipment, employ four persons and be sure to hold the positions as shown in the figure.
     The equipment is quite heavy and weighs approximately 120 kg (264.55 lb.), therefore pay full attention when handling it.



   - Be sure not to hold the movable parts or units (e.g. the control panel, ADU or RADF) when transporting the equipment.
   - Be sure to use a dedicated outlet with AC 110 V / 13.2 A, 115 V or 127 V / 12 A, 220-240 V / 8 A for its power source.
   - The equipment must be grounded for safety.
   - Select a suitable place for installation. Avoid excessive heat, high humidity, dust, vibration and direct sunlight.
   - Provide proper ventilation since the equipment emits a slight amount of ozone.
   - To insure adequate working space for the copying operation, keep a minimum clearance of 80 cm (32”) on the left, 80 cm (32”) on the right and 10 cm (4”) on the rear.
   - The equipment shall be installed near the socket outlet and shall be accessible.
   - Be sure to fix and plug in the power cable securely after the installation so that no one trips over it.

2) **General Precautions at Service**
   - Be sure to turn the power OFF and unplug the power cable during service (except for the service should be done with the power turned ON).
   - Unplug the power cable and clean the area around the prongs of the plug and socket outlet once a year or more. A fire may occur when dust lies on this area.
   - When the parts are disassembled, reassembly is the reverse of disassembly unless otherwise noted in this manual or other related documents. Be careful not to install small parts such as screws, washers, pins, E-rings, star washers in the wrong places.
   - Basically, the equipment should not be operated with any parts removed or disassembled.
   - The PC board must be stored in an anti-electrostatic bag and handled carefully using a wristband since the ICs on it may be damaged due to static electricity.

     Caution: Before using the wristband, unplug the power cable of the equipment and make sure that there are no charged objects which are not insulated in the vicinity.

- Avoid expose to laser beam during service. This equipment uses a laser diode. Be sure not to expose your eyes to the laser beam. Do not insert reflecting parts or tools such as a screwdriver on the laser beam path. Remove all reflecting metals such as watches, rings, etc. before starting service.
- Be sure not to touch high-temperature sections such as the exposure lamp, fuser unit, damp heater and areas around them.
- Be sure not to touch high-voltage sections such as the chargers, transfer belt, 2nd transfer roller, developer, high-voltage transformer, exposure lamp control inverter, inverter for the LCD back-light and power supply unit. Especially, the board of these components should not be touched since the electric charge may remain in the capacitors, etc. on them even after the power is turned OFF.
- Make sure that the equipment will not operate before touching potentially dangerous places (e.g. rotating/operating sections such as gears, belts pulleys, fans and laser beam exit of the laser optical unit).
- Be careful when removing the covers since there might be the parts with very sharp edges underneath.
- When servicing the equipment with the power turned ON, be sure not to touch live sections and rotating/operating sections. Avoid exposing your eyes to laser beam.
- Use designated jigs and tools.
- Use recommended measuring instruments or equivalents.
- Return the equipment to the original state and check the operation when the service is finished.
- Be very careful to treat the touch panel gently and never hit it. Breaking the surface could cause malfunctions.

3) **Important Service Parts for Safety**
   - The breaker, door switch, fuse, thermostat, thermofuse, thermistor, batteries, IC-RAMs including lithium batteries, etc. are particularly important for safety. Be sure to handle/install them properly. If these parts are short-circuited and their functions become ineffective, they may result in fatal accidents such as burnout. Do not allow a short-circuit or do not use the parts not recommended by Toshiba TEC Corporation.

4) **Cautionary Labels**
   - During servicing, be sure to check the rating plate and cautionary labels such as “Unplug the power cable during service”, “CAUTION. HOT”, “CAUTION. HIGH VOLTAGE”, “CAUTION. LASER BEAM”, etc. to see if there is any dirt on their surface and if they are properly stuck to the equipment.

5) **Disposal of the Equipment, Supplies, Packing Materials, Used Batteries and IC-RAMs**
   - Regarding the recovery and disposal of the equipment, supplies, packing materials, used batteries and IC-RAMs including lithium batteries, follow the relevant local regulations or rules.

6) **When the option has been installed:**
   When the EFI printer board has been installed, be sure to unplug the power cable before performing maintenance and inspection, otherwise troubles such as a communication error may occur.

Caution:
Dispose of used batteries and IC-RAMs including lithium batteries according to this manual.
Attention:
Se débarrasser de batteries et IC-RAMs usés y compris les batteries en lithium selon ce manuel.
Vorsicht:
Entsorgung der gebrauchten Batterien und IC-RAMs (inclusive der Lithium-Batterie) nach diesem Handbuch.

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1. SYSTEM BLOCK DIAGRAM

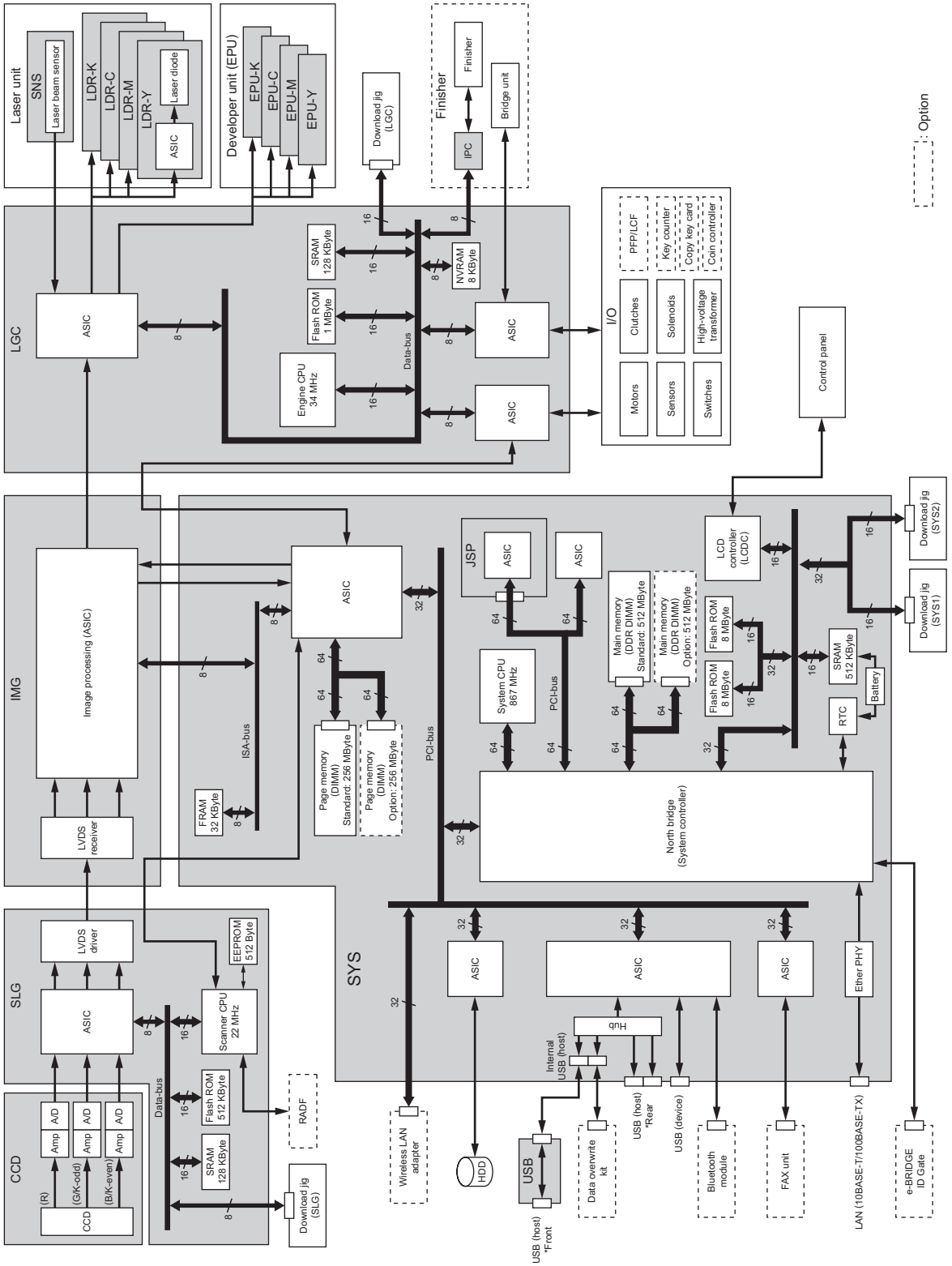

Fig. 1-1

2. GENERAL DESCRIPTION OF MAIN IC

2.1 Scanner CPU (TMP95C063FE)

2.1.1 Outline and features

The TMP95C063FE is developed as a high-speed, advanced 16-bit microcontroller for a range of mid to large-scale equipment.
This device is presented in a 144-pin plastic mini flat package. Its features are as follows.

1) Original high-speed 16-bit CPU (900H_CPU)
   - Instruction mnemonics upwardly compatible with TLCS-90/900
   - 16-Mbyte linear address space
   - General-purpose registers using register bank system
   - 16-bit multiplication/division instructions, bit transfer/arithmetic instructions
   - Micro DMA: 4 channels (640 ns/2 bytes at 25 MHz)
2) Minimum instruction execution time: 160 ns (at 25 MHz)
3) Internal RAM: No
   Internal ROM: No
4) External memory expansion
   - Expandable up to 16 Mbytes (common to programs and data)
   - External data bus width selection pin (AM8/$\overline{16}$)
   - Can use both 8- and 16-bit external buses
     ... Dynamic data bus sizing
5) Internal DRAM controller: 2 channels
   - 2$\overline{CAS}$/2$\overline{WE}$ selectable
6) 8-bit timer: 8 channels
7) 16-bit timer: 2 channels
8) Pattern generator: 4 bits, 2 channels
9) General-purpose serial interface: 2 channels
   - Baud rate generated by external clock
10) 10-bit A/D converter: 8 channels
11) 8-bit D/A converter: 2 channels
12) Watchdog timer
13) Chip selector, wait controller: 4 blocks
14) Interrupt function:
   - CPU interrupts: 2 (software interrupt instructions, illegal instructions)
   - Internal interrupts: 22 (7 priority levels available)
   - External interrupts: 11 (7 priority levels available)
15) Input/output ports
   - 91 pins
16) Standby function
   - 3 HALT modes (RUN, IDLE, STOP)

2.1.2 Functions

The Scanner CPU interfaces with the ASIC on the SYS board and RADF, and controls the whole system of the scanning section such as the scan motor, APS sensor, exposure lamp and such. The Scanner CPU also sets the parameter of each image processing ASIC. These control programs of the Scanner CPU are stored in the Flash ROM on the SLG board. These programs can be updated by downloading the new programs with the download jig, PC which is serially connected and so on.

2.1.3 Pin assignment

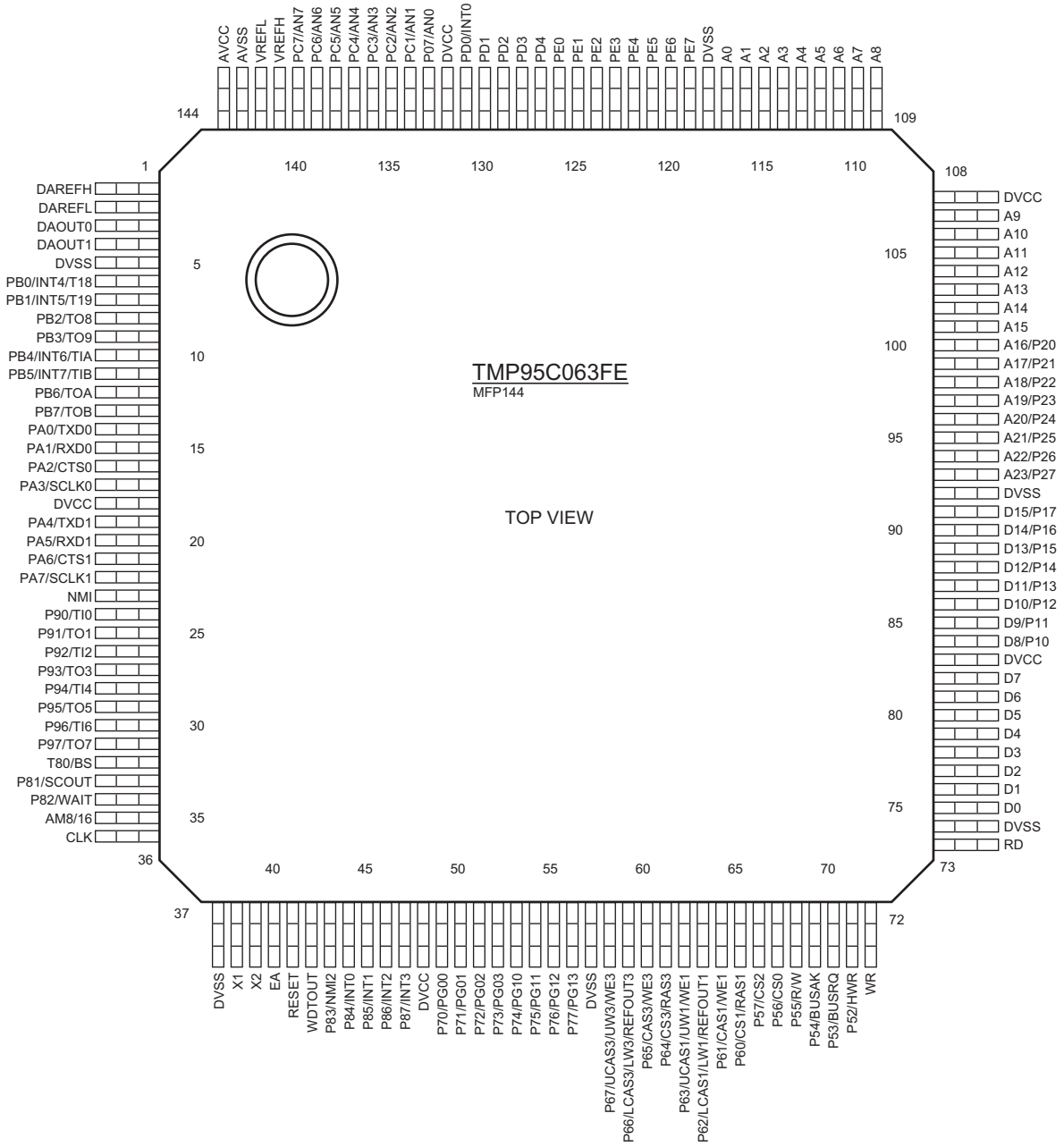

Fig. 2-1

2.1.4 Signals

Pin No.	Port name	Signal name	I/O	Function
1	DAREFH	DAREFH	I	Reference voltage (H) for D/A converter (+5.1VB)
2	DAREFL	DAREFL	I	Reference voltage (L) for D/A converter (Signal ground)
3	DAOUT0	MOTREF-0	O	Reference voltage for scan motor
4	DAOUT1	-	-	Not used (Open)
5	DVSS1	SG	-	Signal ground
6	PB0/INT4/TI8	DFSCST-0	I	RADF scanning start signal
7	PB1/INT5/TI9	-	-	Not used (Open)
8	PB2/TO8	DFRAK-0	I	RADF acknowledge signal: SLG board <- RADF
9	PB3/TO9	EEMCLK-1	O	EEPROM clock
10	PB4/INT6/TIA	DFRRQ-0	I	RADF request signal: SLG board <- RADF
11	PB5/INT7/TIB	-	-	Not used (Open)
12	PB6/TOA	PNCNT-0	I	Debug panel connection signal (L: connected) (for debug)
13	PB7/TOB	SSW-0	I	Debug panel SW status signal (for debug)
14	PA0/TXD0	STXDA-1	O	Transmission data: SLG board -> SYS board
15	PA1/RXD0	SRXD-1A	I	Reception data: SLG board <- SYS board
16	PA2/$\overline{\text{CTS0}}$	SCTS-0A	I	Scanner reception ready signal: SLG board <- SYS board
17	PA3/SCLK0	SRTS-0	O	Scanner transmission ready signal: SLG board -> SYS board
18	DVCC1	+5.1VB	-	+5.1VB
19	PA4/TXD1	DFTXD-0	O	Transmission data: SLG board -> RADF
20	PA5/RXD1	DFRXD-0	I	Reception data: SLG board <- RADF
21	PA6/$\overline{\text{CTS1}}$	DFAK-0	O	Acknowledge signal: SLG board -> RADF
22	PA7/SCLK1	DFRQ-0	O	Request signal: SLG board -> RADF
23	$\overline{\text{NMI}}$	/NMI	I	Non-maskable interrupt signal (Pull-up: +5V)
24	P90/TI0	EEMCS-1	O	EEPROM chip select signal
25	P91/TO1	MOTCLK-0	O	Scan motor reference clock
26	P92/TI2	CHKSAMOK-1	O	Checksum status signal (H: OK, L: NG)
27	P93/TO3	LED-0	O	Download jig LED drive signal
28	P94/TI4	EEMDTIN-1	I	EEPROM read data
29	P95/TO5	EEMDTOUT-1	O	EEPROM write data
30	P96/TI6	-	-	Not used (Open)
31	P97/TO7	-	-	Not used (Open)
32	P80/BS	-	-	Not used (Open)

Pin No.	Port name	Signal name	I/O	Function
33	P81/SCOUT	-	-	Not used (Open)
34	P82/$\overline{WAIT}$	VSYNC-0	I	Secondary scanning synchronizing signal: SLG board <- SYS board
35	AM8/$\overline{16}$	WORD-0	I	Bus width selection signal (H: 8-bit fixed, L: 8/16-bit coexisting)
36	CLK	-	-	Not used (Open)
37	DVSS2	SG	-	Signal ground
38	X1	X1	I	Clock input (22MHz)
39	X2	X2	O	Clock output (22MHz)
40	$\overline{EA}$	/EA	I	Pull-down: signal ground
41	$\overline{RESET}$	MRST	I	Reset signal (Low-active)
42	$\overline{WDTOUT}$	WDTOUT	O	Watchdog output signal (H: CPU is normal, L: CPU is out of control)
43	P83/$\overline{NMI2}$	-	-	Not used (Open)
44	P84/INT0	-	-	Not used (Open)
45	P85/INT1	-	-	-
46	P86/INT2	VSYNC-0	I	Secondary scanning synchronizing signal: SLG board <- SYS board
47	P87/INT3	-	-	Not used (Open)
48	DVCC2	+5.1VB	-	+5.1VB
49	P70/PG00	LED0	O	Debug signal [0]
50	P71/PG01	LED1	O	Debug signal [1]
51	P72/PG02	LED2	O	Debug signal [2]
52	P73/PG03	LED3	O	Debug signal [3]
53	P74/PG10	LED4	O	Debug signal [4]
54	P75/PG11	LED5	O	Debug signal [5]
55	P76/PG12	LED6	O	Debug signal [6]
56	P77/PG13	LED7	O	Debug signal [7]
57	DVSS3	SG	-	Signal ground
58	P67/$\overline{UCAS3}$/$\overline{UW3}$/ $\overline{WE3}$	-	-	Not used (Open)
59	P66/$\overline{LCAS3}$/$\overline{LW3}$/ $\overline{REFOUT3}$	FANONF-0	O	Scanner unit cooling fan ON/OFF signal
60	P65/$\overline{CAS3}$/$\overline{WE3}$	FCNGF1-0	O	Scanner unit cooling fan speed switching signal FCNGF1-0 FANONF-0 Status L L High speed drive L H High speed drive H L Low speed drive H H Stop

Pin No.	Port name	Signal name	I/O	Function
61	P64/$\overline{CS3}$/$\overline{RAS3}$	CS3-0	O	Chip select signal [3] (Low-active) * For Flash ROM (When a PC is being down-loaded)
62	P63/$\overline{UCAS}$/$\overline{UW1}$/$\overline{WE}$	-	-	Not used (Open)
63	P62/$\overline{LCAS}$/$\overline{LW1}$/REFOUT1	LMPON-0	O	Exposure lamp ON signal (L: ON)
64	$\overline{P61}$/$\overline{CAS1}$/$\overline{WE1}$	CCDPSOFF-0	O	CCD power supply control signal (H: supply, L: cutoff)
65	$\overline{P60}$/$\overline{CS1}$/$\overline{RAS1}$	CS1-0	O	Chip select signal [1] (Low-active) * For SRAM
66	P57/$\overline{CS2}$	CS2-0	O	Chip select signal [2] (Low-active) * For Flash ROM
67	P56/$\overline{CS0}$	CS0-0	O	Chip select signal [0] (Low-active) * For ASIC
68	P55/R/$\overline{W}$	GAWR-0	O	ASIC data bus input/output switching signal (H: input, L: output)
69	P54/$\overline{BUSAK}$	LMPEN-0	I	Exposure lamp enable signal (Low-active)
70	P53/$\overline{BUSRQ}$	-	-	Not used (Open)
71	P52/$\overline{HWR}$	SYSCNT-0A	I	SYS board connection signal (L: connected)
72	$\overline{WR}$	MWR-0A	O	Write signal (Low-active)
73	$\overline{RD}$	MRD-0A	O	Read signal (Low-active)
74	DVSS4	SG	-	Signal ground
75	D0	MDT[0]	I/O	Data bus [0]
76	D1	MDT[1]	I/O	Data bus [1]
77	D2	MDT[2]	I/O	Data bus [2]
78	D3	MDT[3]	I/O	Data bus [3]
79	D4	MDT[4]	I/O	Data bus [4]
80	D5	MDT[5]	I/O	Data bus [5]
81	D6	MDT[6]	I/O	Data bus [6]
82	D7	MDT[7]	I/O	Data bus [7]
83	DVCC3	+5.1VB	-	+5.1VB
84	D8/P10	MDT[8]	I/O	Data bus [8]
85	D9/P11	MDT[9]	I/O	Data bus [9]
86	D10/P12	MDT[10]	I/O	Data bus [10]
87	D11/P13	MDT[11]	I/O	Data bus [11]
88	D12/P14	MDT[12]	I/O	Data bus [12]
89	D13/P15	MDT[13]	I/O	Data bus [13]
90	D14/P16	MDT[14]	I/O	Data bus [14]

Pin No.	Port name	Signal name	I/O	Function
91	D15/P17	MDT[15]	I/O	Data bus [15]
92	DVSS5	SG	-	Signal ground
93	A23/P27	DWNLD-0	O	PC download enable signal (Low-active)
94	A22/P26	5VSWON-0	O	+5VSW power supply signal (Low-active)
95	A21/P25	PNGT-0	O	Debug panel control signals ON/OFF signal (for debug)
96	A20/P24	-	-	-
97	A19/P23	SLEEP-1	O	ASIC sleep mode control signal (H: sleep mode)
98	A18/P22	MAD[18]	O	Address bus [18]
99	A17/P21	MAD[17]	O	Address bus [17]
100	A16/P20	MAD[16]	O	Address bus [16]
101	A15	MAD[15]	O	Address bus [15]
102	A14	MAD[14]	O	Address bus [14]
103	A13	MAD[13]	O	Address bus [13]
104	A12	MAD[12]	O	Address bus [12]
105	A11	MAD[11]	O	Address bus [11]
106	A10	MAD[10]	O	Address bus [10]
107	A9	MAD[9]	O	Address bus [9]
108	DVCC4	+5.1VB	-	+5.1VB
109	A8	MAD[8]	O	Address bus [8]
110	A7	MAD[7]	O	Address bus [7]
111	A6	MAD[6]	O	Address bus [6]
112	A5	MAD[5]	O	Address bus [5]
113	A4	MAD[4]	O	Address bus [4]
114	A3	MAD[3]	O	Address bus [3]
115	A2	MAD[2]	O	Address bus [2]
116	A1	MAD[1]	O	Address bus [1]
117	A0	MAD[0]	O	Address bus [0]
118	DVSS6	SG	-	Signal ground
119	PE7	-	-	Not used (Open)
120	PE6	APSON	O	APS sensor power supply control signal (H: supply, L: cutoff)
121	PE5	-	-	Not used (Open)
122	PE4	MOTMD3-0	O	Scan motor control data [3]
123	PE3	MOTMD2-0	O	Scan motor control data [2]
124	PE2	MOTMD1-0	O	Scan motor control data [1]

Pin No.	Port name	Signal name	I/O	Function
125	PE1	MOTDIR-0	O	Scan motor rotational direction switch signal (H: CW, L: CCW)
126	PE0	MOTEN-1	O	Scan motor hold ON/OFF signal (H: ON, L: OFF)
127	PD4	ROMDT-0	I	Download jig connection signal (L: connected)
128	PD3	DFCNT-0	I	RADF connection signal (L: connected)
129	PD2	APS3-0	I	APS-3 sensor detection signal (Low-active)
130	PD1	APS2-0	I	APS-2 sensor detection signal (Low-active)
131	PD0/INT8	APS1-0	I	APS-1 sensor detection signal (Low-active)
132	DVCC5	+5.1VB	-	+5.1VB
133	PC0/AN0	-	-	Signal ground
134	PC1/AN1	-	-	Not used (Open)
135	PC2/AN2	+24CHK	I	+24V voltage check
136	PC3/AN3	-	-	Signal ground
137	PC4/AN4	HOME-1	I	Carriage home position sensor detection signal (H: home position)
138	PC5/AN5	PLTN-1	I	Platen sensor detection signal (H: closed L: open)
139	PC6/AN6	APSC-0	I	APS-C sensor detection signal (Low-active)
140	PC7/AN7	APSR-0	I	APS-R sensor detection signal (Low-active)
141	VREFH	VREFH	I	Reference voltage (H) for A/D converter (+5.1VB)
142	VREFL	VREFL	I	Reference voltage (L) for A/D converter (Signal ground)
143	AVSS	AVSS	I	A/D converter ground (Signal ground)
144	AVCC	AVCC	I	A/D converter power supply (+5.1VB)

2.2 Engine CPU (TMP97CM27FG)

2.2.1 Outline and features

TMP92CM27FG is high-speed advanced 32-bit micro-controller developed for controlling equipment which processes mass data.
This device is presented in a 144-pin plastic flat package. Its features are as follows.

1) CPU : 32-bit CPU (TLCS-900/H1 CPU)
   - Compatible with TLCS-900/L1 instruction code
   - 16Mbytes of linear address space
   - General-purpose register and register banks
   - Micro DMA : 8channels (250ns/4bytes at fc = 40MHz, best case)
2) Minimum instruction execution time : 50ns (at fc=40MHz)
3) Internal memory
   - Internal RAM : 32K-byte (32-bit 1 clock access and program execution are possible)
   - Internal ROM : None
4) External memory expansion
   - Expandable up to 16M bytes (shared program/data area)
   - Can simultaneously support 8/16-bit width external data bus ... Dynamic data bus sizing
   - Separate bus system
5) Memory controller
   - Chip select output : 6 channels
6) 8-bit timers : 8 channels
7) 16-bit timers : 6 channels
8) Pattern generator : 2 channels
9) General-purpose serial interface : 4 channels
   - UART/Synchronous mode : 4 channels (ch.0 to ch.3)
   - IrDA Ver.1.0(115kbps) mode selectable : 1 channels (ch.0)
10) Serial bus interface : 2 channels
   - I2C bus mode/clock synchronous mode selectable
11) High Speed serial interface : 2 channels
12) SDRAM controller : 1 channels
   - Supported 16M, 64M-bit SDR (Single Data Rate)-SDRAM
   - Supported not only operate as RAM and Data for LCD display but also programming directly from SDRAM
13) 10-bit AD converter : 12 channels
14) 8-bit DA converter : 2 channels
15) Watchdog timer
16) Key-on wake up (only for HALT release) : 8 channels
17) Interrupts : 71 interrupts
   - 9 CPU interrupts : Software interrupt instruction and illegal instruction
   - 49 internal interrupts : Seven selectable priority levels
   - 13 external interrupts(INT0 to INTB,$\overline{\text{NMI}}$) : Seven selectable priority levels (INT0 to INTB)
     (INT0 to INTB are selectable edge or level interrupt)
18) External bus release function
19) Input/output ports : 83 pins
20) Stand-by function
   - Three Halt modes : Idle2 (programmable), Idle1, Stop
21) Clock controller
   - Clock doubler (PLL) : fc = fOSCH×4 (fc=40MHz @ fOSCH=10MHz)
   - Clock gear function : Select a High-frequency clock fc to fc/16
22) Operating voltage
   - VCC = 3.0 V to 3.6 V (fc max = 40MHz)

2.2.2 Functions

The Engine-CPU has an interface with each ASIC on the LGC board. It controls the overall printer engine section. Programs for the Engine-CPU to control these are stored into the Flash-ROM on the LGC board. New programs can be downloaded and updated from the download jig or a PC connected to the equipment with a USB by using these programs. Also, to prevent data loss and to simplify the data transfer process during the board replacement, the adjustment value and setting value, etc. are stored into the removable NVRAM on the LGC board.

2.2.3 Pin assignment

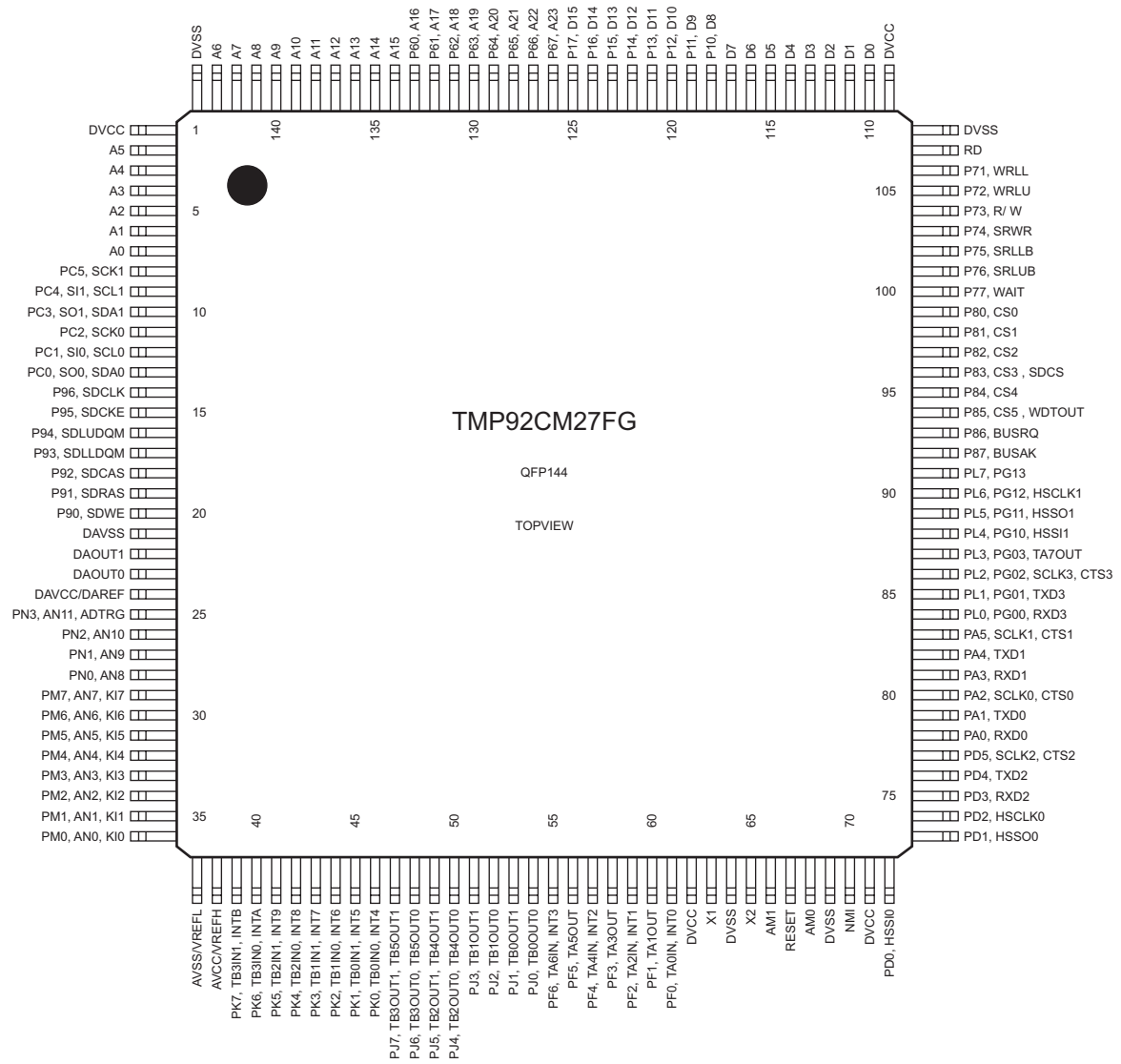

Fig. 2-2

2.2.4 Signals

Pin No.	Port name	Signal name	I/O	Function
1	DVCC1	+3.3VB	-	+3.3VB
2	A5	A[5]	O	Address bus [5]
3	A4	A[4]	O	Address bus [4]
4	A3	A[3]	O	Address bus [3]
5	A2	A[2]	O	Address bus [2]
6	A1	A[1]	O	Address bus [1]
7	A0	A[0]	O	Address bus [0]
8	PC5/SCK1	YIR-0T	I	FIFO overrun/underrun detection signal (L: error)
9	PC4/SL1/SCL1	MIR-0T	I	FIFO overrun/underrun detection signal (L: error)
10	PC3/SO1/SDA1	CIR-0T	I	FIFO overrun/underrun detection signal (L: error)
11	PC2/SCK0	KIR-0T	I	FIFO overrun/underrun detection signal (L: error)
12	PC1/SI0/SCL0	TSSTS-1T	I	Not used (for debug)
13	PC0/SO0/SDA0	ERR-1T	I	H-Sync error detection signal (H: error)
14	P96/SDCLK	SDCLK-1T	O	Bus control clock
15	P95/SDCKE	MASIN-0T	O	Printing start signal (L: start printing)
16	P94/SDLUDQM	LDON-0T	O	Enforced laser ON signal (L: enforced ON)
17	P93/SDLLDQM	LDOFF-0T	O	Enforced laser OFF signal (L: enforced OFF)
18	P92/$\overline{\text{SDCAS}}$	LE-0T	O	Laser enable signal (Low-active)
19	P91/$\overline{\text{SDRAS}}$	TSSTR-1T	O	Not used (for debug)
20	P90/$\overline{\text{SDWE}}$	BUSEN-0T	O	Not used (for debug)
21	DAVSS	SG	-	Reference voltage (L) for D/A converter (Signal ground)
22	DAOUT1	-	-	Not used
23	$\overline{\text{DAOUT0}}$	-	-	Not used
24	DAVCC/DAREF	+3.3VB	-	Reference voltage (H) for D/A converter (+3.3VB)
25	PN3/AN11/$\overline{\text{ADTRG}}$	-	-	Pull-down: signal ground
26	PN2/AN10	TR2MON-1TA	I	2nd transfer bias high voltage detection signal (Analog signal)
27	PN1/AN9	KDRTH-1TA	I	Drum thermistor-K output signal (Analog signal)
28	PN0/AN8	YDRTH-1TA	I	Drum thermistor-Y output signal (Analog signal)
29	PM7/AN7/KI7	KATSN-1TA	I	Auto-toner sensor-K output signal (Analog signal)
30	PM6/AN6/KI6	CATSN-1TA	I	Auto-toner sensor-C output signal (Analog signal)
31	PM5/AN5/KI5	MATSN-1TA	I	Auto-toner sensor-M output signal (Analog signal)
32	PM4/AN4/KI4	YATSN-1TA	I	Auto-toner sensor-Y output signal (Analog signal)

Pin No.	Port name	Signal name	I/O	Function
33	PM3/AN3/KI3	TR1MONK-1TA	I	1st transfer bias (K) high voltage detection signal (Analog signal)
34	PM2/AN2/KI2	TR1MONC-1TA	I	1st transfer bias (C) high voltage detection signal (Analog signal)
35	PM1/AN1/KI1	TR1MONM-1TA	I	1st transfer bias (M) high voltage detection signal (Analog signal)
36	PM0/AN0/KI0	TR1MONY-1TA	I	1st transfer bias (Y) high voltage detection signal (Analog signal)
37	AVSS/VREFL	SG	-	Reference voltage (L) for A/D converter (Signal ground)
38	ACCC/VREFH	+3.3VB	-	Reference voltage (H) for A/D converter (+3.3VB)
39	PK7/TB3IN1/INTB	RSVI0-0	-	-
40	$\overline{\text{PK6/TB3IN0/INTA}}$	RSVI1-0	-	-
41	$\overline{\text{PK5/TB2IN1/INT9}}$	FRMSTS-0T	I	Flash ROM status signal (H: ready, L: busy)
42	$\overline{\text{PK4/TB2IN0/INT8}}$	INT8-1T	I	ASIC(EC/N121) interrupt signal (H: interrupt)
43	PK3/TB1IN1/INT7	INT7-1T	I	ASIC(EC/N121) interrupt signal (H: interrupt)
44	PK2/TB1IN0/INT6	INT6-1T	I	ASIC(EC/N121) interrupt signal (H: interrupt)
45	PK1/TB0IN1/INT5	INT5-1T	I	ASIC(EC/N121) interrupt signal (H: interrupt)
46	PK0/TB0IN0/INT4	UHSCTCP-1T	I	Secondary scanning direction line coincidence status signal (L: match)
47	PJ7/TB3OUT1/ TB5OUT1	YPVDEN-0T	I	Printing status signal (Y) (L: printing)
48	PJ6/TB3OUT0/ TB5OUT0	MPVDEN-0T	I	Printing status signal (M) (L: printing)
49	PJ5/TB2OUT1/ TB4OUT1	CPVDEN-0T	I	Printing status signal (C) (L: printing)
50	PJ4/TB2OUT0/ TB4OUT0	KPVDEN-0T	I	Printing status signal (K) (L: printing)
51	PJ3/TB1OUT1	GCCTCP-1T	I	Pixel counter coincidence status signal (H: coincided)
52	PJ2/TB1OUT0	EWSCN-0T	I	Not used (for debug)
53	PJ1/TB0OUT1	-	-	-
54	PJ0/TB0OUT0	-	-	-
55	PF6/TA6IN/INT3	HSCTCP-1T	I	Secondary scanning direction line coincidence status signal (L: match)
56	PF5/TA5OUT	MCRUN-0T	O	MFP operating signal for external counter
57	PF4/TA4IN/INT2	PWRDN-1TA	I	Switching regulator power down signal (L: normal, up-edge trigger: when +5VB down)
58	PF3/TA3OUT	EXMCK-1T	O	Exit motor reference clock
59	PF2/TA2IN/INT1	SCMDINT-1T	I	System interface command reception end signal
60	PF1/TA1OUT	RGMCK-1T	O	Registration motor reference clock

Pin No.	Port name	Signal name	I/O	Function
61	PF0/TA0IN/INT0	SSTSINT-1T	I	System interface status reception end signal
62	DVCC2	+3.3VB	-	+3.3VB
63	X1	CPUCK-1T	I	Clock input (34MHz)
64	DVSS1	SG	-	Signal ground
65	X2	-	-	Not used (Open)
66	AM1	-	-	Pull-down: signal ground
67	$\overline{\text{RESET}}$	MRST-0T	I	Reset signal (Low-active)
68	AM0	-	-	Pull-up: +3.3VB
69	DVSS2	SG	-	Signal ground
70	$\overline{\text{NMI}}$	-	-	Pull-up: +3.3VB
71	DVCC3	+3.3VB	-	+3.3VB
72	PD0/HSSI0	RGMSETI2-0T	O	Registration motor electric current control signal [2]
73	PD1/HSSO0	EXMSETI2-0T	O	Exit motor electric current control signal [2]
74	PD2/HSCLK0	IPCSW-0TA	I	IPC board (finisher controller) connection signal (L: connected)
75	PD3/RXD2	EXTCTR-0T	O	Paper exit signal for copy key card
76	PD4/TXD2	WRAMUP-0T	O	Fuser unit warming-up detection signal (L: warming-up)
77	PD5/SCLK2/$\overline{\text{CTS2}}$	IMGCNT-0T	I	IMG board connection signal (L: connected)
78	PA0/RXD0	IMGLIFE-1T	I	IMG board status detection signal (H: normal, L: error)
79	PA1/TXD0	MMPI-1T	I	Boards disconnection detection signal (L: disconnected)
80	PA2/SCLK0/$\overline{\text{CTS0}}$	SZ0-0T	O	Paper size signal [0] for copy key card
81	PA3/RXD1	SZ1-0T	O	Paper size signal [1] for copy key card
82	PA4/TXD1	SZ2-0T	O	Paper size signal [2] for copy key card
83	PA5/SCLK1/$\overline{\text{CTS1}}$	SZ3-0T	O	Paper size signal [3] for copy key card
84	PL0/PG00/RXD3	RGMRST-0T	O	Registration motor reset signal (Low-active)
85	PL1/PG01/TXD3	RGMEN-1T	O	Registration motor enable signal (H: ON, L: OFF)
86	PL2/PG02/SCLK3/ $\overline{\text{CTS3}}$	RGMSETI1-0T	O	Registration motor electric current control signal [1]
87	PL3/PG03/ TA7OUT	RGMCW-1T	O	Registration motor rotational direction signal (H: CCW, L: CW)
88	PL4/PG10/HSSI1	EXMRST-0T	O	Exit motor reset signal (Low-active)
89	PL5/PG11/HSSO1	EXMEN-1T	O	Exit motor enable signal (H: ON, L: OFF)
90	PL6/PG12/ HSCLK1	EXMSETI1-0T	O	Exit motor electric current control signal [1]
91	PL7/PG13	EXMCW-1T	O	Exit motor rotational direction signal (H: CCW, L: CW)

Pin No.	Port name	Signal name	I/O	Function
92	P87/$\overline{\text{BUSAK}}$	FLCTR-0T	O	Full color printing count signal for copy key card
93	P86/$\overline{\text{BUSRQ}}$	MNCTR-0T	O	Mono color printing count signal for copy key card
94	P85/$\overline{\text{CS5}}$/ WDTOUT	WDT-0T	O	Watchdog output signal (H: CPU is normal, L: CPU is out of control)
95	P84/$\overline{\text{CS4}}$	WDE-1T	O	Watchdog enable signal (H: enable)
96	P83/$\overline{\text{CS3}}$/$\overline{\text{SDCS}}$	BKCTR-0T	O	Black-side printing count signal for copy key card
97	P82/$\overline{\text{CS2}}$	CS2-0T	O	Chip select signal [2] (Low-active) * For ASIC (EC/N121)
98	P81/$\overline{\text{CS1}}$	-	-	Not used (Open)
99	P80/$\overline{\text{CS0}}$	CS0-0T	O	Chip select signal [0] (Low-active) * For ASIC (EC/N121)
100	P77/$\overline{\text{WAIT}}$	WAIT-0T	I	Wait signal (Low-active)
101	P76/$\overline{\text{SRLUB}}$	SRLUB-0T	O	High-level data enable signal for SRAM (Low-active)
102	P75/$\overline{\text{SRLLB}}$	SRLLB-0T	O	Low-level data enable signal for SRAM (Low-active)
103	P74/$\overline{\text{SRWR}}$	SRWR-0T	O	Write signal for SRAM (Low-active)
104	P73/R/$\overline{\text{W}}$	R/W-0T	O	Read/write signal (H: read, L: write)
105	P72/$\overline{\text{WRLU}}$	SCRST-1T	O	PWM reset signal (Low-active)
106	P71/$\overline{\text{WRLL}}$	WR-0T	O	Write signal (Low-active)
107	$\overline{\text{RD}}$	RD-0T	O	Read signal (Low-active)
108	DVSS3	SG	-	Signal ground
109	DVCC4	+3.3VB	-	+3.3VB
110	D0	D[0]	I/O	Data bus [0]
111	D1	D[1]	I/O	Data bus [1]
112	D2	D[2]	I/O	Data bus [2]
113	D3	D[3]	I/O	Data bus [3]
114	D4	D[4]	I/O	Data bus [4]
115	D5	D[5]	I/O	Data bus [5]
116	D6	D[6]	I/O	Data bus [6]
117	D7	D[7]	I/O	Data bus [7]
118	P10/D8	D[8]	I/O	Data bus [8]
119	P11/D9	D[9]	I/O	Data bus [9]
120	P12/D10	D[10]	I/O	Data bus [10]
121	P13/D11	D[11]	I/O	Data bus [11]
122	P14/D12	D[12]	I/O	Data bus [12]
123	P15/D13	D[13]	I/O	Data bus [13]
124	P16/D14	D[14]	I/O	Data bus [14]
125	P17/D15	D[15]	I/O	Data bus [15]

Pin No.	Port name	Signal name	I/O	Function
126	P67/A23	A[23]	O	Address bus [23]
127	P66/A22	A[22]	O	Address bus [22]
128	P65/A21	A[21]	O	Address bus [21]
129	P64/A20	A[20]	O	Address bus [20]
130	P63/A19	A[19]	O	Address bus [19]
131	P62/A18	A[18]	O	Address bus [18]
132	P61/A17	A[17]	O	Address bus [17]
133	P60/A16	A[16]	O	Address bus [16]
134	A15	A[15]	O	Address bus [15]
135	A14	A[14]	O	Address bus [14]
136	A13	A[13]	O	Address bus [13]
137	A12	A[12]	O	Address bus [12]
138	A11	A[11]	O	Address bus [11]
139	A10	A[10]	O	Address bus [10]
140	A9	A[9]	O	Address bus [9]
141	A8	A[8]	O	Address bus [8]
142	A7	A[7]	O	Address bus [7]
143	A6	A[6]	O	Address bus [6]
144	DVSS4	SG	-	Signal ground

2.3 ASIC (EC/N121)

2.3.1 Functions

The ASIC is controlled by command from the Engine-CPU and the logic circuit inside the ASIC. The primary functions of the ASIC are as follows.

- I/O control of each electrical part (motor, sensor, switch, electromagnetic spring clutch, solenoid, etc.)
- Interface to control the PFP, LCF and finisher
- Interface to control the NVRAM on the LGC board
  (An erroneous data loss is prevented with a key circuit provided when the CPU is running away.)

2.3.2 Pin assignment

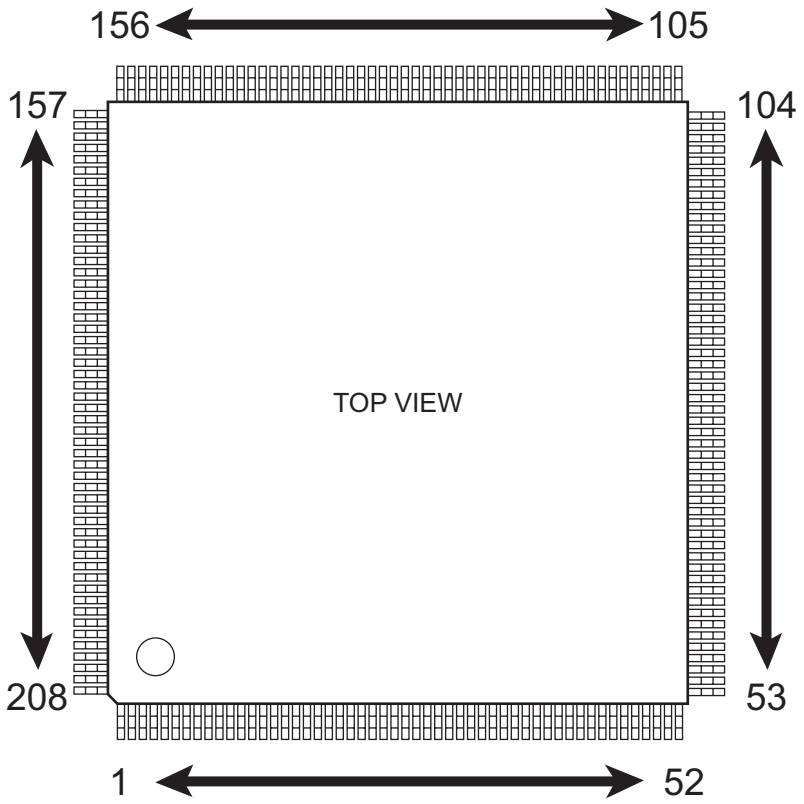

Fig. 2-3

2.3.3 Signals

Pin No.	Port name	Signal name	I/O	Function
1	GND1	SG	-	Signal ground
2	GND2	SG	-	Signal ground
3	VDD_IO1	+3.3VB	-	+3.3VB
4	SDCLK	SDCLK-1T	I	Bus control clock
5	GND3	SG	-	Signal ground
6	A0	A[0]	I	Address bus [0]
7	A1	A[1]	I	Address bus [1]
8	A2	A[2]	I	Address bus [2]
9	A3	A[3]	I	Address bus [3]
10	A4	A[4]	I	Address bus [4]
11	A5	A[5]	I	Address bus [5]
12	A6	A[6]	I	Address bus [6]
13	A7	A[7]	I	Address bus [7]
14	A8	A[8]	I	Address bus [8]
15	A9	A[9]	I	Address bus [9]
16	A10	A[10]	I	Address bus [10]
17	A11	A[11]	I	Address bus [11]
18	A12	A[12]	I	Address bus [12]
19	PL0/MON0	-	-	Pull-up: +3.3VB
20	PL1/MON1	-	-	Pull-up: +3.3VB
21	PL2/MON2	-	-	Pull-up: +3.3VB
22	A16	A[16]	I	Address bus [16]
23	A17	A[17]	I	Address bus [17]
24	A18	A[18]	I	Address bus [18]
25	A19	A[19]	I	Address bus [19]
26	GND4	SG	-	Signal ground
27	VDD_CORE1	+2.5V	-	+2.5V
28	PM0/A20	A[20]	I	Address bus [20]
29	PM1/A21	A[21]	I	Address bus [21]
30	PM2/A22	A[22]	I	Address bus [22]
31	PM3/A23	A[23]	I	Address bus [23]
32	D7	D[7]	I/O	Data bus [7]
33	D6	D[6]	I/O	Data bus [6]
34	D5	D[5]	I/O	Data bus [5]

Pin No.	Port name	Signal name	I/O	Function
35	D4	D[4]	I/O	Data bus [4]
36	D3	D[3]	I/O	Data bus [3]
37	D2	D[2]	I/O	Data bus [2]
38	D1	D[1]	I/O	Data bus [1]
39	D0	D[0]	I/O	Data bus [0]
40	TEST1	-	-	Pull-up: +3.3VB
41	CPURD	RD-0T	I	Read signal (Low-active)
42	CPUWRL	EMWR-0 T	I	Write signal (Low-active)
43	WAIT	WAIT-0T	O	Wait signal (Low-active)
44	CSI	CS0-0T	I	Chip select signal [0] (Low-active) * For ASIC (EC/N121)
45	DLCS	-	-	Pull-up: +3.3VB
46	BTCPUCS	CS2-0T	I	Chip select signal [2] (Low-active) * For ASIC (EC/N121)
47	ROM_SEL	ROMDT-0T	I	Download jig connection signal (L: connected)
48	GND5	SG	-	Signal ground
49	RESET	MRST-0T	I	Reset signal (Low-active)
50	VDD_IO2	+3.3VB	-	+3.3VB
51	GND6	SG	-	Signal ground
52	GND7	SG	-	Signal ground
53	VDD_CORE2	+2.5V	-	+2.5V
54	VDD_IO3	+3.3VB	-	+3.3VB
55	PK7/CS11	LZCS-0T	O	Chip select signal (Low-active) * For printer engine ASIC
56	PK6/CS10	DEBCS-0T	O	Not used (for debug)
57	PK5/CS9	PMCS4-0T	O	Chip select signal (Low-active) * For PWM-K
58	PK4/CS8	PMCS3-0T	O	Chip select signal (Low-active) * For PWM-C
59	PK3/INTO3	INT6-1T	O	ASIC (EC/N121) interrupt signal (H: interrupt)
60	PK2/INTO2	INT5-1T	O	ASIC (EC/N121) interrupt signal (H: interrupt)
61	PK1/INTO1	SSTSINT-1T	O	System interface status reception end signal
62	PK0/INTO0	SCMDINT-1T	O	System interface command reception end signal
63	MWR	MWR-0T	O	Write enable signal for NVRAM (Low-active)
64	PC7/CS7	PMCS2-0T	O	Chip select signal (Low-active) * For PWM-M
65	PC6/CS6	PMCS1-0T	O	Chip select signal (Low-active) * For PWM-Y

Pin No.	Port name	Signal name	I/O	Function
66	PC5/CS5	OPALCS-0T	O	Chip select signal (Low-active) * For ASIC (EC/N106)
67	PC4/CS4	IPCCS-0T	O	Chip select signal (Low-active) * For IPC board (finisher controller)
68	PC3/CS3/FRAM	NVCS-0T	O	Chip select signal (Low-active) * For NVRAM
69	PC2/CS2	SRAMCS-0T	O	Chip select signal (Low-active) * For SRAM
70	PC1/CS1	DLBDCS-0T	O	Chip select signal (Low-active) * For download jig
71	PC0/CS0	FROMCS-0T	O	Chip select signal (Low-active) * For Flash ROM
72	TDO	-	-	Not used (Open)
73	TMS	-	-	Not used (Open)
74	TCK	-	-	Not used (Open)
75	GND8	SG	-	Signal ground
76	CLKIN	EXCLK-1T	I	Clock input (34MHz)
77	VDD_IO4	+3.3VB	-	+3.3VB
78	VDD_CORE3	+2.5V	-	+2.5V
79	GND9	SG	-	Signal ground
80	TRST	-	-	Not used (Open)
81	PD7/TO11	DVMCK-1T	O	Developer motor reference clock
82	PD6/TO10	FDMCK-1T	O	Feed/transport motor reference clock
83	PD5/TO9	FSMCK-1T	O	Fuser motor reference clock
84	PD4/TO8	PMCK-1T	O	Polygonal motor reference clock
85	PD3/TO7	HVTCLK-1T	O	Clock for Developer AC bias
86	PD2/TO6	TNLED-0T	O	Image quality sensor switching signal (H: black toner detected, L: color toner detected)
87	PD1/INTPO5/SIO-CLK	INT8-1T	O	ASIC (EC/N121) interrupt signal (H: interrupt)
88	PD0/INTPO4	INT7-1T	O	ASIC (EC/N121) interrupt signal (H: interrupt)
89	PE7/DACDO	DACOUT-1T	O	D/A converter serial data
90	PE6/DACCK	DACCLK-1T	O	D/A converter serial data transfer clock
91	PE5/DACLD	DACLD-1T	O	D/A converter latch signal
92	PE4/EEPRMCS1	YPUCNT-0T	I	EPU-Y connection signal (L: connected)
93	PE3/EEPRMDO	KCLNLT-0T	I	Needle electrode cleaner detection sensor detection signal (H: limit position)
94	PE2/EEPRMDI	CCLNLT-0T	I	Not used
95	PE1/EEPRMCK	MCLNLT-0T	I	Not used

Pin No.	Port name	Signal name	I/O	Function
96	PE0/EEPRMCS0	YCLNLT-0T	I	Not used
97	TDI	-	-	Not used (Open)
98	PB7/MON2	KPUCNT-0T	I	EPU-K connection signal (L: connected)
99	PB6/MON1	CPUCNT-0T	I	EPU-C connection signal (L: connected)
100	PB5/MON0	MPUCNT-0T	I	EPU-M connection signal (L: connected)
101	PB4/RW	R/W-0T	I	Read/write signal (H: read, L: write)
102	PB3/BUSOE	BUSOE-0T	O	Bus output enable signal for IPC (Low-active)
103	VDD_IO5	+3.3VB	-	+3.3VB
104	VDD_CORE4	+2.5V	-	+2.5V
105	GND10	SG	-	Signal ground
106	GND11	SG	-	Signal ground
107	VDD_IO6	+3.3VB	-	+3.3VB
108	PB2/BUSOE1	BUSOE1-0T	O	Bus output enable signal for NVRAM (Low-active)
109	PB1/BUSDIR0	BUSDIR-0T	O	Bus connection direction switching signal (H: CPU -> printer engine ASIC, L: CPU <- ASIC)
110	PB0/WR_P	EXWR-0T	O	PWM write signal (Low-active)
111	TEST3	-	-	Pull-up: +3.3VB
112	PJ7/PIFCKB	PIFCKB-1T	O	PFP/LCF output data latch signal [B] (Up-edge trigger) * 📖 P. 2-27 "[3] Description of signals DRV0-0C to 7-0C"
113	PJ6/PIFCKA	PIFCKA-1T	O	PFP/LCF output data latch signal [A] (Up-edge trigger) * 📖 P. 2-27 "[3] Description of signals DRV0-0C to 7-0C"
114	PJ5/SCSWB	SCSWB-0T	O	PFP/LCF input data enable signal [B] (Low-active) * 📖 P. 2-25 "[2] Description of signals RETS0-0C to 7C"
115	PJ4/SCSWA	SCSWA-0T	O	PFP/LCF input data enable signal [A] (Low-active) * 📖 P. 2-25 "[2] Description of signals RETS0-0C to 7C"
116	PJ3/PIFDI11	PIFDI[11]	I/O	PFP/LCF input/output signal [11] * 📖 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
117	PJ2/PIFDI10	PIFDI[10]	I/O	PFP/LCF input/output signal [10] * 📖 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
118	PJ1/PIFDI9	PIFDI[9]	I/O	PFP/LCF input/output signal [9] * 📖 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
119	PJ0/PIFDI8	PIFDI[8]	I/O	PFP/LCF input/output signal [8] * 📖 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"

Pin No.	Port name	Signal name	I/O	Function
120	PI7/PIFDI7	PIFDI[7]	I/O	PFP/LCF input/output signal [7] * 🕮 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
121	PI6/PIFDI6	PIFDI[6]	I/O	PFP/LCF input/output signal [6] * 🕮 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
122	PI5/PIFDI5	PIFDI[5]	I/O	PFP/LCF input/output signal [5] * 🕮 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
123	PI4/PIFDI4	PIFDI[4]	I/O	PFP/LCF input/output signal [4] * 🕮 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
124	PI3/PIFDI3	PIFDI[3]	I/O	PFP/LCF input/output signal [3] * 🕮 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
125	PI2/PIFDI2	PIFDI[2]	I/O	PFP/LCF input/output signal [2] * 🕮 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
126	PI1/PIFDI1	PIFDI[1]	I/O	PFP/LCF input/output signal [1] * 🕮 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
127	PI0/PIFDI0	PIFDI[0]	I/O	PFP/LCF input/output signal [0] * 🕮 P. 2-24 "[1] Description of signals PIFDI [0] to [11]"
128	PG7/HT2ON	PHON-0T	O	Pressure roller lamp control signal (L: ON)
129	TMC1	-	-	Not used (Open)
130	VDD_CORE5	+2.5V	-	+2.5V
131	GND12	SG	-	Signal ground
132	VDD_IO7	+3.3V	-	+3.3V
133	TMC2	-	-	Not used (Open)
134	PG6/HT1ON	BHSON-0T	O	Side heater lamp control signal (L: ON)
135	PG5/HT0ON	BHCON-0T	O	Center heater lamp control signal (L: ON)
136	PG4/THCMP	-	-	Pull-up: +3.3VB
137	PG3/TH2	TBCNT-0TA	I	Transfer belt unit connection signal (L: connected)
138	PG2/TH1	CS2FEED-1TA	I	2nd drawer feed sensor detection signal (H: paper being transported, L: no paper)
139	PG1/TH0	CS1FEED-1TA	I	1st drawer feed sensor detection signal (H: paper being transported, L: no paper)
140	HTERR/PG0	HTERR-0C	I	Fuser unit abnormality detection signal (H: heater abnormal)
141	GND13	SG	-	Signal ground
142	PA3/TRG3/TI1	TB2JAM-1TA	I	Paper clinging detection sensor detection signal (H: paper clinging)
143	PA2/TRG2/TI0	RGSTS-1TA	I	Registration sensor detection signal (H: paper being transported, L: no paper)

Pin No.	Port name	Signal name	I/O	Function
144	PA1/TRG1	RGREAR-1TA	I	Image positioning sensor (rear) detection signal (L: test pattern detected)
145	PA0/TRG0	RGFRNT-1TA	I	Image positioning sensor (front) detection signal (L: test pattern detected)
146	TRG5/PF7	LCCNT-0TA	I	LCF connection signal (L: connected)
147	TRG4/PF6	EXTSW-1TA	I	Exit sensor detection signal (H: paper being transported, L: no paper)
148	PF5/ADCDI	ADCDI-1C	I	A/D converter input data
149	PF4/ADCSTRB	ADCSTRB-1C	I	A/D converter status signal
150	PF3/ADCCS1	-	-	Pull-up: +3.3VB
151	PF2/ADCDO	ADCDO-1T	O	A/D converter output data
152	PF1/ADCCK	ADCCK-1T	O	A/D converter driving clock
153	PF0/ADCCS0	ADCCS0-0T	O	Chip select signal (Low-active) * For A/D converter
154	VDD_IO8	+3.3VB	-	+3.3VB
155	GND14	SG	-	Signal ground
156	GND15	SG	-	Signal ground
157	VDD_CORE6	+2.5V	-	+2.5V
158	VDD_IO9	+3.3VB	-	+3.3VB
159	PH7/CMD0	CMD-0TA	I	System interface received data signal
160	PH6/CERR0	CERR-0T	O	System interface command error signal
161	PH5/CBSY0	CBSY-0TA	I	System interface command busy signal
162	PH4/CACK0	CACK-0T	O	System interface command acknowledge signal
163	PH3/STS0	STS-0T	O	System interface transmitted data signal
164	PH2/SERR0	SERR-0TA	I	System interface status error signal
165	PH1/SBSY0	SBSY-0T	O	System interface status busy signal
166	PH0/SACK0	SACK-0TA	I	System interface status acknowledge signal
167	TEST2	-	-	Not used (Open)
168	CTRI	-	-	Pull-down: signal ground
169	STPA7/TO4	-	-	Pull-up: +3.3VB
170	STPA6/IC02	TILTC-0T	O	Mirror motor-C enable signal (H: OFF, L: ON)
171	STPA5/IC01	TILTM-0T	O	Mirror motor-M enable signal (H: OFF, L: ON)
172	STPA4/IC00	TILTK-0T	O	Mirror motor-K enable signal (H: OFF, L: ON)
173	STPA3/RST0/ PH0D	TILT3-0T	O	Mirror motor driving signal [phase-D]
174	STPA2/ENBL0/ PH0C	TILT2-0T	O	Mirror motor driving signal [phase-C]
175	STPA1/DIR0/PH0B	TILT1-0T	O	Mirror motor driving signal [phase-B]

Pin No.	Port name	Signal name	I/O	Function
176	STPA0/TO0/PH0A	TILT0-0T	O	Mirror motor driving signal [phase-A]
177	STPB7/TO5	PFPCK-1	O	PFP/LCF data transfer clock
178	STPB6/IC12	DMSETI3-0T	O	Drum motor electric current control signal [2]
179	STPB5/IC11	DMSETI2-0T	O	Drum motor electric current control signal [1]
180	STPB4/IC10	DMSETI1-0T	O	Drum motor electric current control signal [0]
181	STPB3/RST1	DMRST-0T	O	Drum motor reset signal (Low-active)
182	GND16	SG	-	Signal ground
183	VDD_CORE7	+2.5V	-	+2.5V
184	VDD_IO9	+3.3VB	-	+3.3VB
185	STPB2/ENBL1/ PH1C	DMEN-1T	O	Drum motor enable signal (H: ON, L: OFF)
186	STPB1/DIR1/ PH1B	DRMDIR-0T	O	Drum motor rotational direction signal (H: CCW, L: CW)
187	STPB0/TO1/PH1A	DMCK-1T	O	Drum motor reference clock
188	STPC7/IC41	-	-	Pull-up: +3.3VB
189	STPC6/IC40	-	-	Pull-up: +3.3VB
190	STPC5/IC21	TBMSETI2-0T	O	Transfer belt motor electric current control signal [1]
191	STPC4/IC20	TBMSETI1-0T	O	Transfer belt motor electric current control signal [0]
192	STPC3/RST2/ PH2D	TBMRST-1T	O	Transfer belt motor reset signal (Low-active)
193	STPC2/ENBL2/ PH2C	TBMEN-0T	O	Transfer belt motor enable signal (H: ON, L: OFF)
194	STPC1/DIR2/ PH2B	TBMDIR-0T	O	Transfer belt motor rotational direction signal (H: CCW, L: CW)
195	STPC0/TO2/PH2A	TBMCK-1T	O	Transfer belt motor reference clock
196	STPD7/IC51	CLKSEL-0	-	-
197	STPD6/IC50	MTEN-1T	O	Pulse motor enable signal (H: ON, L: OFF) * Enable the buffer for each signal of the drum motor, transfer belt motor, registration motor, exit motor and ADU motor.
198	STPD5/IC31	ADMSETI2-0T	O	ADU motor electric current control signal [1]
199	STPD4/IC30	ADMSETI1-0T	O	ADU motor electric current control signal [0]
200	STPD3/RST3/ PH3D	ADUMD-0T	O	ADU motor driving signal [phase-D]
201	STPD2/ENBL3/ PH3C	ADUMC-0T	O	ADU motor driving signal [phase-C]
202	SPD1/DIR3/PH3B	ADUMB-0T	O	ADU motor driving signal [phase-B]
203	STPD0/TO3/PH3A	ADUMA-0T	O	ADU motor driving signal [phase-A]
204	PROTECT	-	-	Pull-up: +3.3VB
205	GND17	SG	-	Signal ground

Pin No.	Port name	Signal name	I/O	Function
206	SYSCLKO	-	-	Not used (Open)
207	VDD_IO11	+3.3VB	-	+3.3VB
208	VDD_CORE8	+2.5V	-	+2.5V

[1] Description of signals PIFDI [0] to [11]

Each signal is assigned to PIFDI [0] to [11] which are the interface signals of the PFP and LCF as shown in the following table. See the items below for the details of the signals.

- 🕮 P. 2-25 "[2] Description of signals RETS0-0C to 7C"
- 🕮 P. 2-27 "[3] Description of signals DRV0-0C to 7-0C"

Signal name	Input port (ASIC <- PFP/LCF)	Output port (ASIC -> PFP/LCF)
PIFDI[0]	RETS0-0C	DRV0-0C
PIFDI[1]	RETS1-0C	DRV1-0C
PIFDI[2]	RETS2-0C	DRV2-0C
PIFDI[3]	RETS3-0C	DRV3-0C
PIFDI[4]	RETS4-0C	DRV4-0C
PIFDI[5]	RETS5-0C	DRV5-0C
PIFDI[6]	RETS6-0C	DRV6-0C
PIFDI[7]	RETS7-0C	DRV7-0C
PIFDI[8]	SIZE0-0C (Not used)	-
PIFDI[9]	SIZE1-0C (Not used)	-
PIFDI[10]	SIZE2-0C (Not used)	-
PIFDI[11]	SIZE3-0C (Not used)	-

[2] Description of signals RETS0-0C to 7C

The following functions are assigned to signals RETS0-0C to 7C depending on the status of the signals SCSWA-0T to B-0T and installation status of the PFP and LCF.

[2-1] When SCSWA-0T is Low and the PFP is installed:

Signal name	Function
RETS0-0C	PFP upper drawer tray-up sensor detection signal (H: top position, L: normal)
RETS1-0C	PFP upper drawer empty sensor detection signal (H: no paper, L: paper presence)
RETS2-0C	PFP side cover opening/closing switch detection signal (H: cover opened, L: cover closed)
RETS3-0C	PFP connection signal (L: connected)
RETS4-0C	PFP upper drawer feed sensor detection signal (H: paper being transported, L: no paper)
RETS5-0C	PFP upper drawer paper stock sensor detection signal (H: drawer almost empty, L: others except this)
RETS6-0C	PFP upper drawer detection switch detection signal (H: drawer open, L: drawer closed)
RETS7-0C	Not used

[2-2] When SCSWB-0T is Low and PFP is installed:

Signal name	Function
RETS0-0C	PFP lower drawer tray-up sensor detection signal (H: top position, L: normal)
RETS1-0C	PFP lower drawer empty sensor detection signal (H: no paper, L: paper presence)
RETS2-0C	Not used
RETS3-0C	PFP motor PLL control signal (H: stop or error, L: driving in constant speed)
RETS4-0C	PFP lower drawer feed sensor detection signal (H: paper being transported, L: no paper)
RETS5-0C	PFP lower drawer paper stock sensor detection signal (H: drawer almost empty, L: others except this)
RETS6-0C	PFP lower drawer detection switch detection signal (H: drawer open, L: drawer closed)
RETS7-0C	Not used

[2-3] When SCSWA-0T is Low and LCF is installed:

Signal name	Function
RETS0-0C	LCF feeding side paper stock sensor detection signal (H: drawer almost empty, L: others except this)
RETS1-0C	Not used
RETS2-0C	Not used
RETS3-0C	Not used
RETS4-0C	Not used
RETS5-0C	LCF drawer detection switch detection signal (H: drawer open, L: drawer closed)
RETS6-0C	LCF feeding side paper mis-stacking sensor detection signal (H: lever to detect mis-stacking is opened)
RETS7-0C	LCF tray bottom sensor detection signal (H: bottom position, L: normal)

[2-4] When SCSWB-0T is Low and LCF is installed:

Signal name	Function
RETS0-0C	LCF feeding side paper empty sensor detection signal (H: paper presence, L: no paper)
RETS1-0C	LCF drawer feed sensor detection signal (H: no paper, L: paper being transported)
RETS2-0C	LCF tray-up sensor detection signal (H: top position, L: normal)
RETS3-0C	LCF transport motor LD signal (H: normal rotation, L: rotation error)
RETS4-0C	LCF side cover opening/closing switch detection signal (H: cover closed, L: cover open)
RETS5-0C	LCF standby side paper empty sensor detection signal (H: no paper, L: paper presence)
RETS6-0C	LCF end fence stop position sensor detection signal (H: stop position)
RETS7-0C	LCF end fence home position sensor detection signal (H: home position)

[3] Description of signals DRV0-0C to 7-0C

The following functions are assigned to the signals DRV0-0C to 7-0C depending on the installation status of the PFP and LCF. These signals are latched by the up-edge trigger of the PIFCLKA-1T or PIFCLKB-1T signal.

[3-1] When PIFCKA-1 is Up-edge trigger and PFP is installed:

Signal name	Function
DRV0-0C	Not used
DRV1-0C	PFP motor drive signal (H: OFF, L: ON)
DRV2-0C	PFP motor speed switching signal (H: high speed drive, L: low speed drive)
DRV3-0C	Not used
DRV4-0C	PFP upper drawer feed clutch driving signal (H: ON, L: OFF)
DRV5-0C	PFP lower drawer feed clutch driving signal (H: ON, L: OFF)
DRV6-0C	PFP transport clutch drive signal (H: ON, L: OFF)
DRV7-0C	Not used

[3-2] When PIFCKB-1 is Up-edge trigger and PFP is installed:

Signal name	Function
DRV0-0C	PFP upper drawer tray-up motor driving signal [A]
DRV1-0C	PFP upper drawer tray-up motor driving signal [B] DRV1-0C DRV0-0C Status L L OFF L H Up H L Down H H Brake
DRV2-0C	PFP lower drawer tray-up motor driving signal [A]
DRV3-0C	PFP lower drawer tray-up motor driving signal [B] DRV3-0C DRV2-0C Status L L OFF L H Up H L Down H H Brake
DRV4-0C	Not used
DRV5-0C	Not used
DRV6-0C	Not used
DRV7-0C	Not used

[3-3] When PIFCKA-1 is Up-edge trigger and LCF is installed:

Signal name	Function
DRV0-0C	LCF transport motor driving signal (H: ON)
DRV1-0C	LCF transport motor speed switch signal (H: low speed drive, L: high speed drive)
DRV2-0C	LCF transport clutch drive signal (H: ON, L: OFF)
DRV3-0C	LCF feed clutch drive signal (H: ON, L: OFF)
DRV4-0C	LCF pickup solenoid driving signal (H: ON, L: OFF)
DRV5-0C	Not used
DRV6-0C	Not used
DRV7-0C	Not used

[3-4] When PIFCKB-1 is Up-edge trigger and LCF is installed:

Signal name	Function
DRV0-0C	LCF tray-up motor driving signal [A]
DRV1-0C	LCF tray-up motor driving signal [B] DRV1-0C DRV0-0C Status L L OFF L H Up H L Down H H Brake
DRV2-0C	LCF end fence motor driving signal [A]
DRV3-0C	LCF end fence motor driving signal [B] DRV3-0C DRV2-0C Status L L OFF L H Transfer H L Reverse H H Brake
DRV4-0C	LCF end fence solenoid driving signal (H: OFF, L: ON)
DRV5-0C	Not used
DRV6-0C	Not used
DRV7-0C	Not used

2.4 ASIC (EC/N106)

2.4.1 Functions

The ASIC is controlled by command from the Engine-CPU and the logic circuit inside the ASIC. The primary functions of the ASIC are as follows.

- I/O control of each electrical part (motor, sensor, switch, electromagnetic spring clutch, solenoid, etc.)
- Interface to control the high-voltage transformer, bypass unit and ADU

2.4.2 Pin assignment

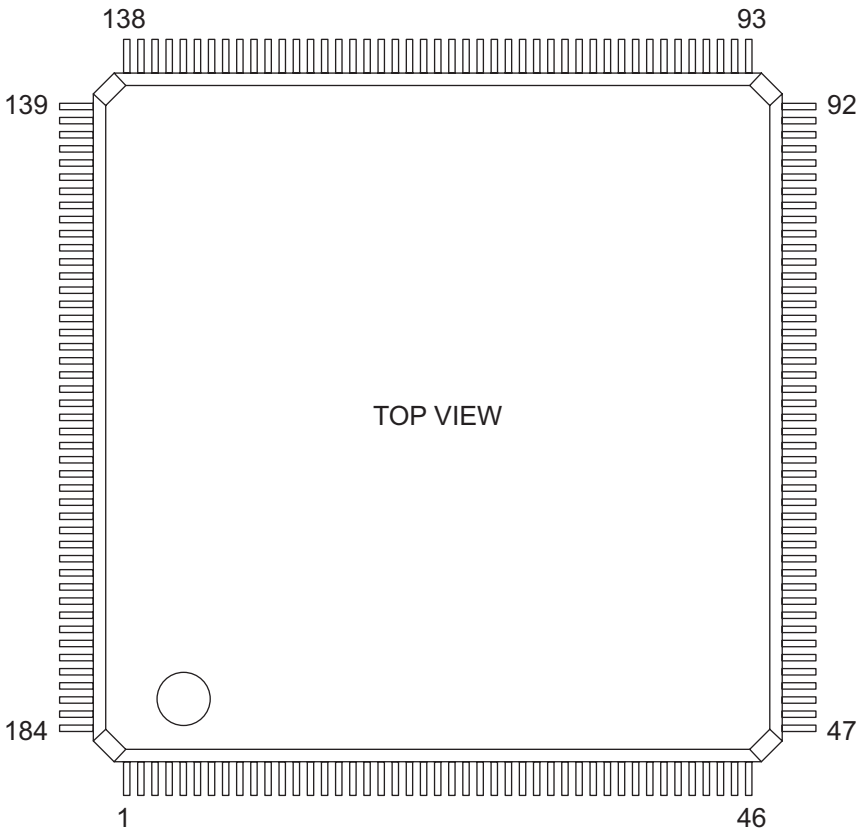

Fig. 2-4

2.4.3 Signals

Pin No.	Port name	Signal name	I/O	Function
1	VSS1	SG	-	Signal ground
2	D7_1	D[7]	I/O	Data bus [7]
3	D6_1	D[6]	I/O	Data bus [6]
4	D5_1	D[5]	I/O	Data bus [5]
5	D4_1	D[4]	I/O	Data bus [4]
6	D3_1	D[3]	I/O	Data bus [3]
7	D2_1	D[2]	I/O	Data bus [2]
8	D1_1	D[1]	I/O	Data bus [1]
9	D0_1	D[0]	I/O	Data bus [0]
10	HVDD1-1	+3.3VB	-	+3.3VB
11	VSS2	SG	-	Signal ground
12	PA7_1	OZFANL-0C	O	Ozone exhaust fan low speed driving signal
13	PA6_1	OZFANH-0C	O	Ozone exhaust fan high speed driving signal OZFANH-0C OZFANL-0C Status L L Not used L H High speed drive H L Low speed drive H H Stop
14	PA5_1	PLFANL-0C	O	Laser unit cooling fan low speed driving signal
15	PA4_1	PLFANH-0C	O	Laser unit cooling fan high speed driving signal PLFANH-0C PLFANL-0C Status L L Not used L H High speed drive H L Low speed drive H H Stop
16	PA3_1	MRSTSW-0C	O	Main switch reset signal (H: normal L: reset (power is turned OFF))
17	PA2_1	PMMTR-0C	O	Polygonal motor ON/OFF signal (H: OFF, L: ON)
18	PA1_1	RGREON-0C	O	Image positioning sensor LED lighting signal (L: light)
19	PA0_1	-	-	Not used
20	HVDD2-1	+5.1VB	-	+5.1VB
21	LVDD1	+3.3VB	-	+3.3VB
22	PB7_1	LSUSLB-0C	-	Not used
23	PB6_1	LSUSLA-0C	O	Sensor shutter solenoid ON/OFF signal (H: OFF, L: ON)
24	PB5_1	-	-	Not used
25	PB4_1	-	-	Not used
26	PB3_1	KERSLP-0C	O	Discharge LED-K driving signal (L: ON)
27	PB2_1	-	-	Not used

Pin No.	Port name	Signal name	I/O	Function
28	PB1_1	-	-	Not used
29	PB0_1	YERLED-0C	O	Discharge LED-Y/M/C driving signal (L: ON)
30	VSS3	SG	-	Signal ground
31	PC7_1	PMSNC-0C	I	Polygonal motor ready signal (L: ready)
32	PC6_1	24VCHK-1C	I	+24V supply status detection signal (H: Supply (cover closed), L: Cutoff (cover open)) * +24VD1/D2/D3 are supplied/cut off by the cover interlock switch.
33	PC5_1	ADCOV-0C	I	ADU opening/closing switch detection signal (H: ADU open, L: ADU closed)
34	PC4_1	LUSTSW-1C	I	Shutter status detection sensor detection signal (Up-edge trigger)
35	PC3_1	USTFULL-1C	I	Toner bag full detection sensor detection signal (H: toner bag full) * Detects only when the front cover is closed
36	PC2_1	TB2PS-1C	I	2nd transfer roller position detection sensor detection signal (H: release, L: contact)
37	PC1_1	BTPS2-1C	I	Used toner motor lock detection sensor detection signal (Signal level not changed: locked)
38	PC0_1	BTPS1-1C	I	1st transfer roller status detection sensor detection signal (Up-edge trigger: all colors contacted, Down-edge trigger: only K contacted)
39	HVDD2-2	+5.1VB	-	+5.1VB
40	PD7_1	RSVI10-0	-	Not used
41	PD6_1	RSVI9-0	-	Not used
42	PD5_1	RSVI8-0	-	Not used
43	PD4_1	RSVI7-0	-	Not used
44	PD3_1	RSVI6-0	-	Not used
45	PD2_1	RSVI5-0	-	Not used
46	PD1_1	RSVI4-0	-	Not used
47	PD0_1	RSVI3-0	-	Not used
48	VSS4	SG	-	Signal ground
49	PE7_1	-	-	Not used
50	PE6_1	LODLED-0C	O	Download jig LED driving signal (L: ON)
51	PE5_1	TBLTM1B-1C	O	1st transfer roller cam motor driving signal [B]
52	PE4_1	TBLTM1A-0C	O	1st transfer roller cam motor driving signal [A] TBLTM1B-1C / TBLTM1A-0C / Status L / L / OFF L / H / Not used H / L / Release H / H / Brake
53	PE3_1	TNMXMT-0C	O	Used toner motor ON/OFF signal (L: ON)
54	PE2_1	ADUCL-0C	O	ADU clutch ON/OFF signal (L: ON)

Pin No.	Port name	Signal name	I/O	Function
55	PE1_1	MNTLSL-0C	O	Bypass pickup solenoid driving signal (H: OFF, L: ON (pickup))
56	PE0_1	MNFDCL-0C	O	Bypass feed clutch ON/OFF signal (L: ON)
57	HVDD2-3	+5.1VB	-	+5.1VB
58	PF7_1	ADUS2-1C	I	ADU exit sensor detection signal (H: paper being transported, L: no paper)
59	PF6_1	ADUS1-1C	I	ADU entrance sensor detection signal (H: paper being transported, L: no paper)
60	PF5_1	MNPEN-1C	I	Bypass paper sensor detection signal (H: no paper on the bypass tray, L: paper presence)
61	PF4_1	MNFDSN-1C	I	Bypass feed sensor detection signal (H: normal, L: paper being transported)
62	PF3_1	MNPS3-0C	I	Bypass unit slide guide width detection signal [3] (Low-active)
63	PF2_1	MNPS2-0C	I	Bypass unit slide guide width detection signal [2] (Low-active)
64	PF1_1	MNPS1-0C	I	Bypass unit slide guide width detection signal [1] (Low-active)
65	PF0_1	MNPS0-0C	I	Bypass unit slide guide width detection signal [0] (Low-active)
66	VSS5	SG	-	Signal ground
67	LVDD2	+3.3VB	-	+3.3VB
68	PG7_1	CS2PCL-0C	O	2nd drawer feed clutch ON/OFF signal (L: ON)
69	PG6_1	CS1PCL-0C	O	1st drawer feed clutch ON/OFF signal (L: ON)
70	PG5_1	CS1TUMB-1C	O	Tray-up motor control signal [2]
71	PG4_1	CS1TUMA-0C	O	Tray-up motor control signal [1] CS1TUMB-1C / CS1TUMA-0C / Status L / L / OFF L / H / CCW (1st) H / L / CW (2nd) H / H / Brake
72	PG3_1	MDT2CLL-0C	O	2nd drawer transport clutch (Low speed) ON/OFF signal (L: ON)
73	PG2_1	MDT2CLH-0C	O	2nd drawer transport clutch (High speed) ON/OFF signal (L: ON)
74	PG1_1	MDT1CLL-0C	O	1st drawer transport clutch (Low speed) ON/OFF signal (L: ON)
75	PG0_1	MDT1CLH-0C	O	1st drawer transport clutch (High speed) ON/OFF signal (L: ON)
76	HVDD2-4	+5.1VB	-	+5.1VB
77	PH7_1	CS2TL-1C	I	2nd drawer tray-up sensor detection signal (H: top position, L: normal)
78	PH6_1	CS1TL-1C	I	1st drawer tray-up sensor detection signal (H: top position, L: normal)

Pin No.	Port name	Signal name	I/O	Function
79	PH5_1	CS2PNEM-1C	I	2nd drawer paper stock sensor detection signal (H: no paper, L: paper presence)
80	PH4_1	CS1PNEM-1C	I	1st drawer paper stock sensor detection signal (H: no paper, L: paper presence)
81	PH3_1	CS2PS-0C	I	2nd drawer detection switch detection signal (H: drawer open, L: drawer closed)
82	PH2_1	CS1PS-0C	I	1st drawer detection switch detection signal (H: drawer open, L: drawer closed)
83	PH1_1	CS2PEM-1C	I	2nd drawer empty sensor detection signal (H: no paper, L: paper presence)
84	PH0_1	CS1PEM-1C	I	1st drawer empty sensor detection signal (H: no paper, L: paper presence)
85	VSS6	SG	-	Signal ground
86	PI7_1	FDMGA-0C	O	Feed/transport motor speed switching signal (H: high speed drive, L: low speed drive)
87	PI6_1	FDMBK-0C	O	Feed/transport motor brake signal (L: brake)
88	PI5_1	FDMON-0C	O	Feed/transport motor ON/OFF signal (L: ON)
89	PI4_1	GASOL-0C	O	Bridge unit gate solenoid driving signal (H: OFF (to finisher), L: ON (to inner receiving tray))
90	PI3_1	HTRFNL-0C	O	Fuser/exit section cooling fan low speed driving signal
91	PI2_1	HTRFNH-0C	O	Fuser/exit section cooling fan high speed driving signal HTRFNH-0C HTRFNL-0C Status L L Not used L H High speed drive H L Low speed drive H H Stop
92	PI1_1	LUSTMB-0C	O	Shutter motor control signal [2]
93	PI0_1	LUSTMA-0C	O	Shutter motor control signal [1] LUSTMB-0C LUSTMA-0C Status L L OFF L H Shutter opened H L Shutter closed H H Brake
94	PJ7_1	HVTSTS-1C	I	High voltage transformer leak detection signal (L: error)
95	PJ6_1	THCNT-1CA	I	Pressure roller thermistor connection signal (H: connected)
96	PJ5_1	FUSCRU-0C	I	Fuser unit use status determining signal (H: Used, L: New)
97	PJ4_1	RLC2S-0C	I	Bridge unit exit sensor detection signal (H: paper being transported, L: normal)
98	PJ3_1	RLCSW-0C	I	Bridge unit transport cover opening/closing sensor detection signal (H: cover open, L: cover closed)
99	PJ2_1	RLTRS-0C	I	Bridge unit intermediary transport sensor detection signal (H: paper being transported, L: normal)

Pin No.	Port name	Signal name	I/O	Function
100	PJ1_1	RLHSW-0C	I	Bridge unit load-full sensor detection signal (H: full, L: normal)
101	PJ0_1	RLCNT-0C	I	Bridge unit connection signal (L: connected)
102	HVDD2-5	+5.1VB	-	+5.1VB
103	VSS7	SG	-	Signal ground
104	PK7_1	HVTECC-0C	O	Cleaner bias-Y/M/C ON/OFF signal (L: ON)
105	PK6_1	HVTECK-0C	O	Cleaner bias-K ON/OFF signal (L: ON)
106	PK5_1	TR2IV-0C	O	2nd transfer bias control switching signal (H: constant voltage control, L: constant current control)
107	PK4_1	HVTTR2-0C	O	2nd transfer bias ON/OFF signal (L: ON)
108	PK3_1	HVTTR1C-0C	O	1st transfer bias-C ON/OFF signal (L: ON)
109	PK2_1	HVTTR1M-0C	O	1st transfer bias-M ON/OFF signal (L: ON)
110	PK1_1	HVTTR1Y-0C	O	1st transfer bias-Y ON/OFF signal (L: ON)
111	PK0_1	HVTTR1K-0C	O	1st transfer bias-K ON/OFF signal (L: ON)
112	LVDD3	+3.3VB	-	+3.3VB
113	PL7_1	TR1CC-0C	O	1st transfer bias current setting signal
114	PL6_1	TR1IV-0C	O	1st transfer bias control switching signal (H: constant voltage control, L: constant current control)
115	PL5_1	HVTDACC-0C	O	Developer AC bias-Y/M/C ON/OFF signal (L: ON)
116	PL4_1	HVTDACK-0C	O	Developer AC bias-K ON/OFF signal (L: ON)
117	PL3_1	HVTDDCC-0C	O	Developer DC bias-Y/M/C ON/OFF signal (L: ON)
118	PL2_1	HVTDDCK-0C	O	Developer DC bias-K ON/OFF signal (L: ON)
119	PL1_1	HVTMC-0C	O	Charger bias-Y/M/C ON/OFF signal (L: ON)
120	PL0_1	HVTMK-0C	O	Charger bias-K ON/OFF signal (L: ON)
121	VSS8	SG	-	Signal ground
122	PM7_1	DVMDIR-0C	O	Developer motor rotational direction switching signal (H: CCW, L: CW)
123	PM6_1	FUSCUT-0C	O	Fuser unit fuse blow-out signal (L: fusing)
124	PM5_1	DVMGA-0C	O	Developer motor speed switching signal (H: high speed drive, L: low speed drive)
125	PM4_1	FSMGA-0C	O	Fuser motor speed switching signal (H: high speed drive, L: low speed drive)
126	PM3_1	DVMBK-0C	O	Developer motor brake signal (L: brake)
127	PM2_1	FSMBK-0C	O	Fuser motor brake signal (L: brake)
128	PM1_1	DVMON-0C	O	Developer motor ON/OFF signal (L: ON)
129	PM0_1	FSMON-0C	O	Fuser motor ON/OFF signal (L: ON)
130	HVDD2-6	+5.1VB	-	+5.1VB
131	PN7_1	DVMRDY-1C	I	Developer motor ready signal (L: ready)

Pin No.	Port name	Signal name	I/O	Function
132	PN6_1	FSMRDY-1C	I	Fuser motor ready signal (L: ready)
133	PN5_1	FDMRDY-1C	I	Feed/transport motor ready signal (L: ready)
134	PN4_1	2TRCOV-0C	I	Transfer cover switch detection signal (H: cover open, L: cover closed)
135	PN3_1	KCRGSW-0C	I	Toner cartridge detection sensor-K detection signal
136	PN2_1	CCRGSW-0C	I	Toner cartridge detection sensor-C detection signal
137	PN1_1	MCRGSW-0C	I	Toner cartridge detection sensor-M detection signal
138	PN0_1	YCRGSW-0C	I	Toner cartridge detection sensor-Y detection signal
139	VSS9	SG	-	Signal ground
140	PO7_1	-	-	-
141	PO6_1	-	-	-
142	PO5_1	CKMMB-1C	O	Drum switching motor control signal [2]
143	PO4_1	CKMMA-0C	O	Drum switching motor control signal [1] CKMMB-1C CKMMA-0C Status L L OFF L H Y/M/C/K drive H L K drive H H Brake
144	PO3_1	KTNMT-0C	O	Toner motor-K ON/OFF signal (L: ON)
145	PO2_1	CTNMT-0C	O	Toner motor-C ON/OFF signal (L: ON)
146	PO1_1	MTNMT-0C	O	Toner motor-M ON/OFF signal (L: ON)
147	PO0_1	YTNMT-0C	O	Toner motor-Y ON/OFF signal (L: ON)
148	HVDD2-7	+5.1VB	-	+5.1VB
149	PP7_1	FAN2L-0C	-	Not used
150	PP6_1	FAN2H-0C	-	Not used
151	PP5_1	-	-	Not used
152	PP4_1	-	-	Not used
153	PP3_1	CGFANL-0	O	Internal cooling fan low speed driving signal
154	PP2_1	CGFANH-0	O	Internal cooling fan high speed driving signal CGFNH-0C CGFNL-0C Status L L Not used L H High speed drive H L Low speed drive H H Stop
155	PP1_1	PWFANL-0	O	Switching regulator cooling fan-1/2 low speed driving signal
156	PP0_1	PWFANH-0	O	Switching regulator cooling fan-1/2 high speed driving signal PWFANH-0C PWFANL-0C Status L L Not used L H High speed drive H L Low speed drive H H Stop

Pin No.	Port name	Signal name	I/O	Function
157	LVDD4	+3.3VB	-	+3.3VB
158	TST_1	TST1-1	-	Pull-down: signal ground
159	VSS10	SG	-	Signal ground
160	PQ7_1	-	-	Pull-up: +5.1VB
161	PQ6_1	CSTCV-0C	I	Side cover switch detection signal (H: cover open, L: cover closed)
162	PQ5_1	RSVI2-0	-	Not used
163	PQ4_1	-	-	Pull-up: +5.1VB
164	PQ3_1	CKMODE1-1C	I	Drum switching detection sensor detection signal (H: Y/M/C drive, L: Y/M/C stop)
165	PQ2_1	CTRCNT2-0C	-	Not used
166	PQ1_1	CTRON-0C	O	Coin controller count signal (H: normal, L: count)
167	PQ0_1	KCTRON-0C	O	Key copy counter count signal (H: normal, L: count)
168	HVDD2-8	+5.1VB	-	+5.1VB
169	CLK_1	SDCLK-1T	I	Bus control clock
170	RSTSE1	OPRSTSEL-0	I	Pull-down: signal ground
171	PR1_1	FUSCNT-1C	I	Fuser unit connection signal (L: connected)
172	PR0_1	KCTRC-0	I	External counter connection signal (L: connected)
173	HVDD1-2	+3.3VB	-	+3.3VB
174	RST_0	MRST-0T	I	Reset signal (Low-active)
175	VSS11	SG	-	Signal ground
176	A0	A[0]	I	Address bus [0]
177	A1	A[1]	I	Address bus [1]
178	A2	A[2]	I	Address bus [2]
179	A3	A[3]	I	Address bus [3]
180	A4	A[4]	I	Address bus [4]
181	CS_0	OPALCS-0T	I	Chip select signal (Low-active) * For ASIC (EC/N106)
182	RD_0	OPALRD-0T	I	Read signal (Low-active) * For ASIC (EC/N106)
183	HVDD1-3	+3.3VB	-	+3.3VB
184	WR_0	WR-0T	I	Write signal (Low-active)

3. ELECTRIC CIRCUIT DIAGRAMS

3.1	System control circuit (SYS board)	1/24 to 24/24
3.2	CODEC circuit (JSP board)	1/1
3.3	Logic circuit (LGC board)	1/43 to 43/43
3.4	Imaging processing circuit (IMG board)	1/23 to 23/23
3.5	Scanning section circuit (SLG board)	1/18 to 18/18
3.6	CCD driving circuit (CCD board)	1/5 to 5/5
3.7	ADU driving circuit (ADU board)	1/2 to 2/2
3.8	Display circuit (DSP board)	1/1
3.9	Key control circuit (KEY board)	1/1
3.10	Filter circuit (FIL board)	1/1
3.11	Facsimile circuit (FAX board: GD-1210)	1/14 to 14/14
3.12	Facsimile power supply circuit (FAX PWR board: GD-1210)	1/1
3.13	Modem circuit (MDM board: GD-1160)	1/4 to 4/4
3.14	Telephone line network control circuit (NCU board: GD-1210NA/TW / GD-1160NA/TW)	1/2 to 2/2
3.15	Telephone line network control circuit (NCU board: GD-1210EU/AU/AS/ C/KR / GD-1160EU-N/C)	1/2 to 2/2

3.1 System control circuit (SYS board)

SYS board 1/24

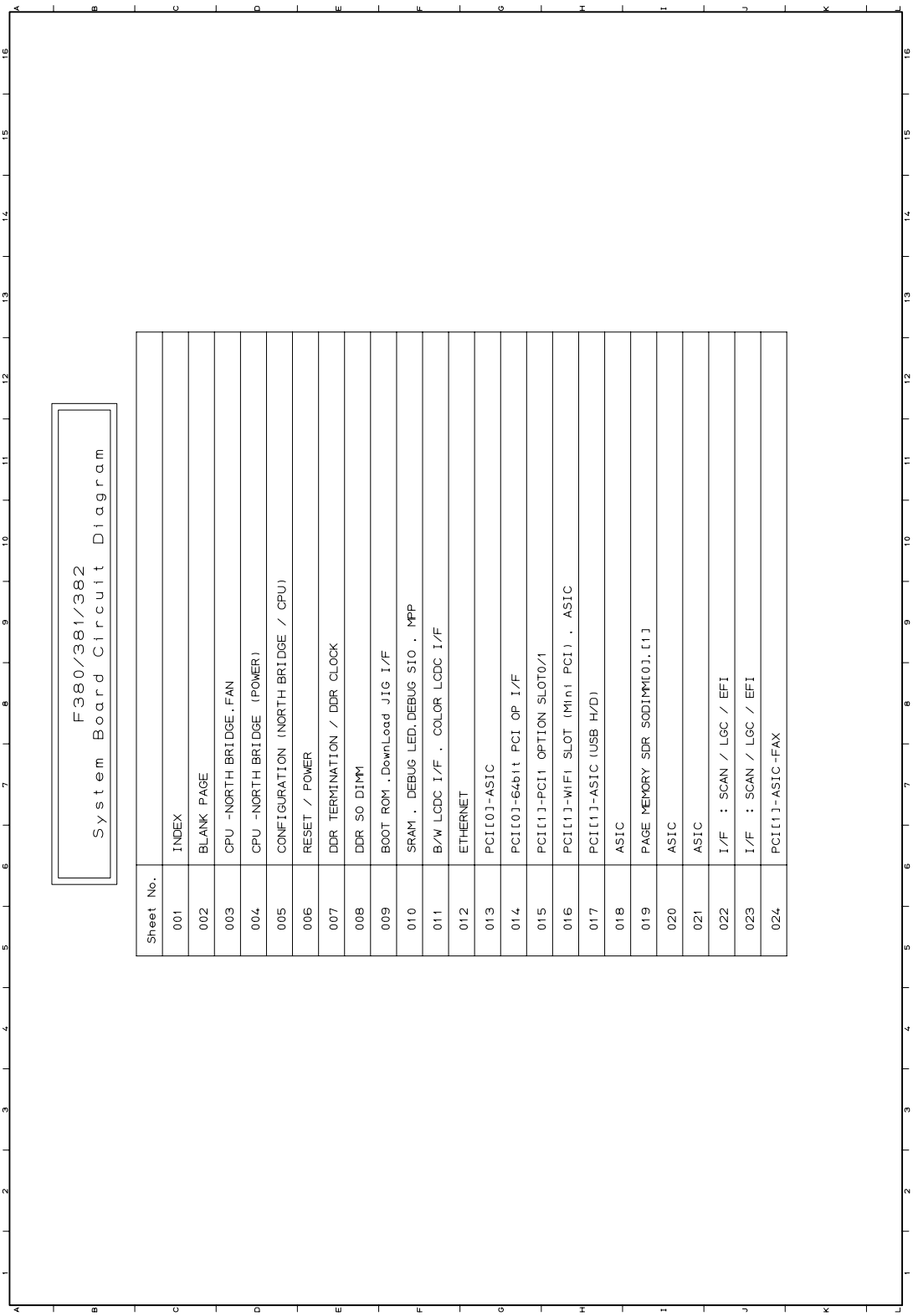

Fig. 3-1

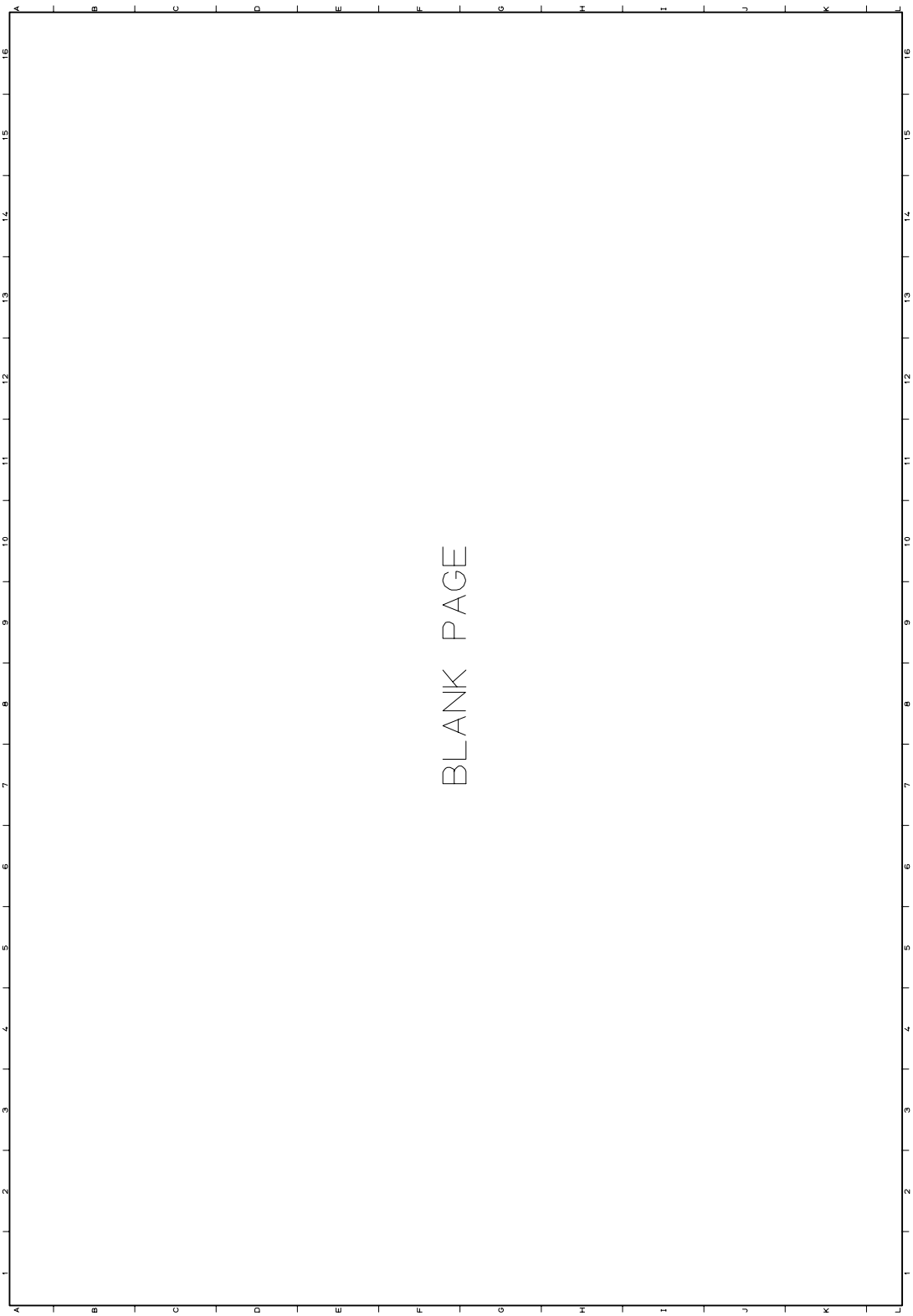

Fig. 3-2

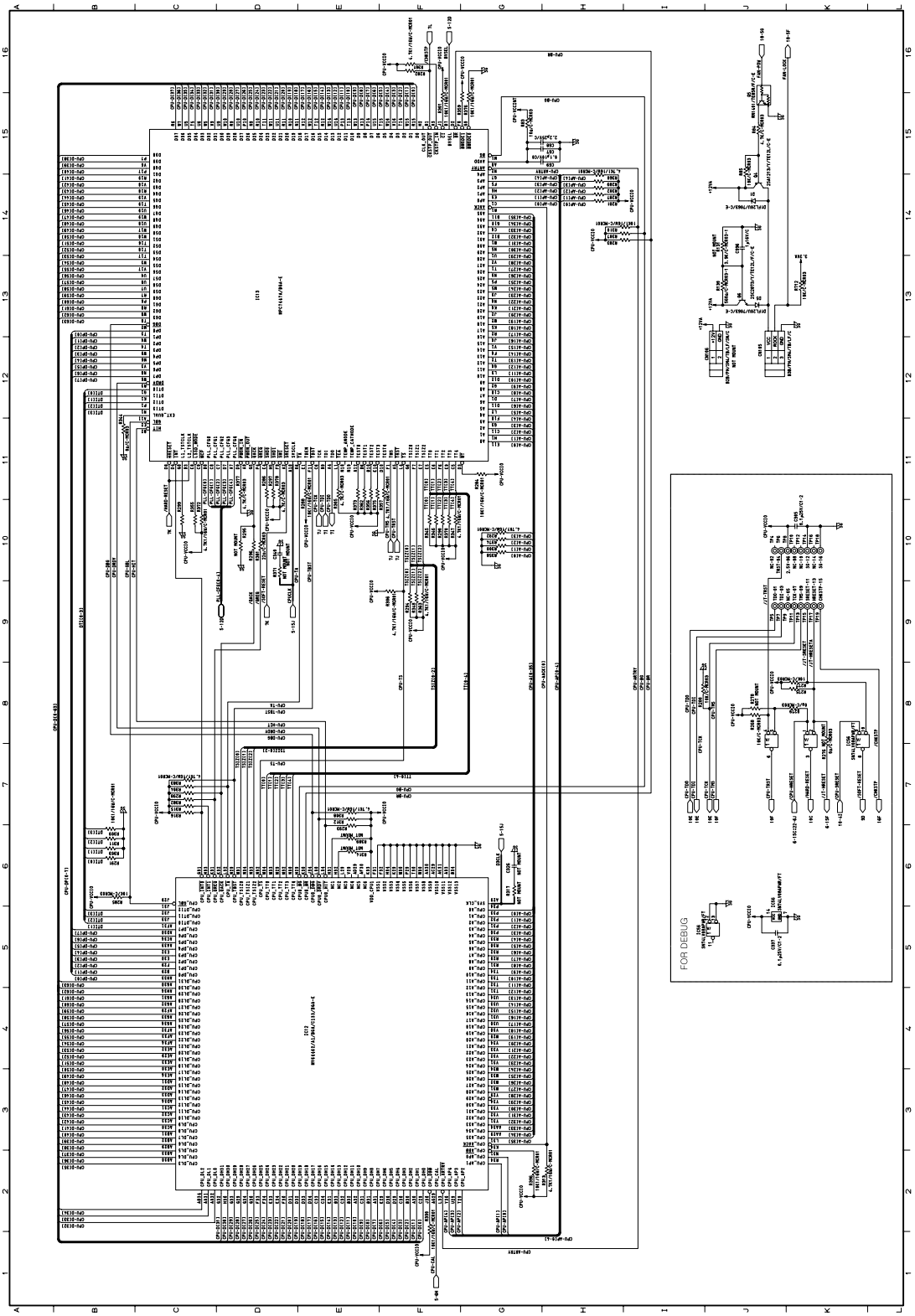

Fig. 3-3

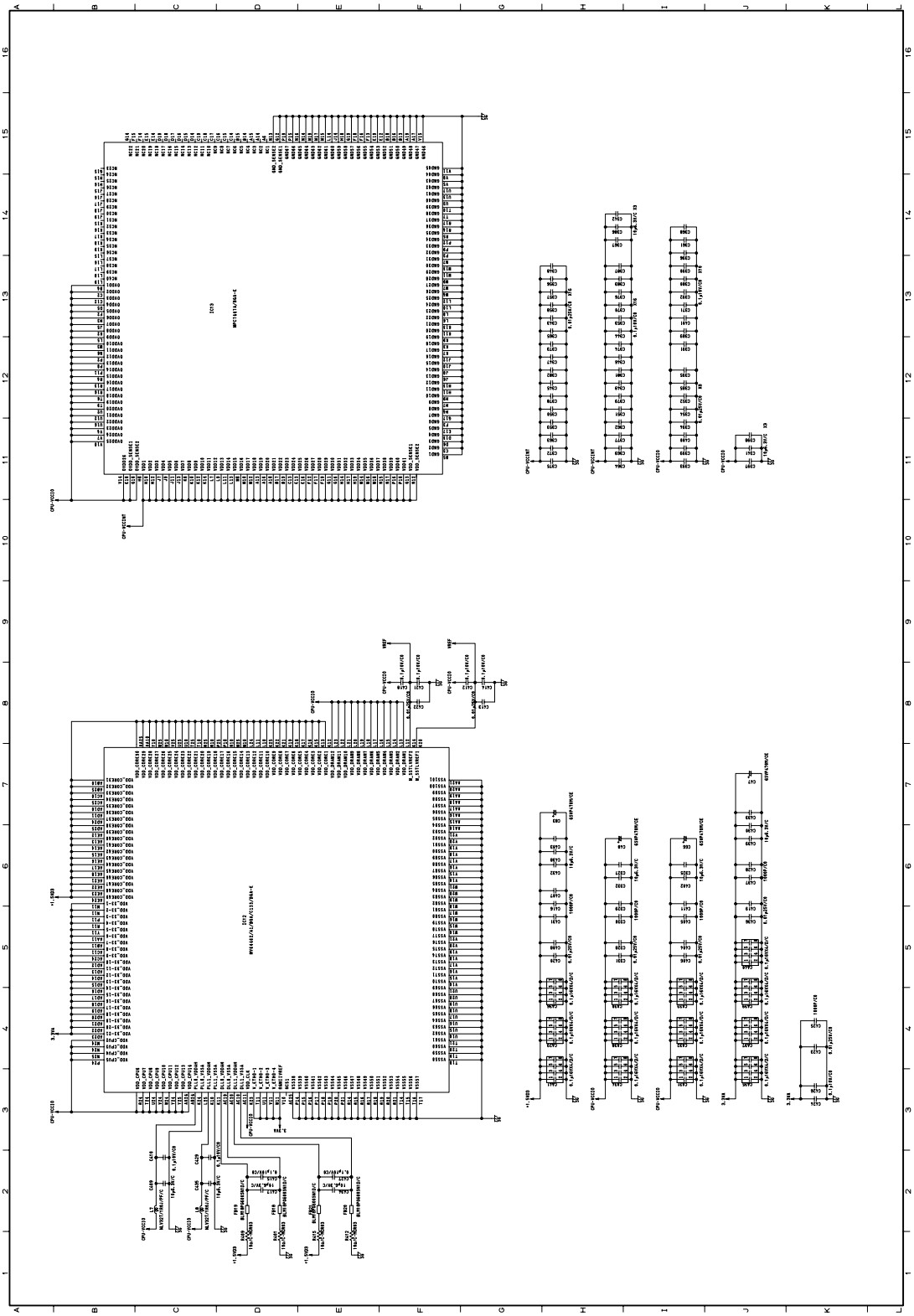

Fig. 3-4

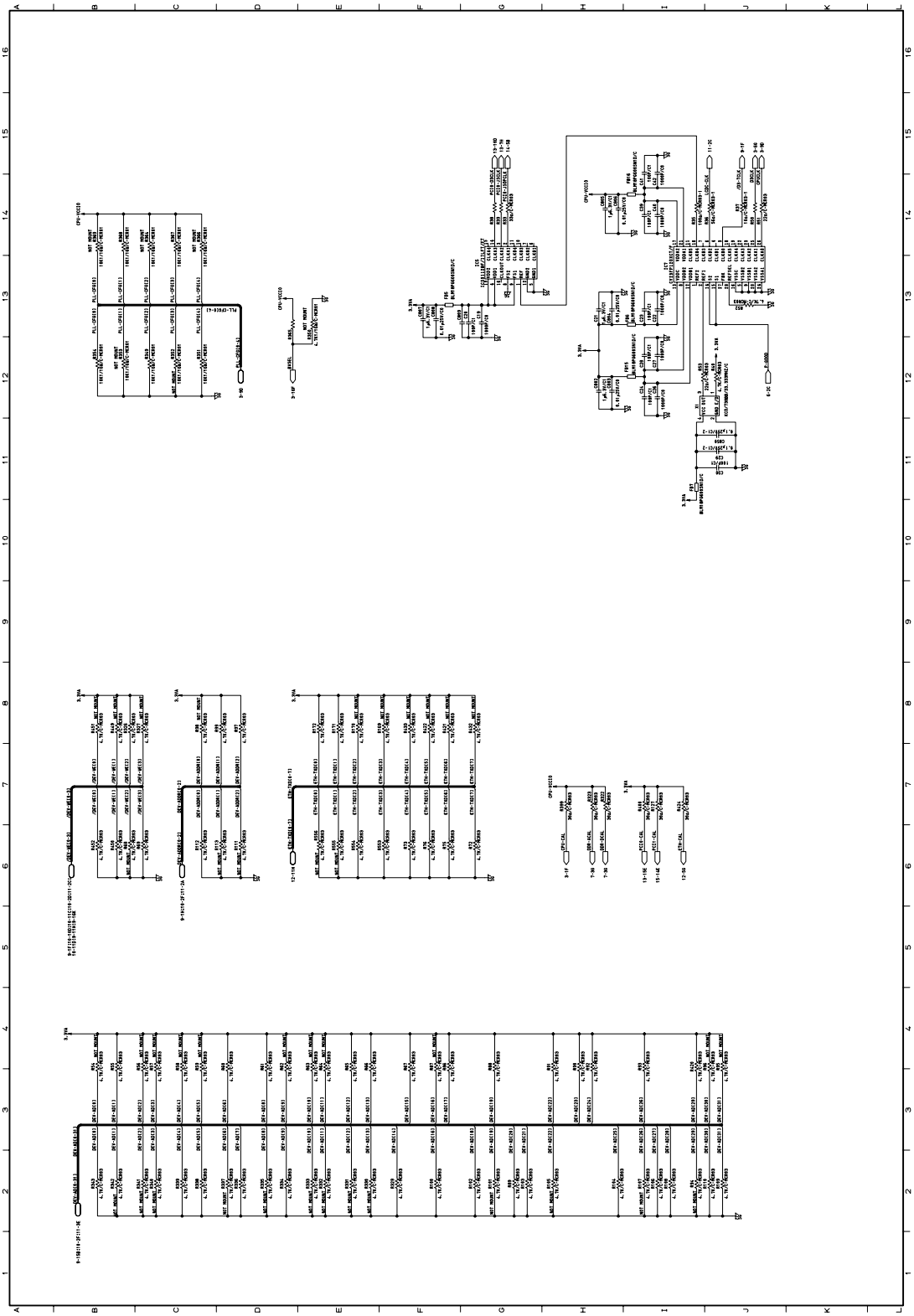

Fig. 3-5

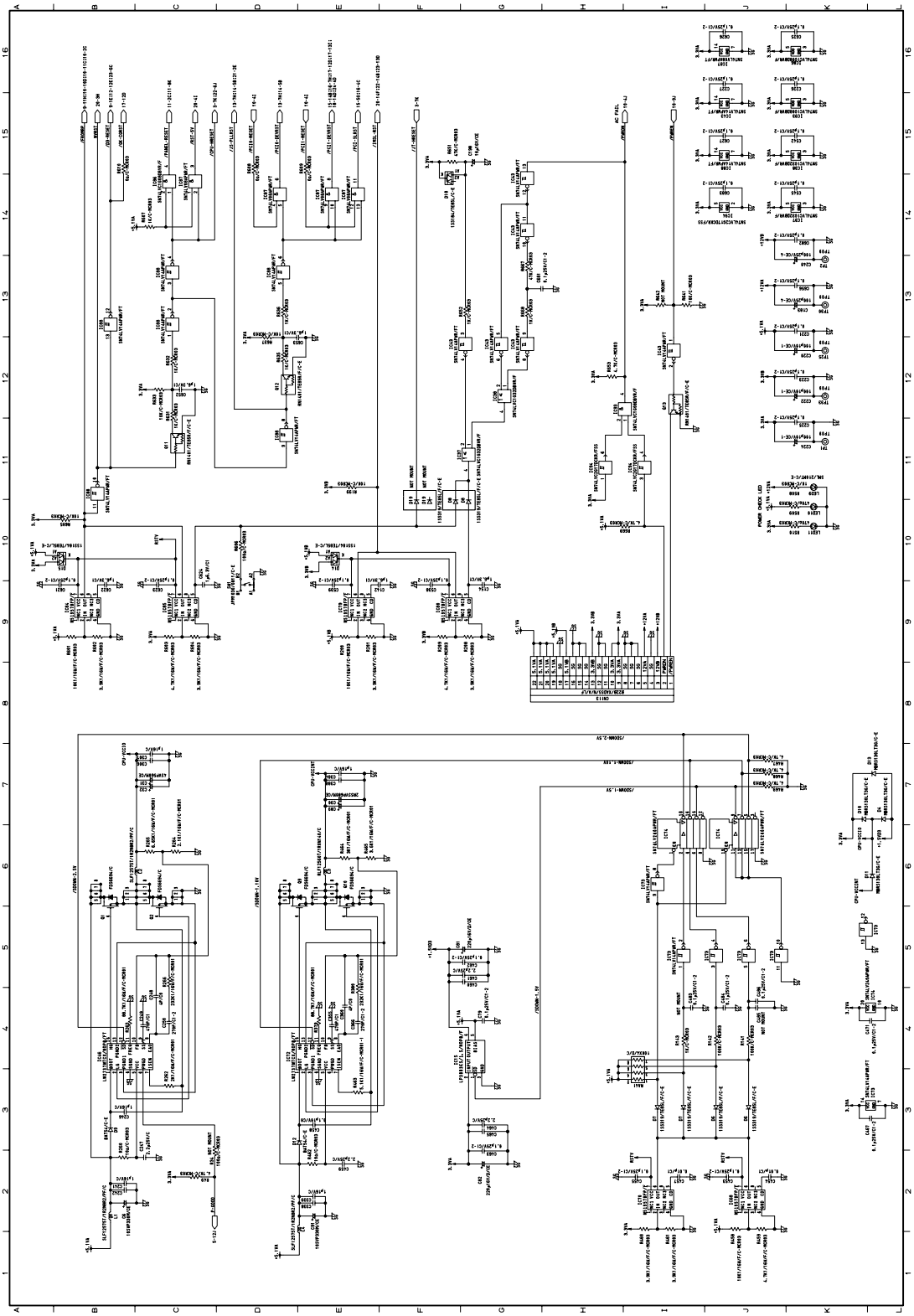

Fig. 3-6

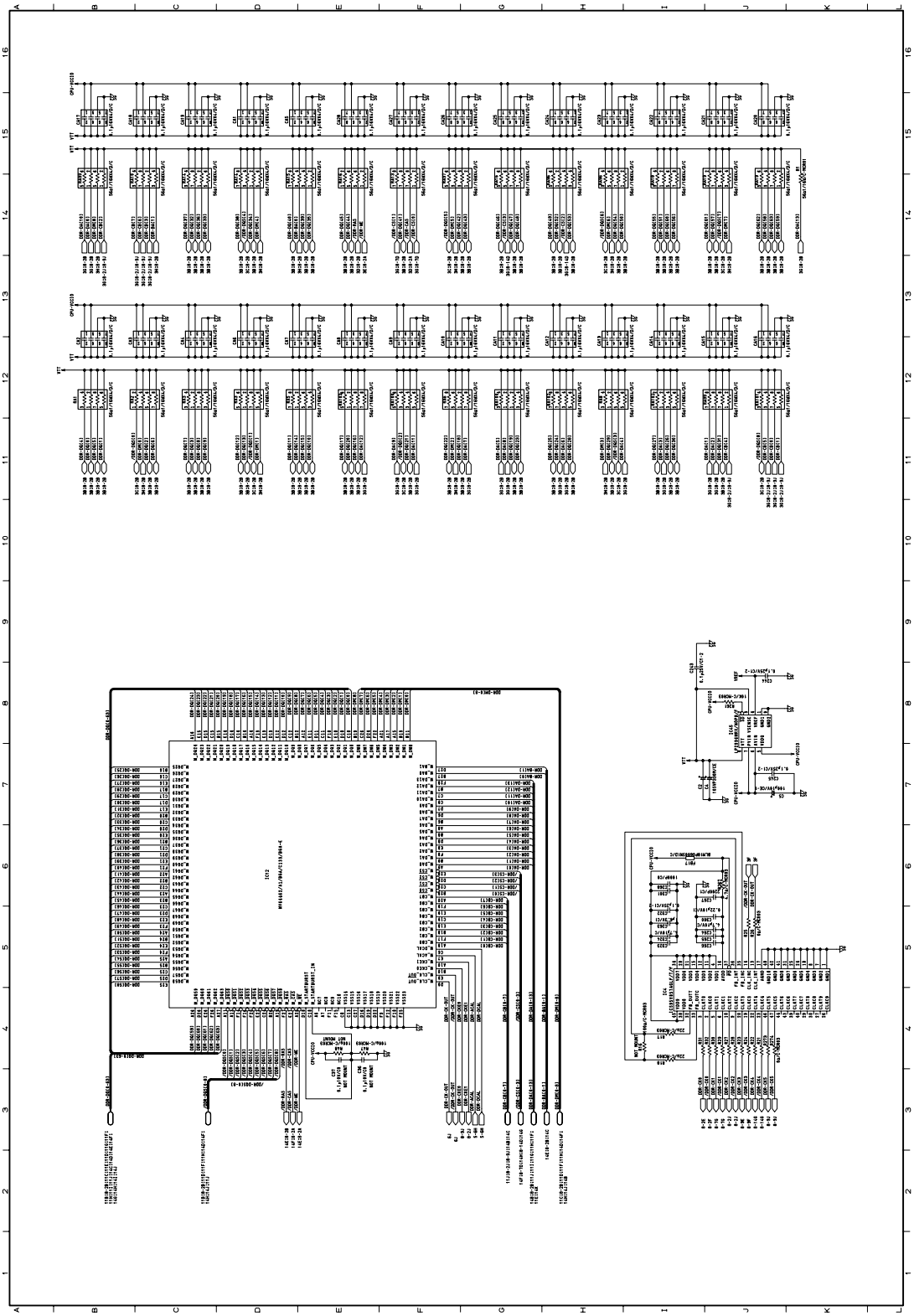

Fig. 3-7

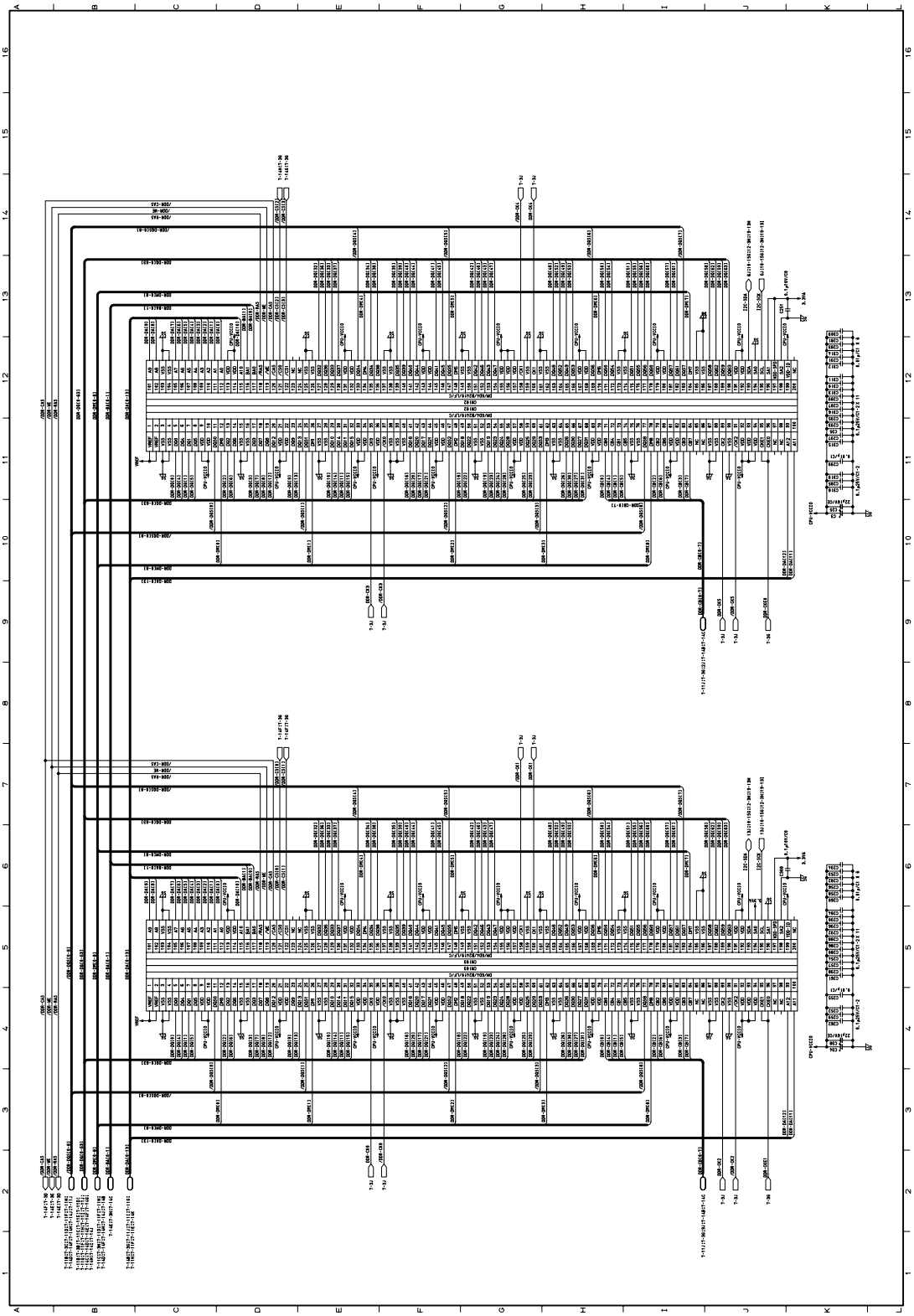

Fig. 3-8

SYS board 9/24

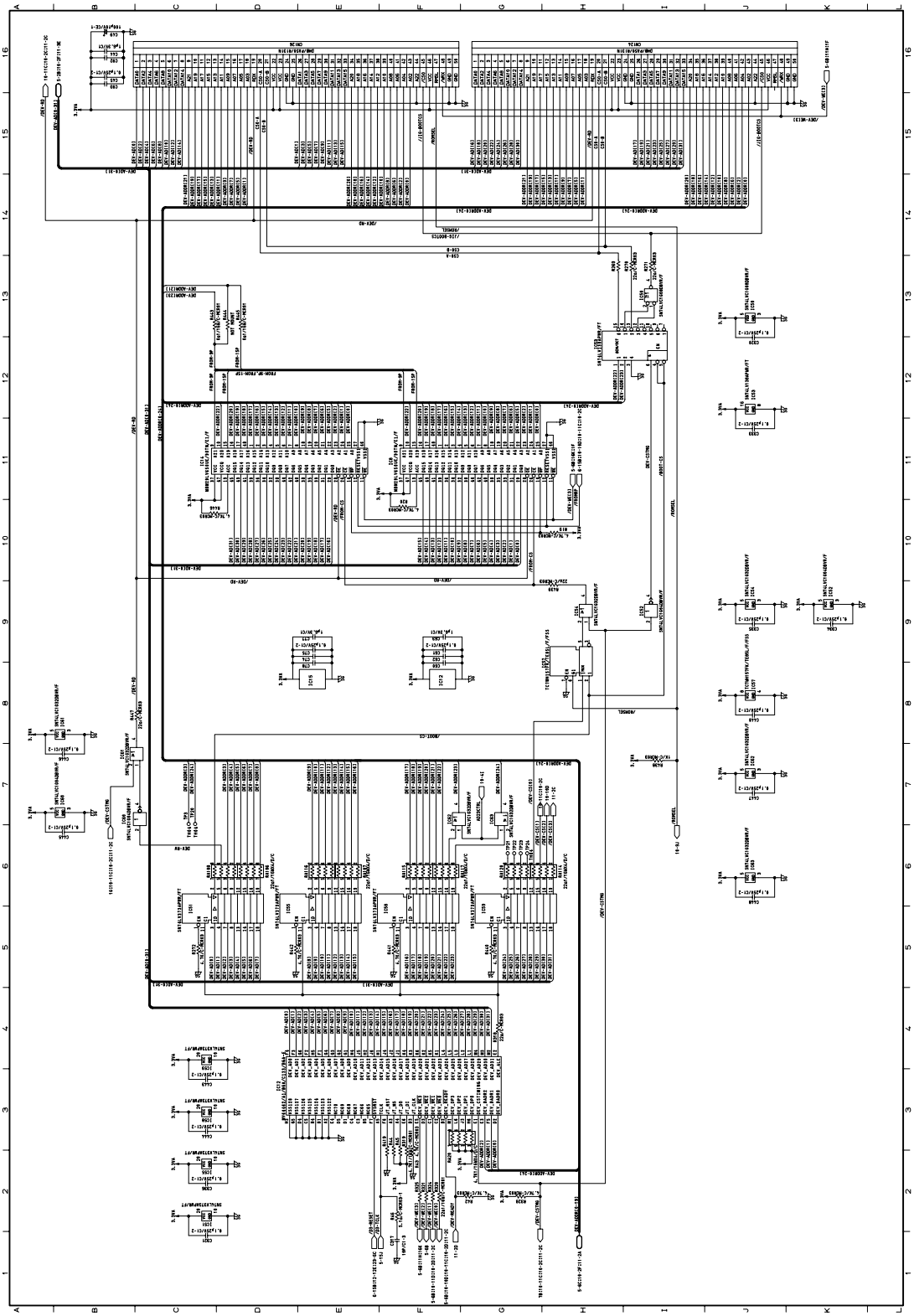

Fig. 3-9

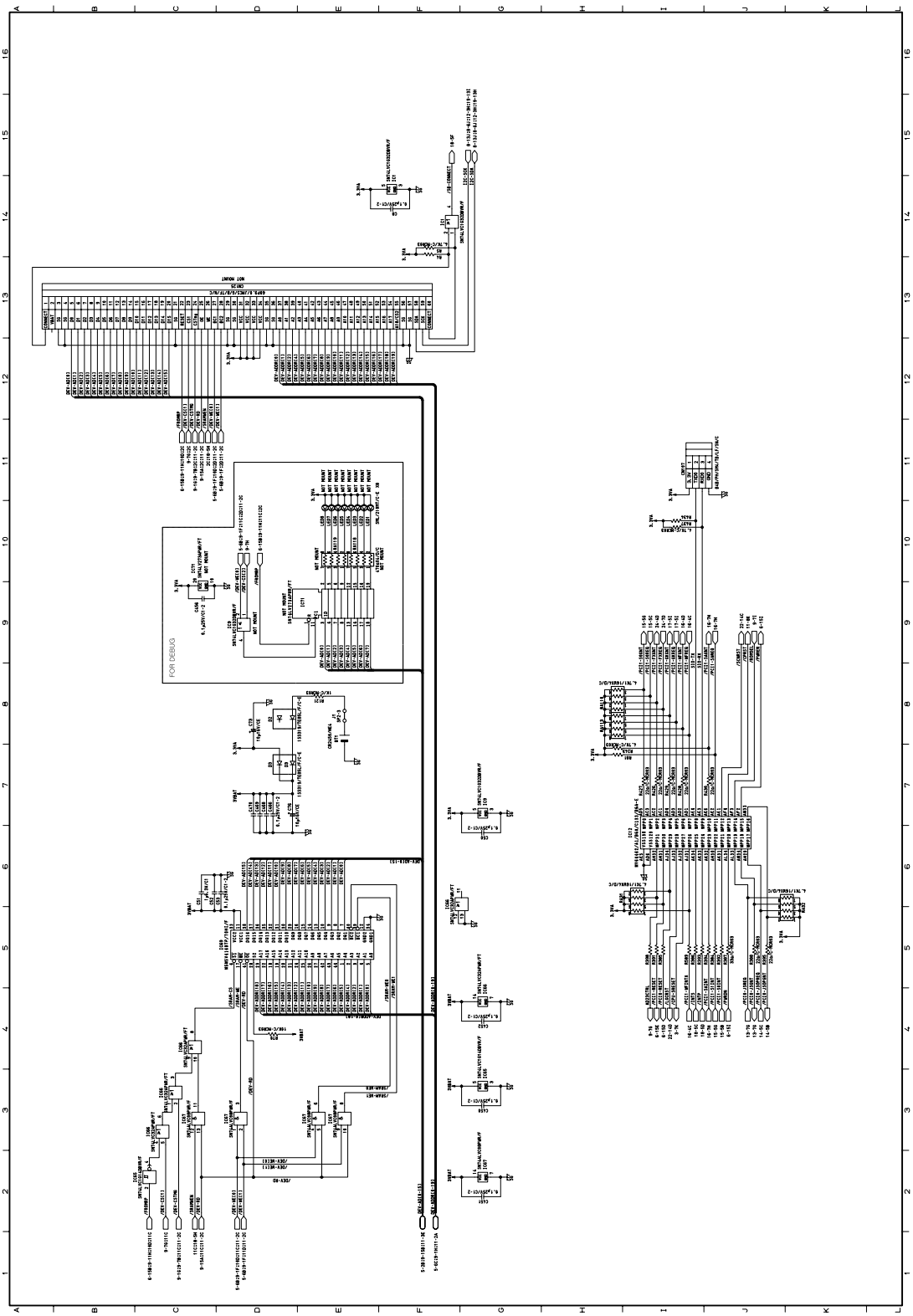

Fig. 3-10

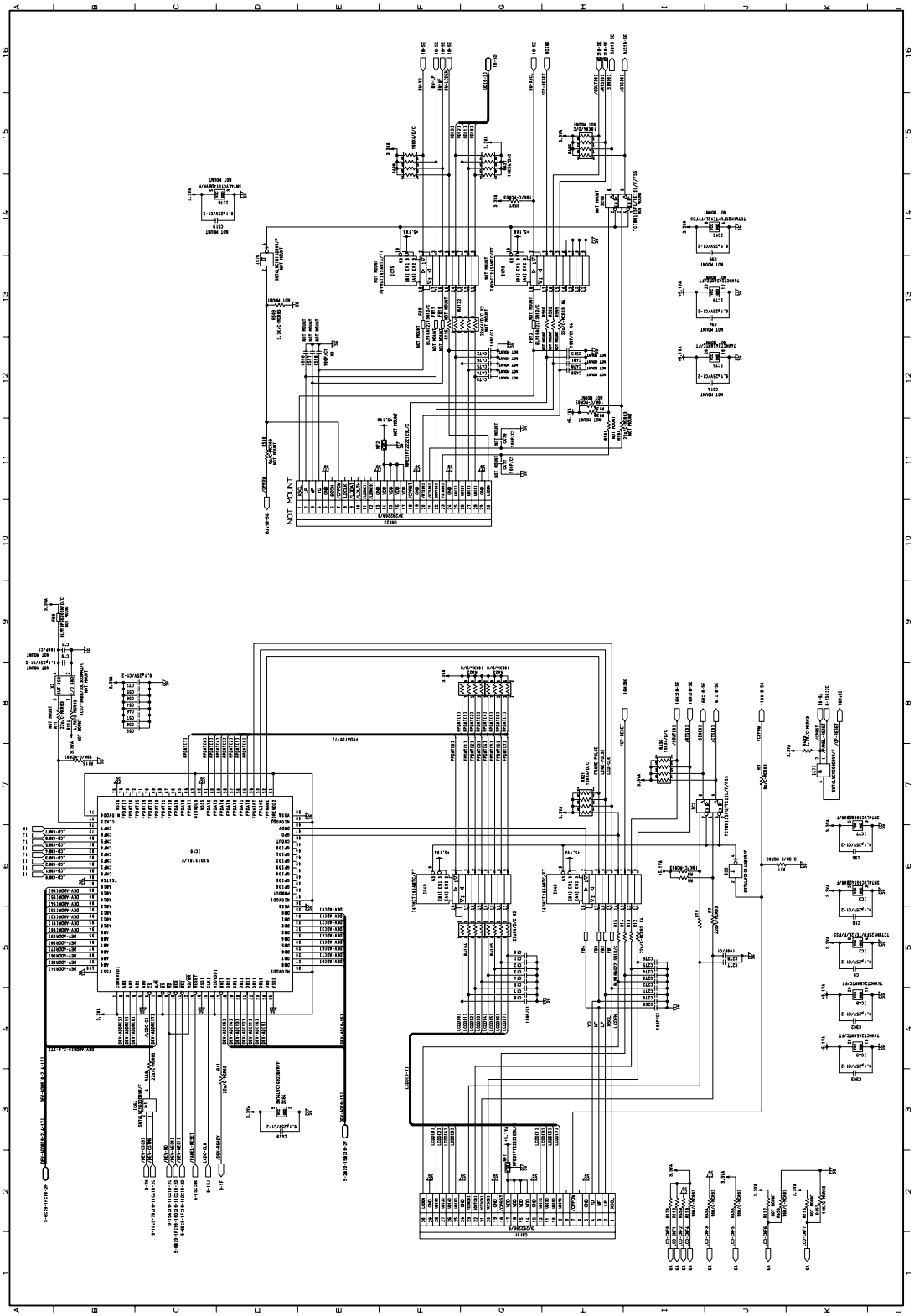

Fig. 3-11

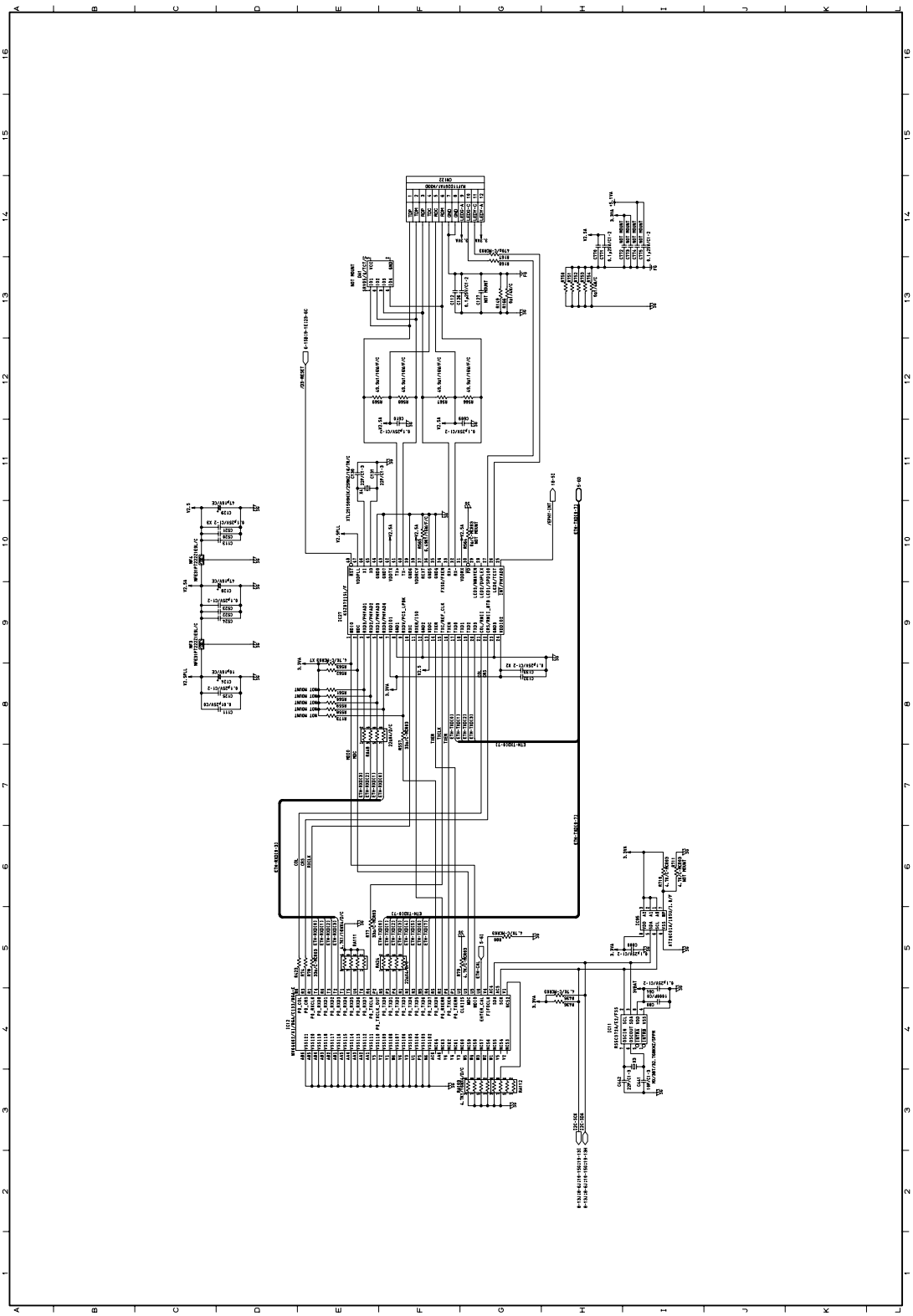

Fig. 3-12

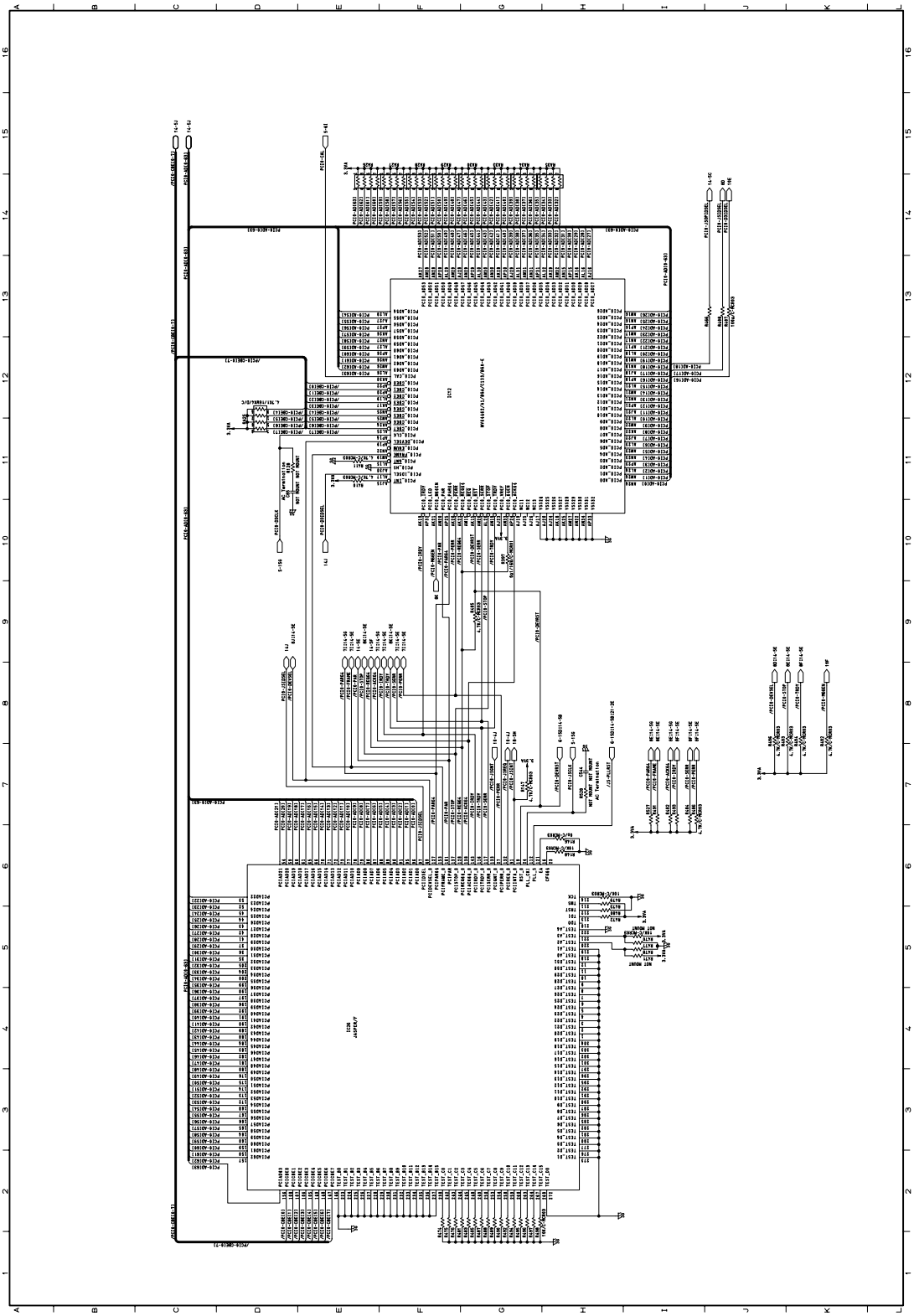

Fig. 3-13

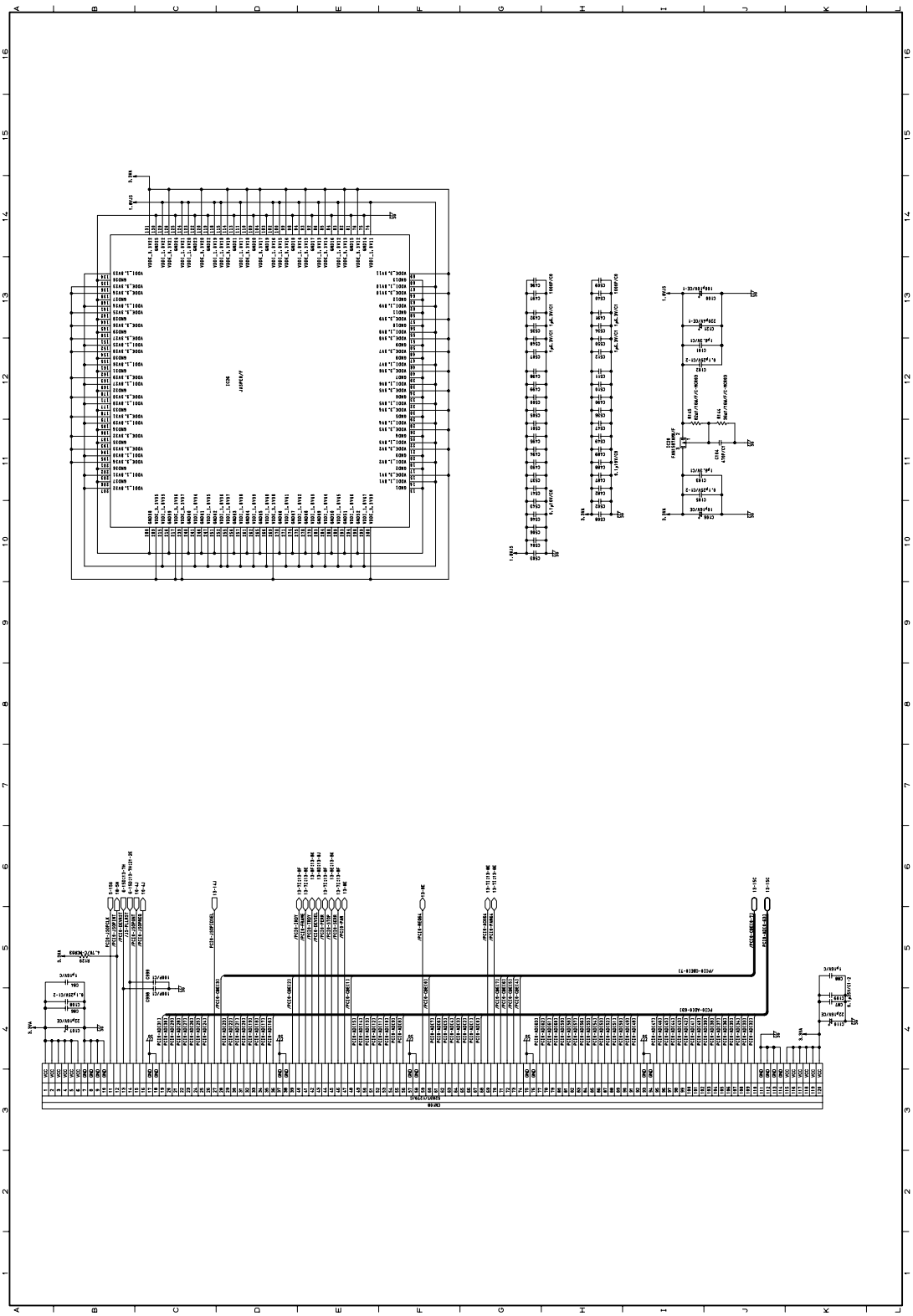

Fig. 3-14

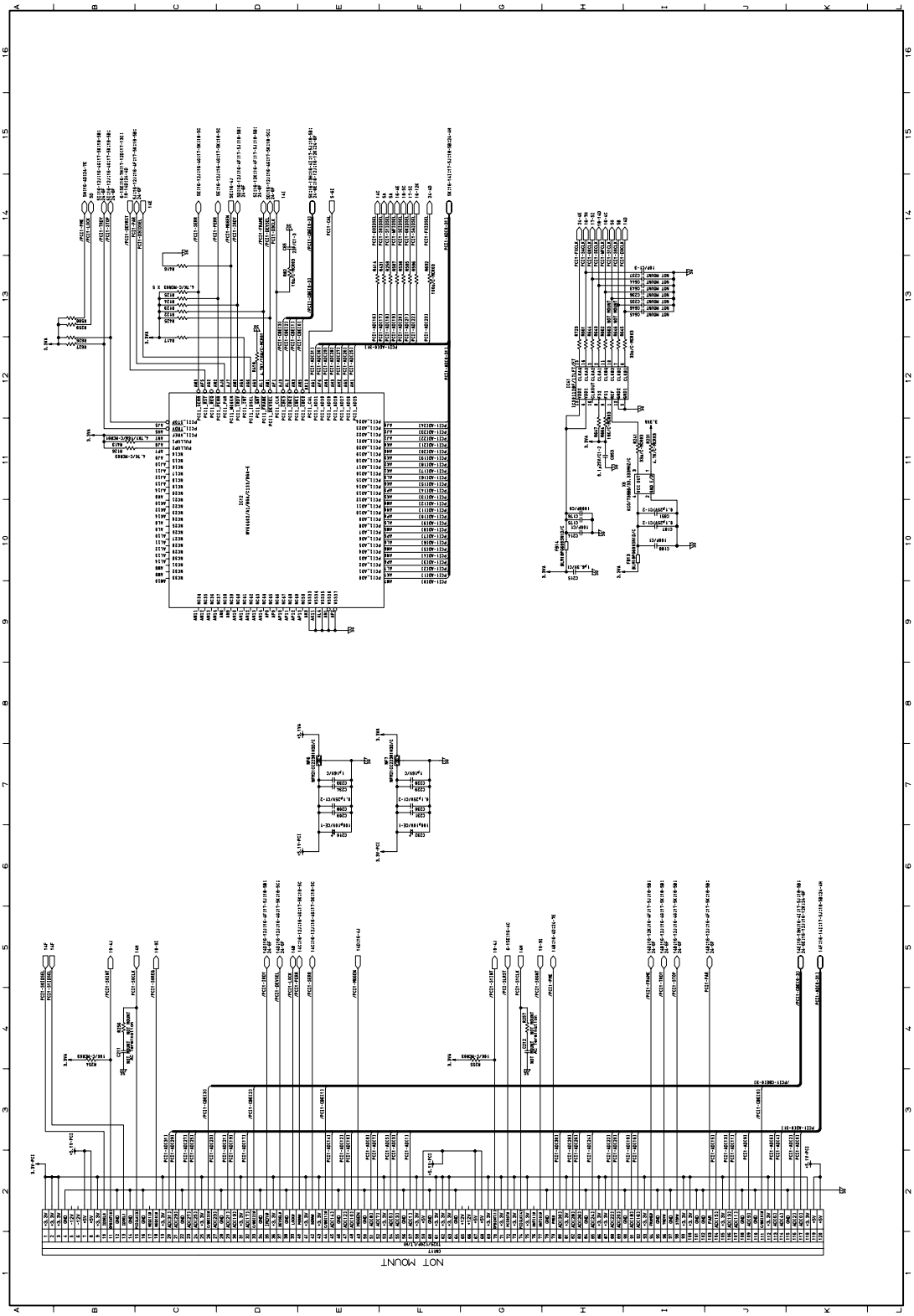

Fig. 3-15

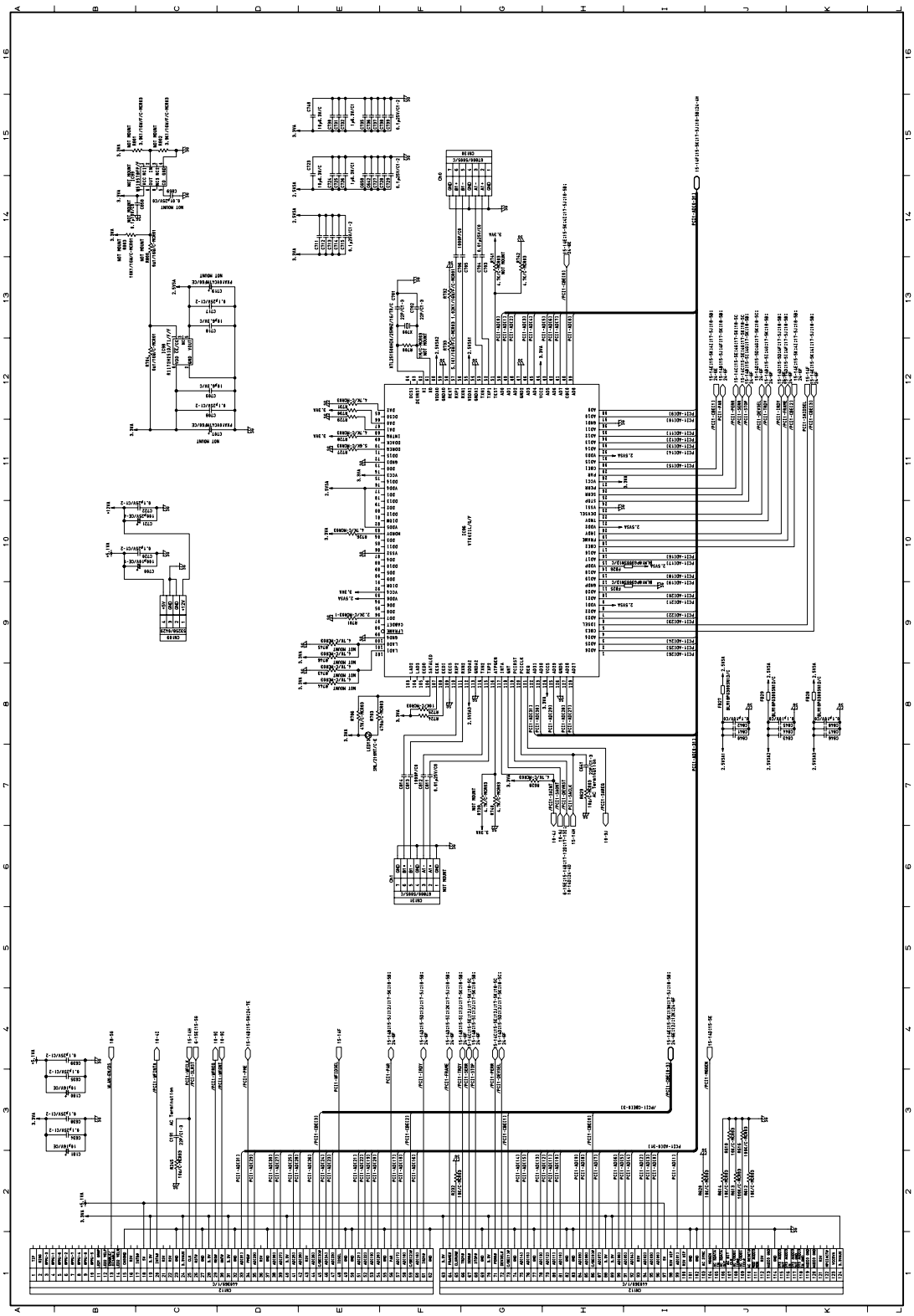

Fig. 3-16

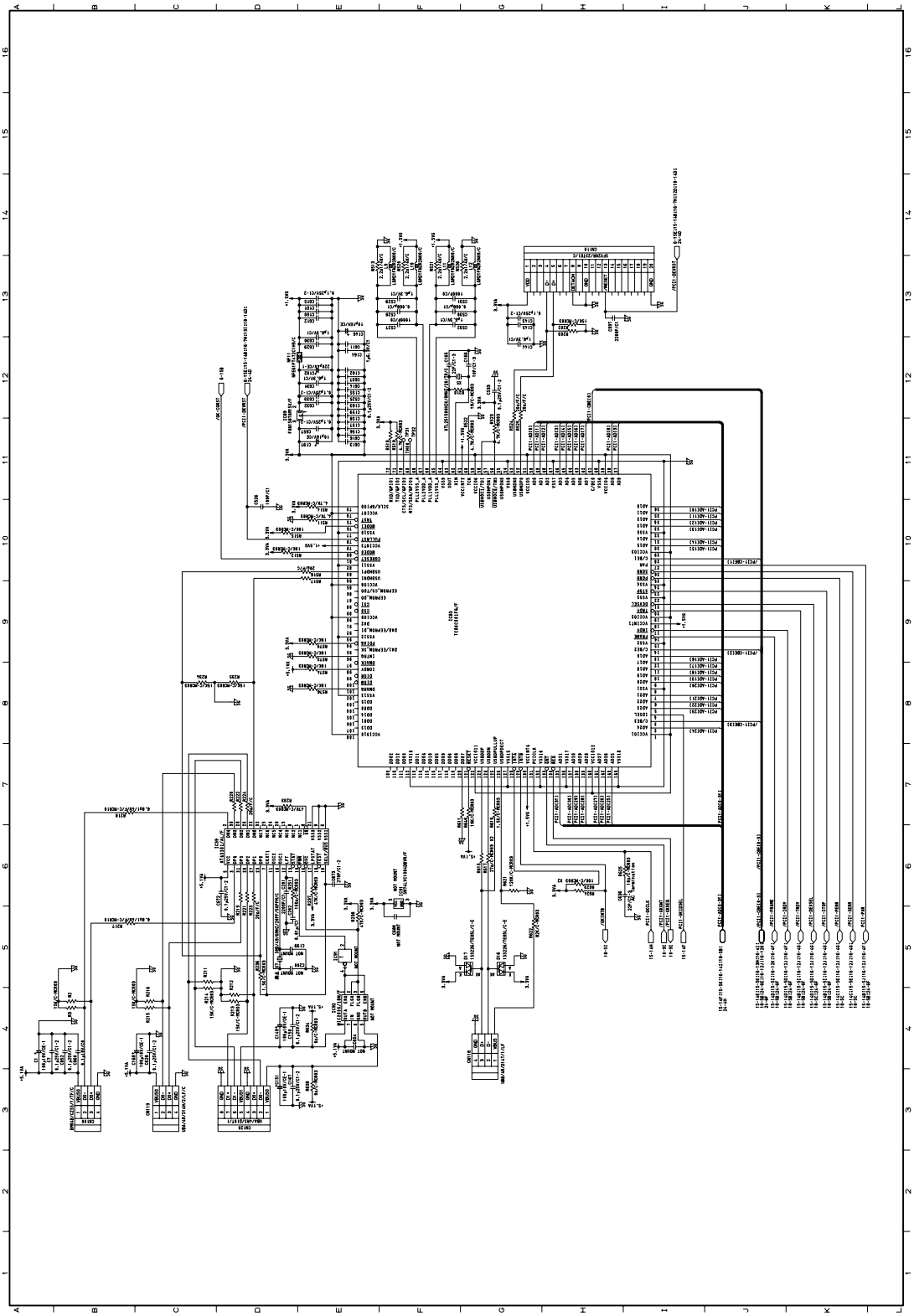

Fig. 3-17

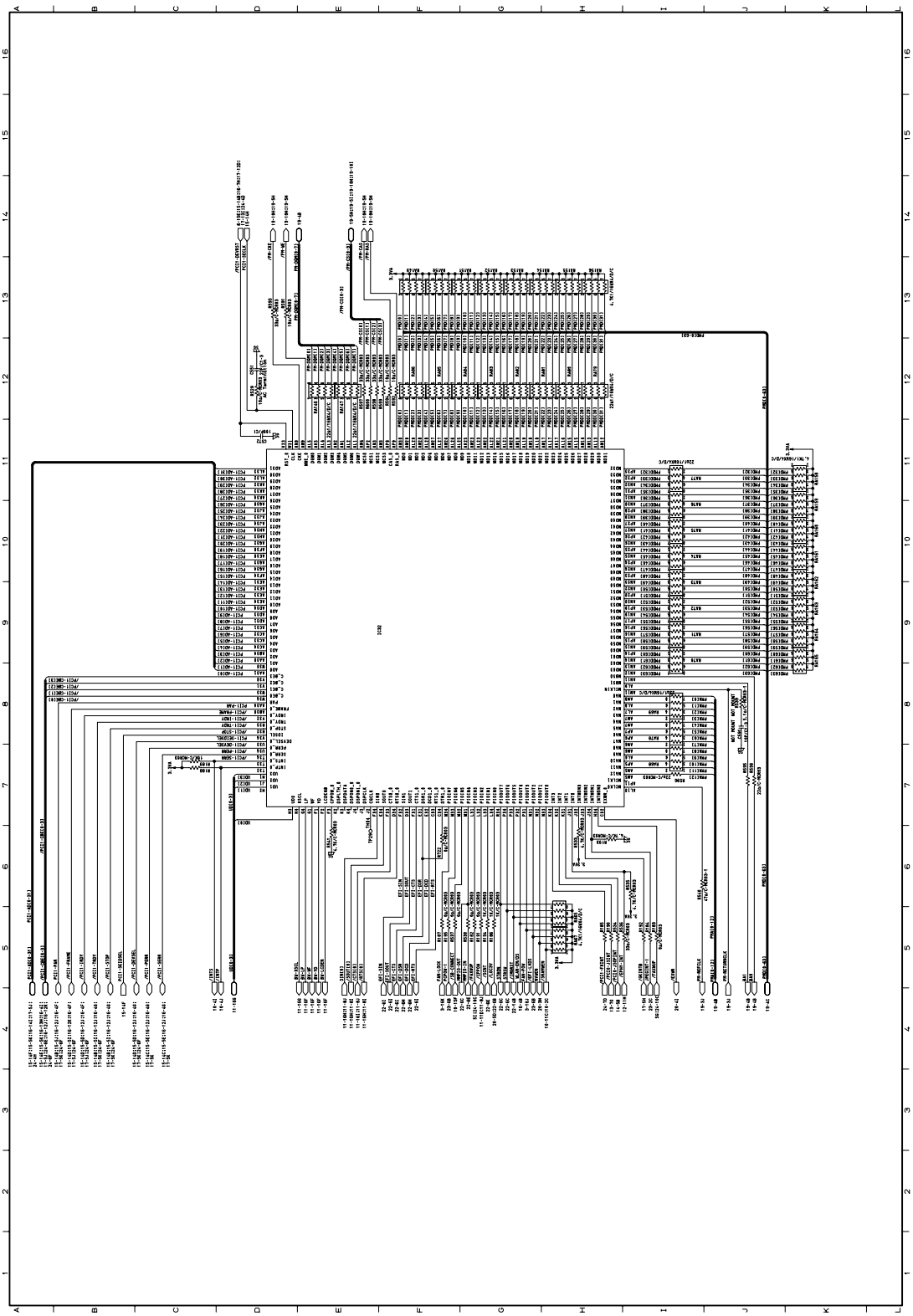

Fig. 3-18

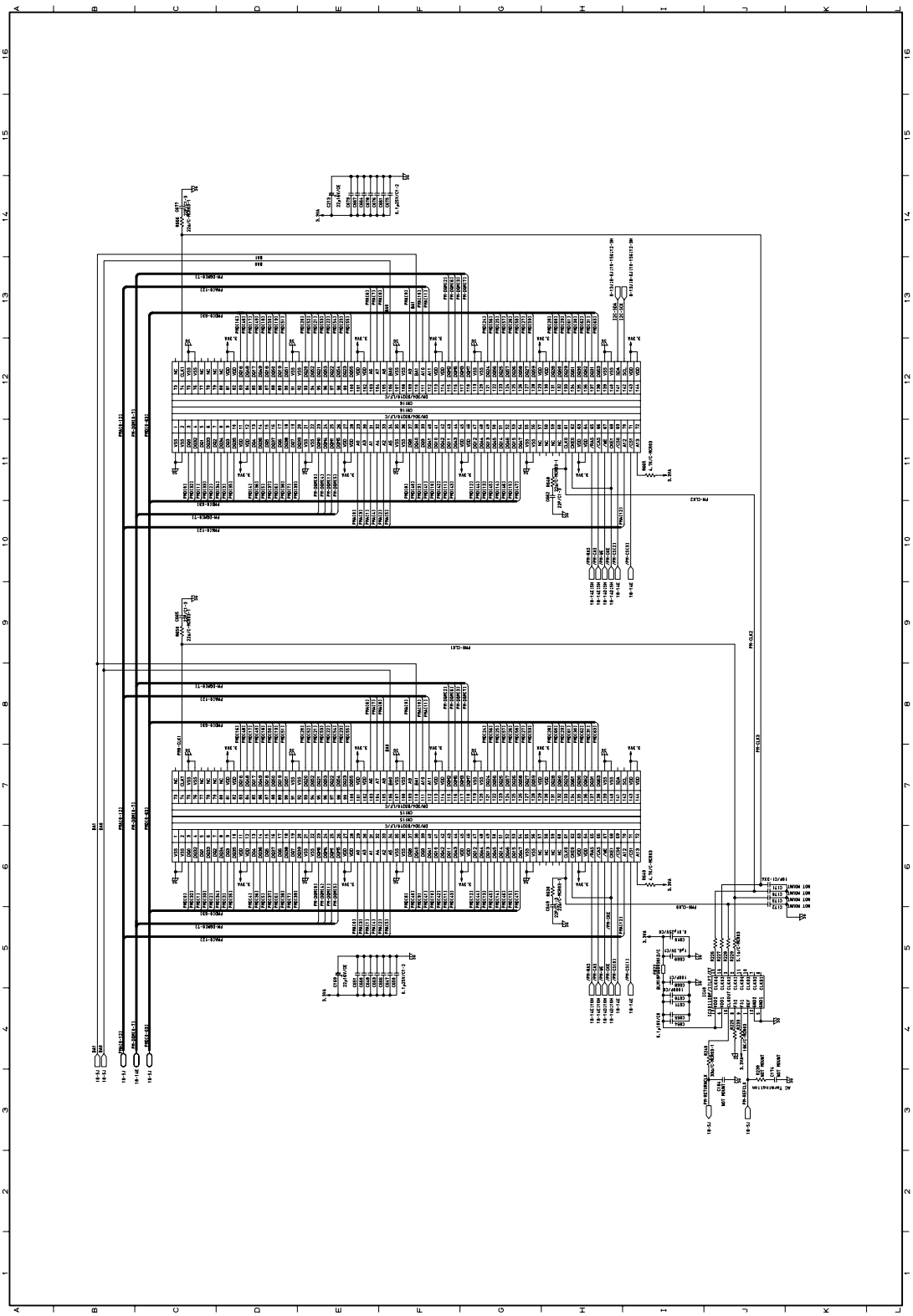

Fig. 3-19

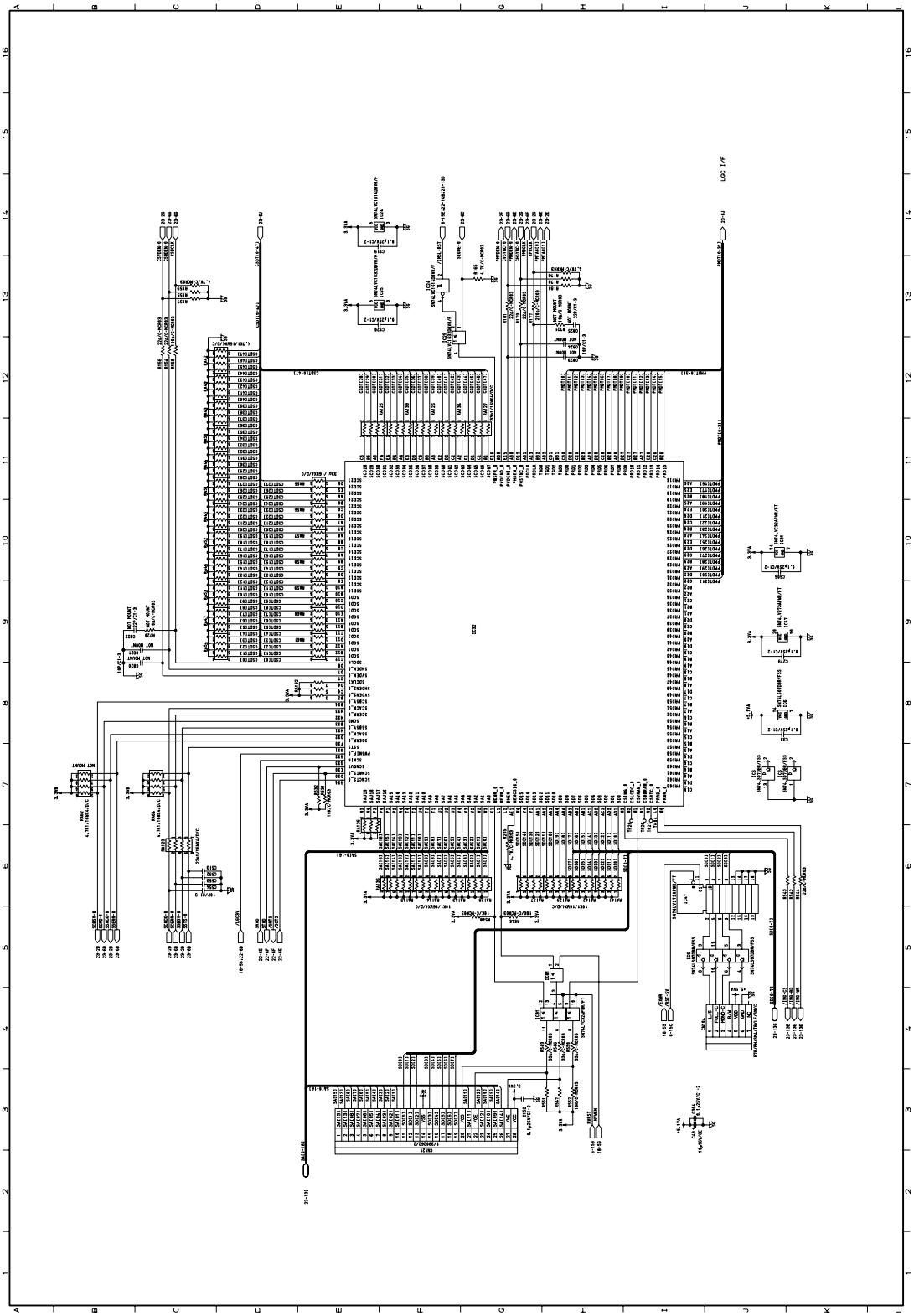

Fig. 3-20

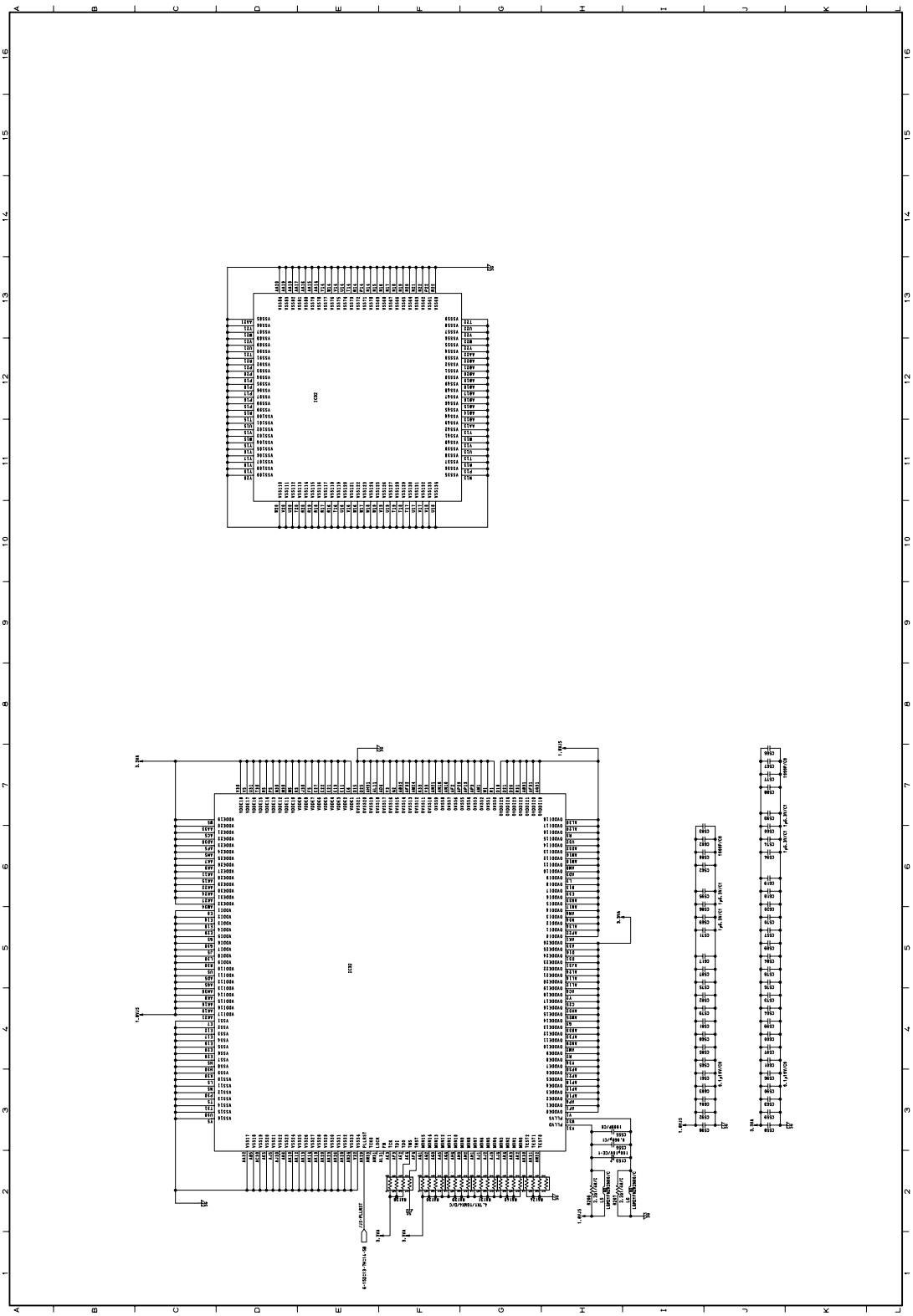

Fig. 3-21

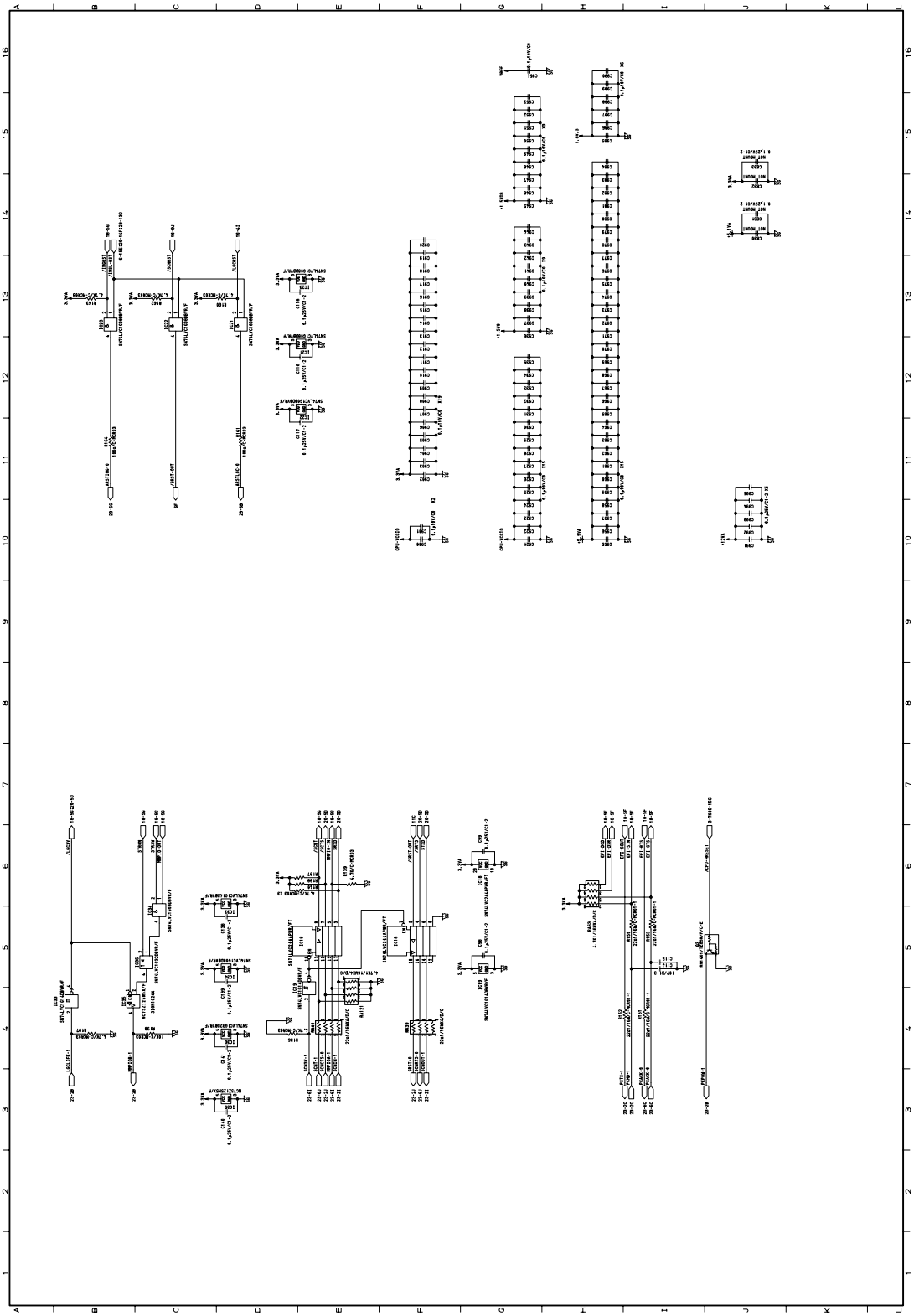

Fig. 3-22

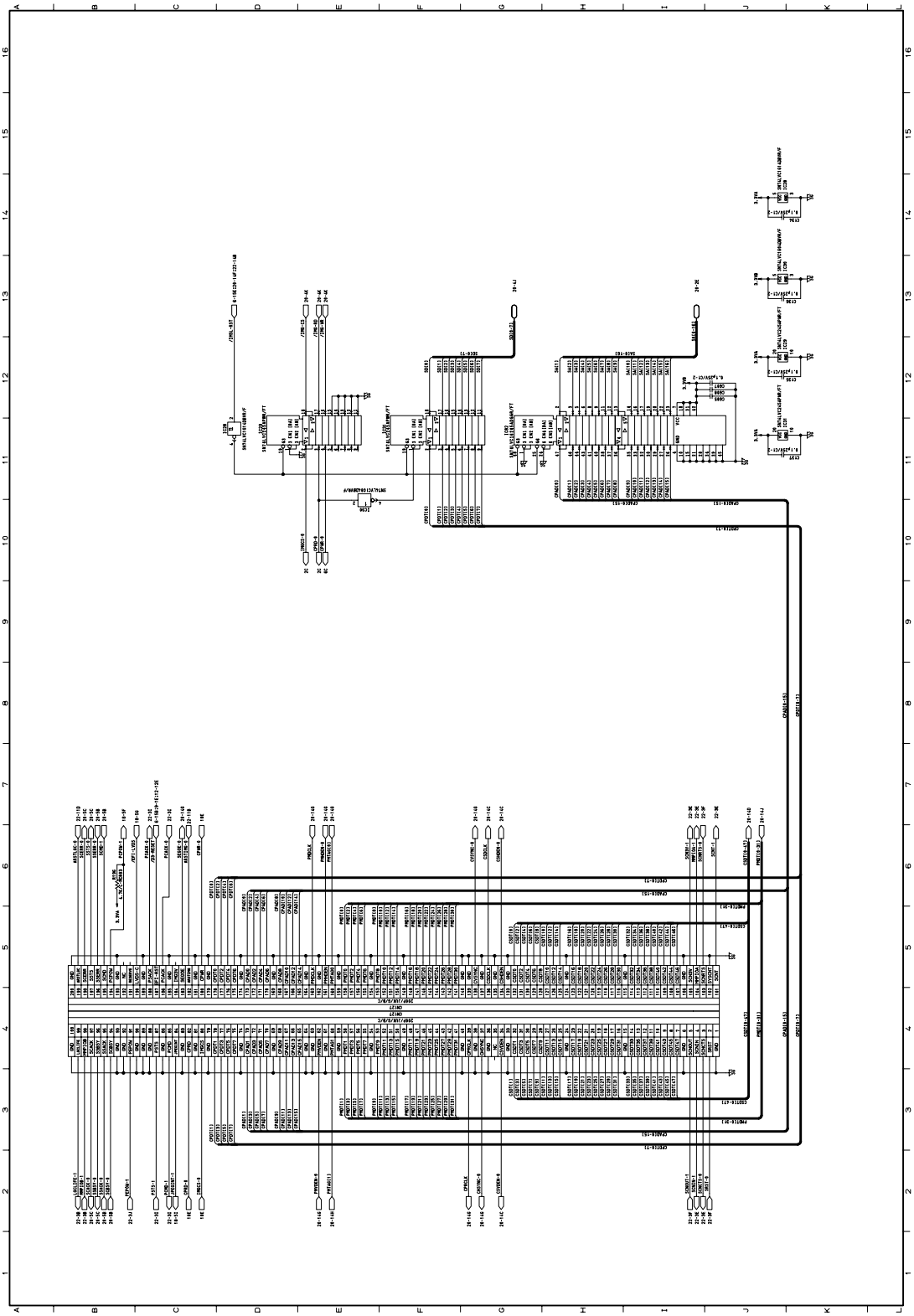

Fig. 3-23

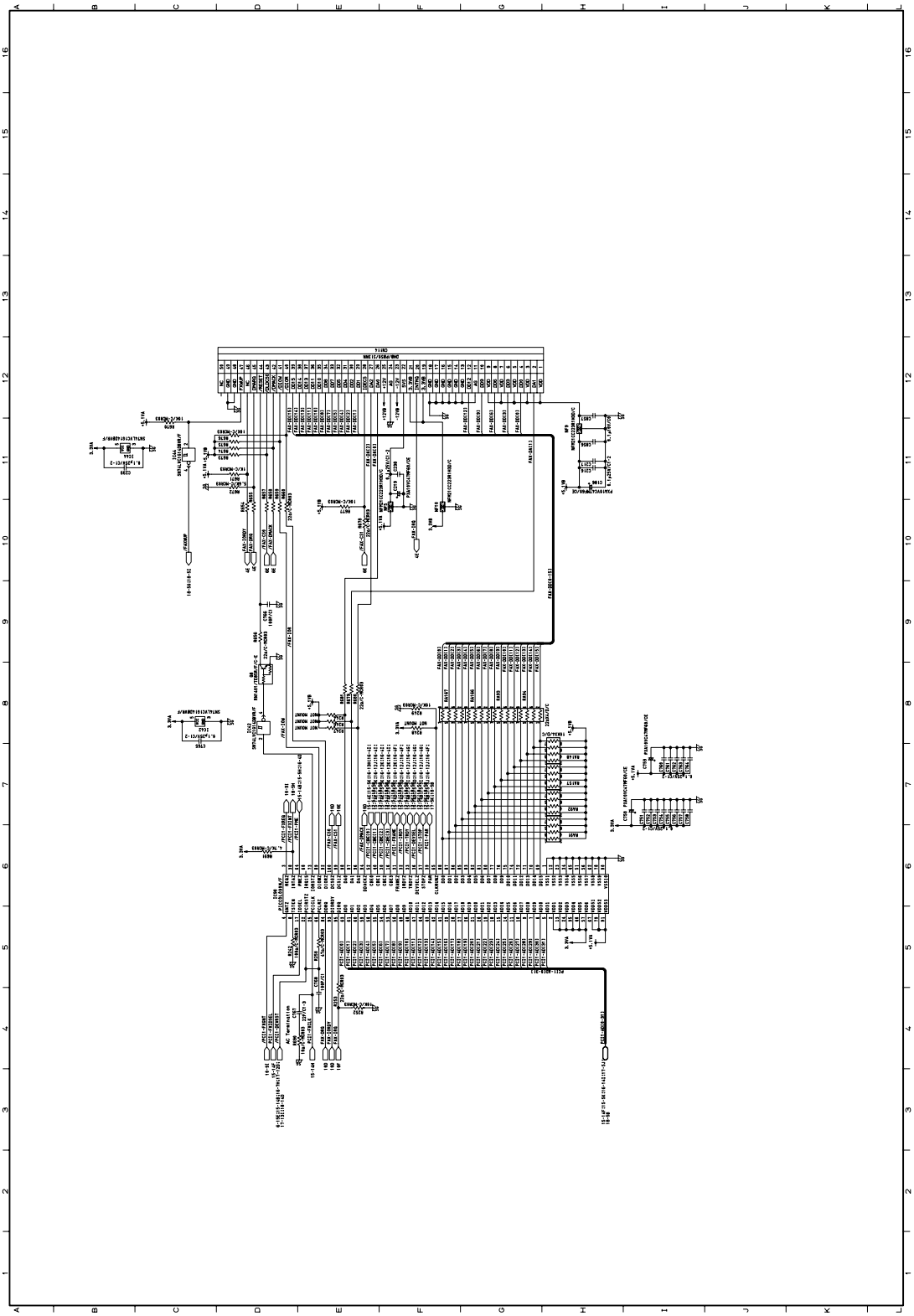

Fig. 3-24

3.2 CODEC circuit (JSP board)

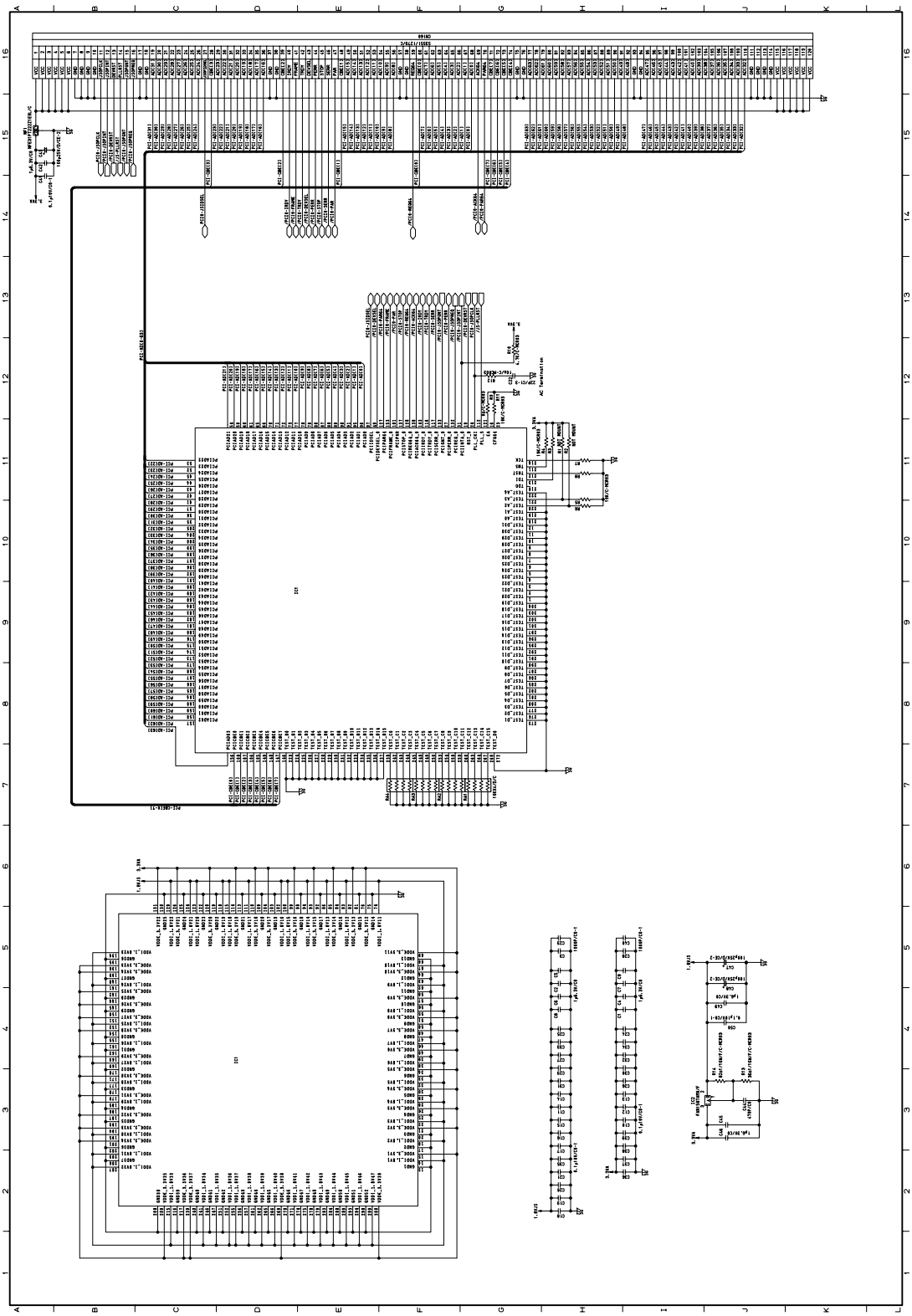

Fig. 3-25

3.3 Logic circuit (LGC board)

LGC board 1/43

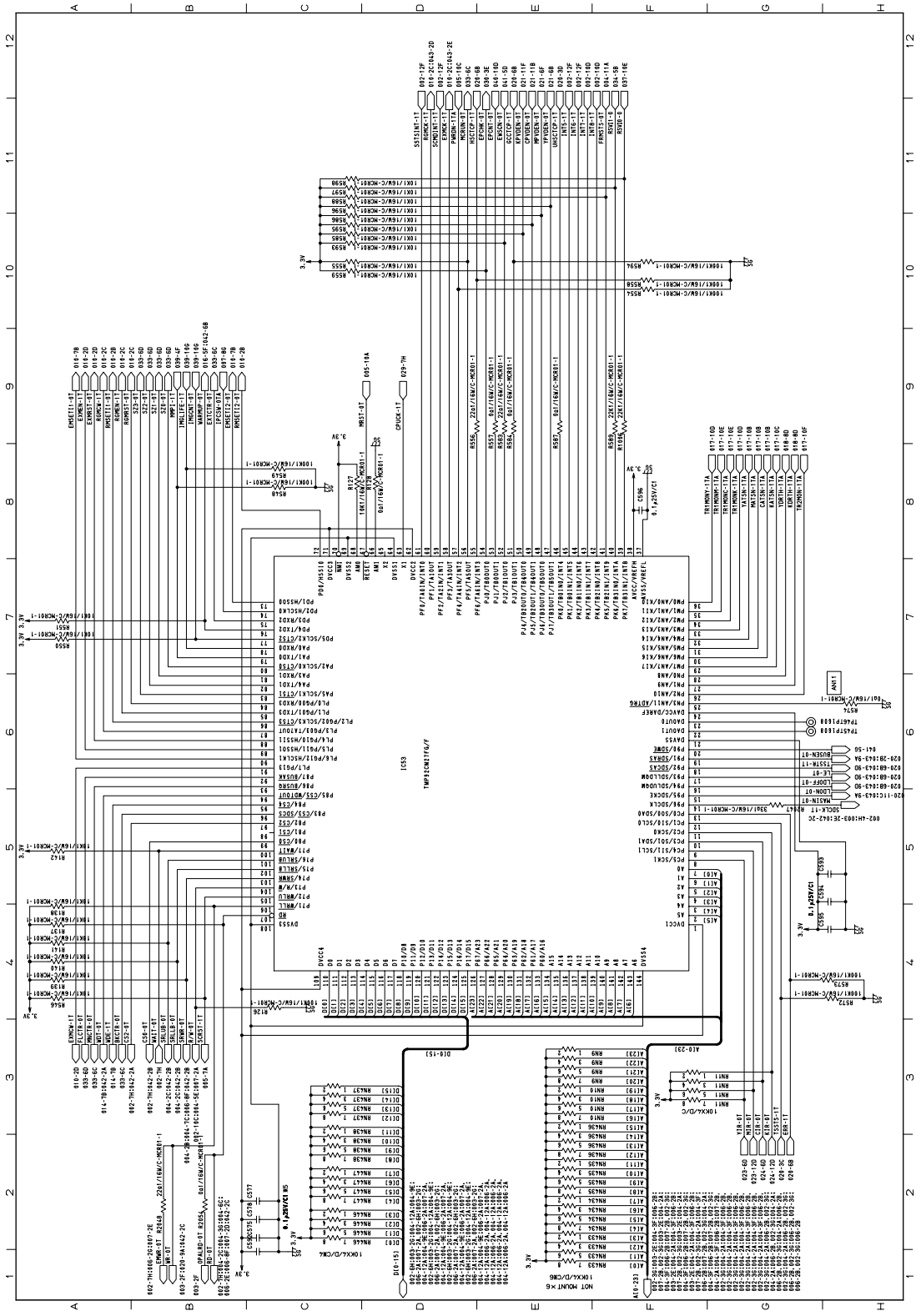

Fig. 3-26

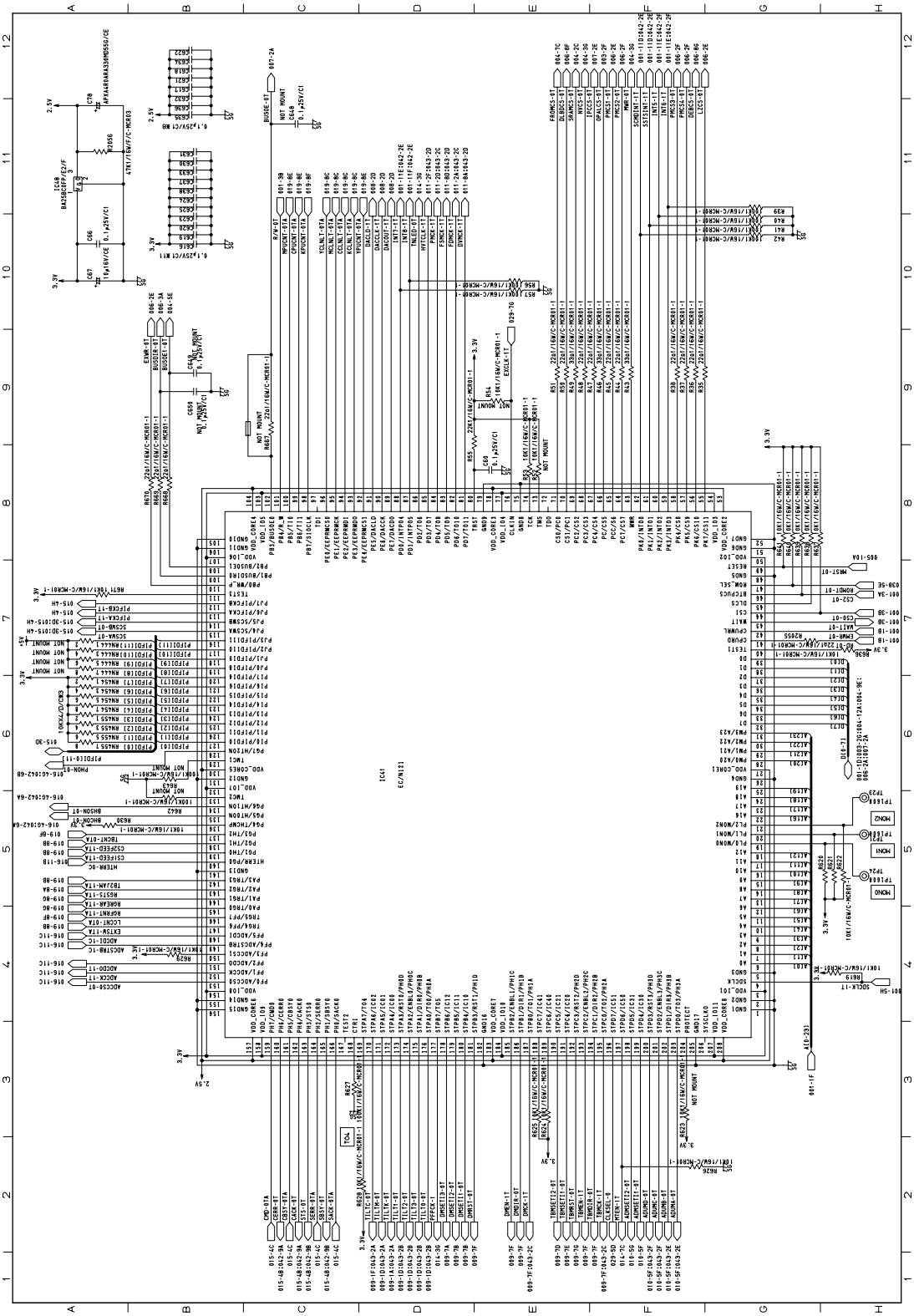

Fig. 3-27

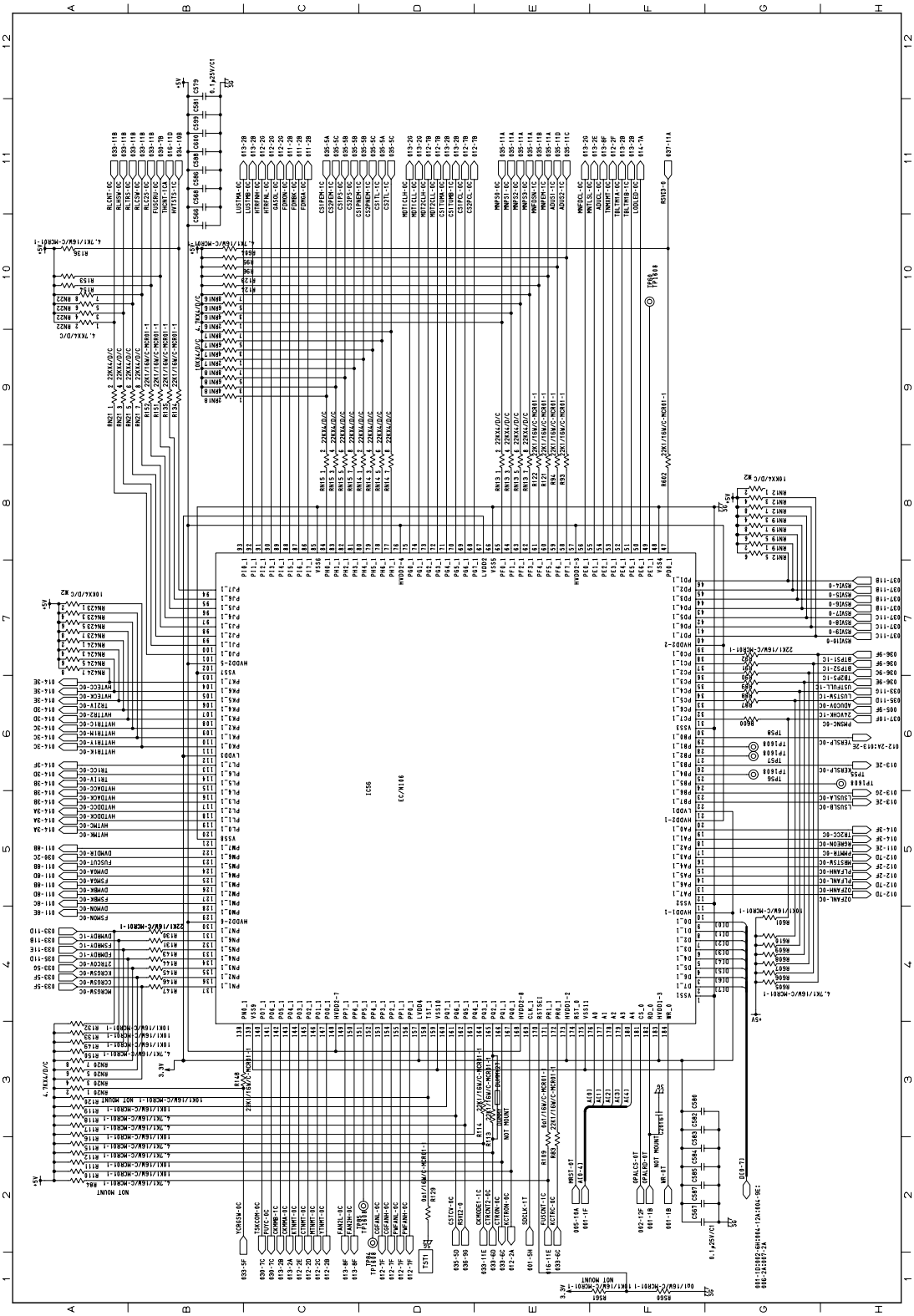

Fig. 3-28

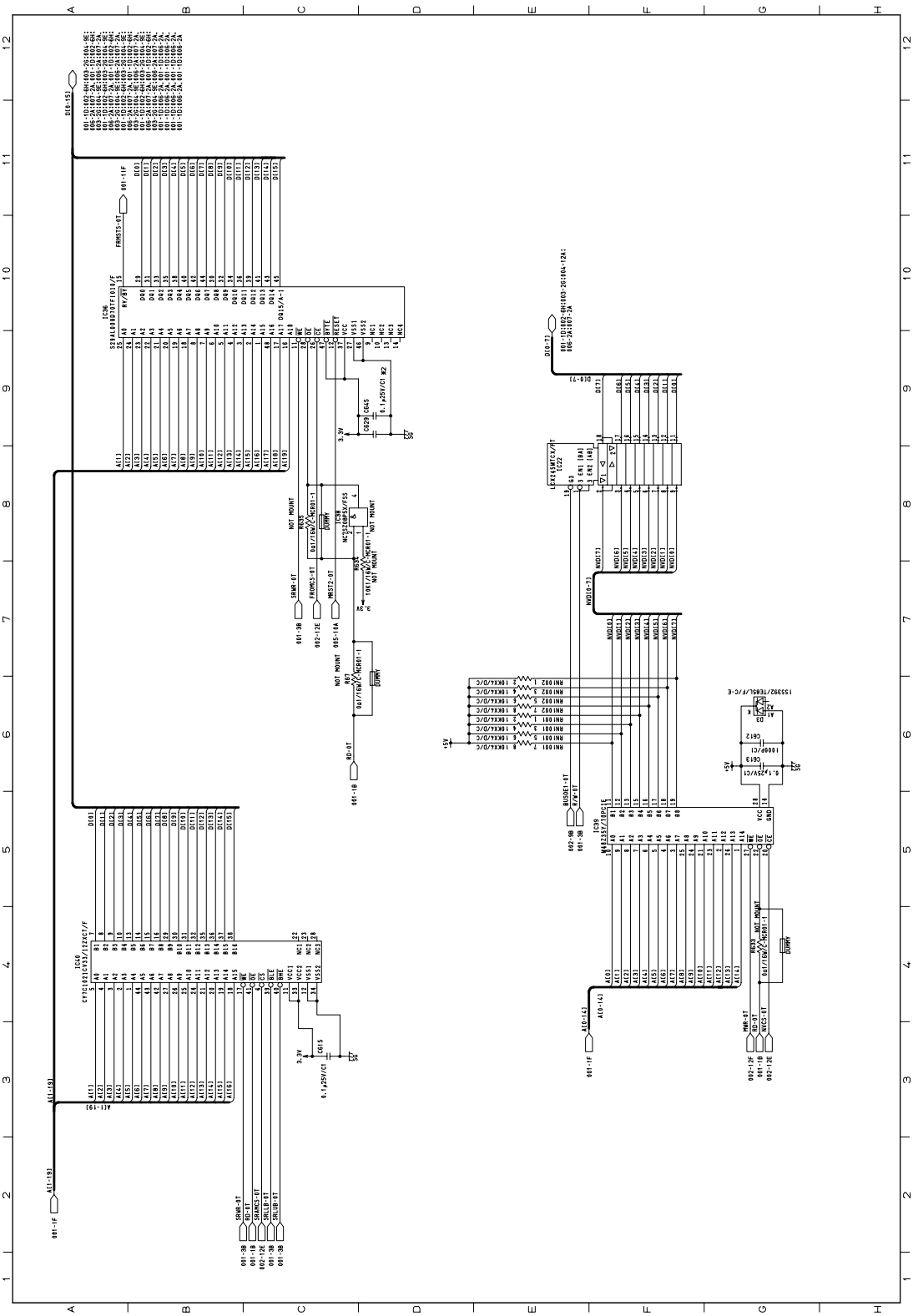

Fig. 3-29

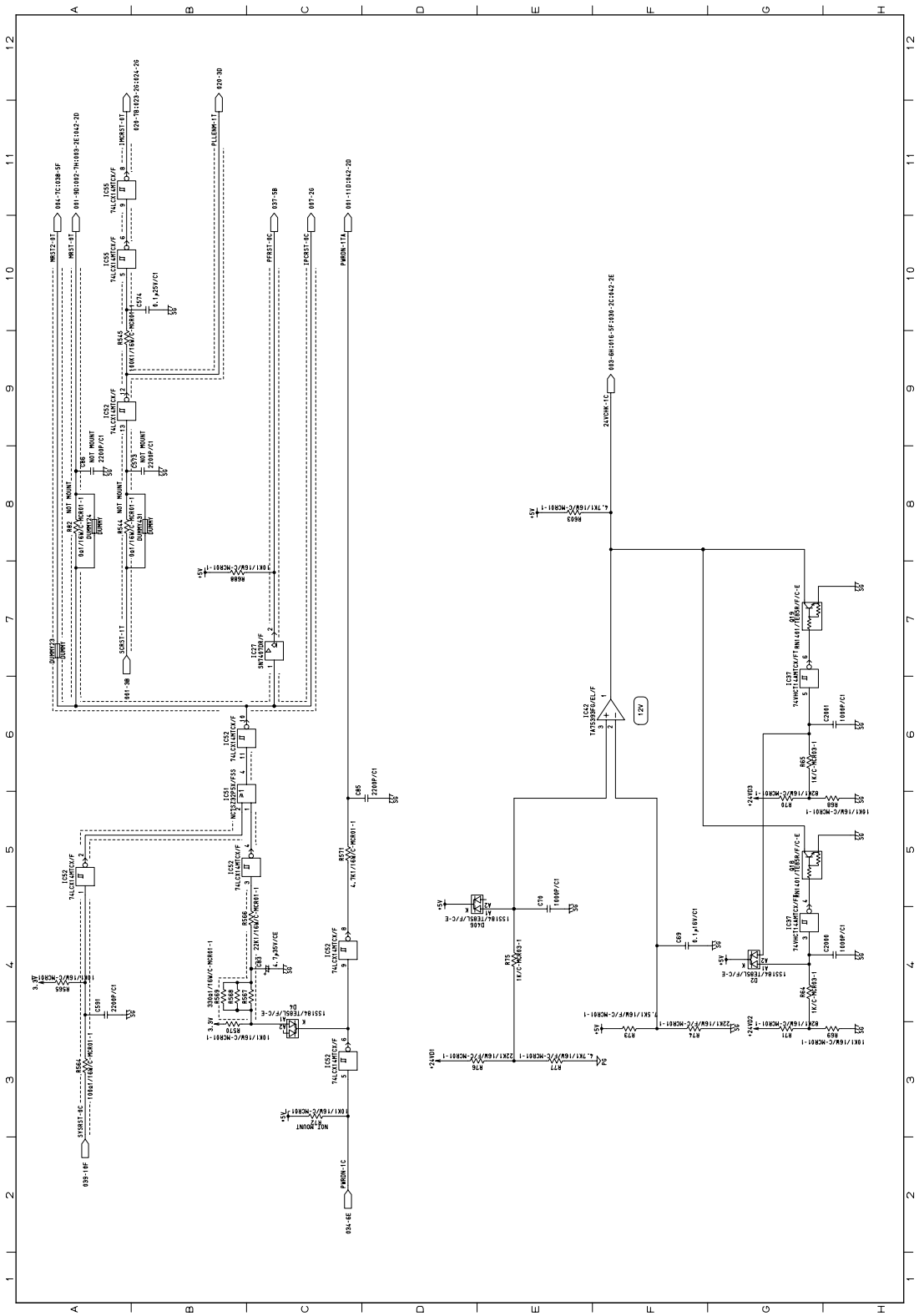

Fig. 3-30

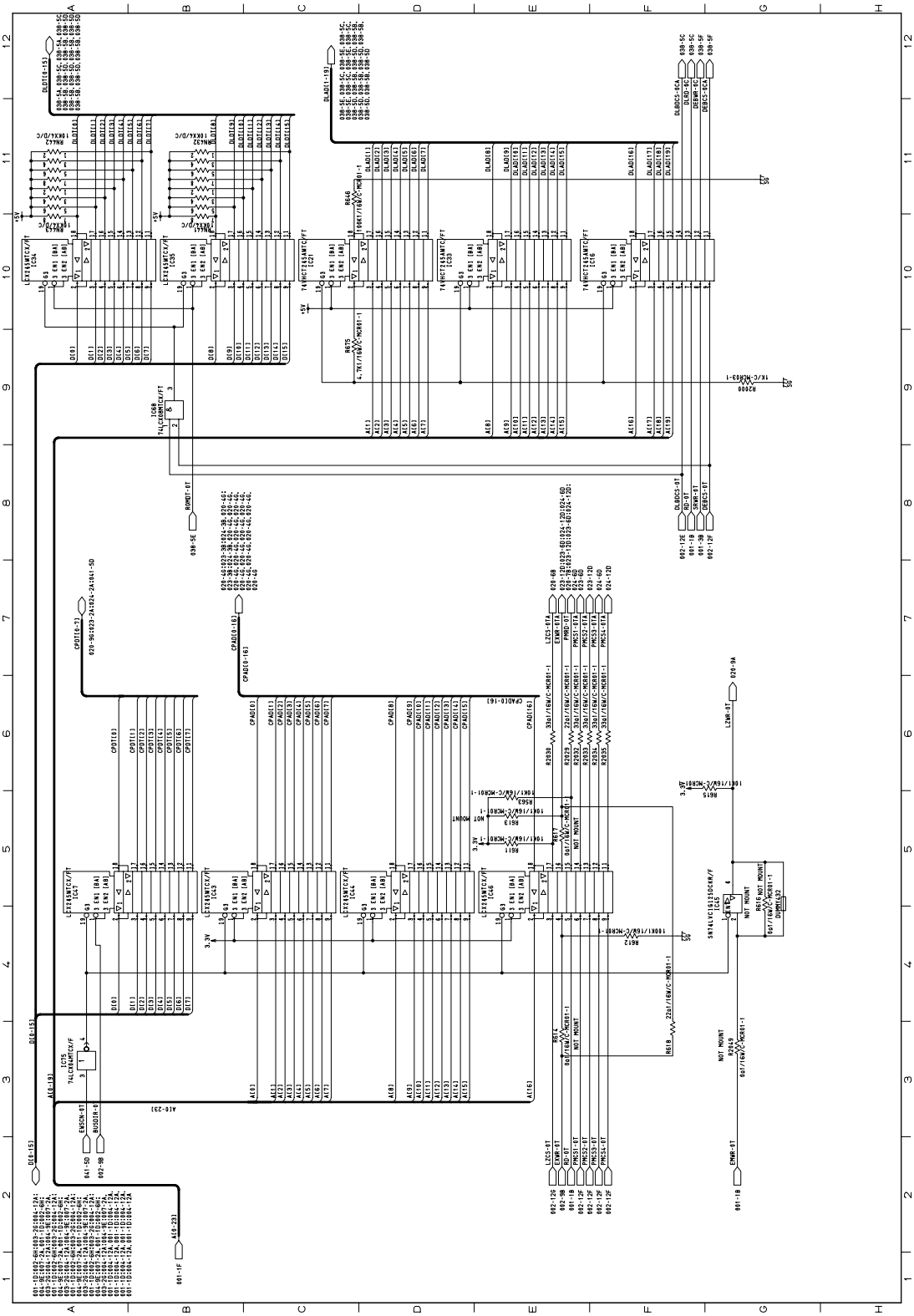

Fig. 3-31

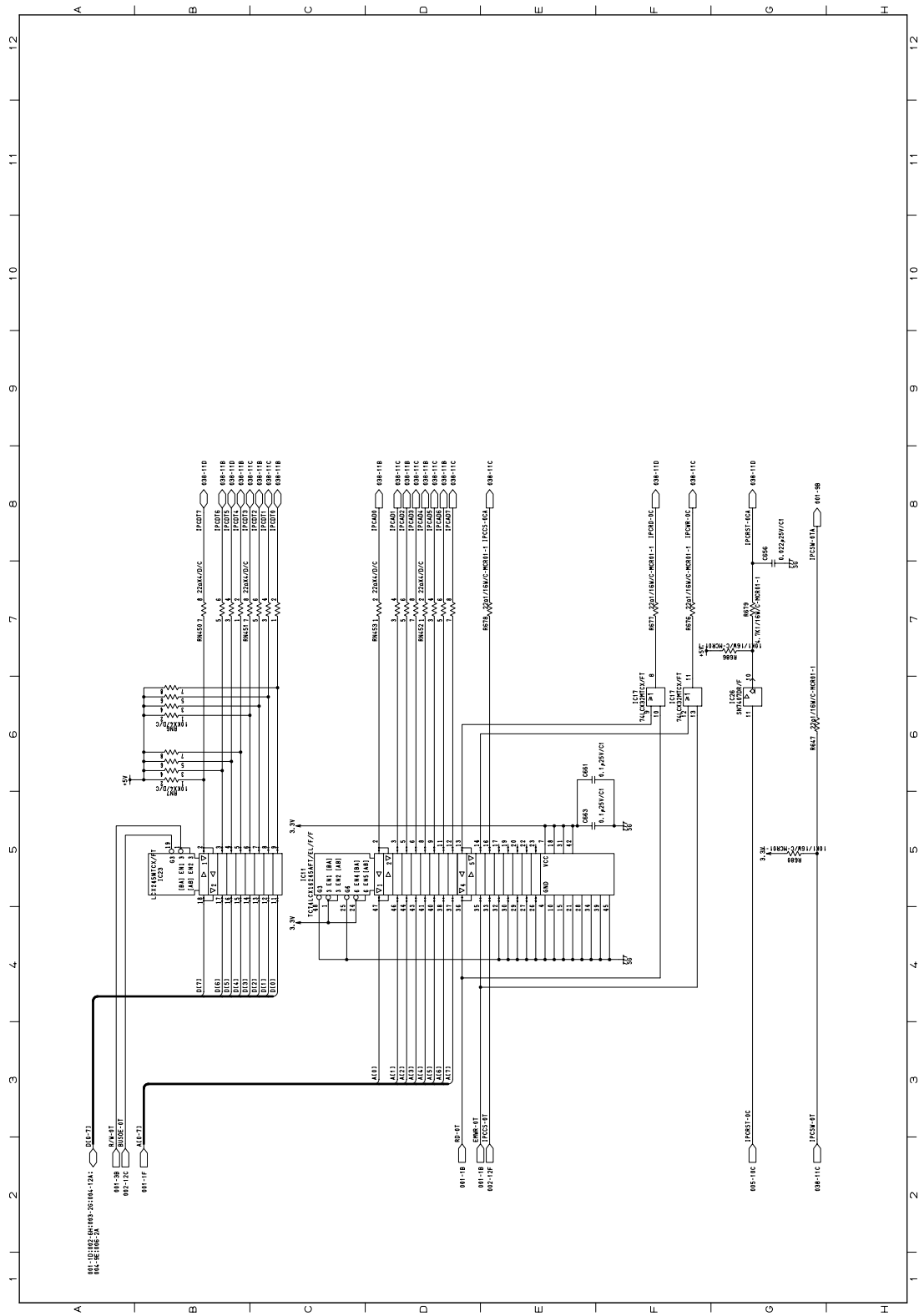

Fig. 3-32

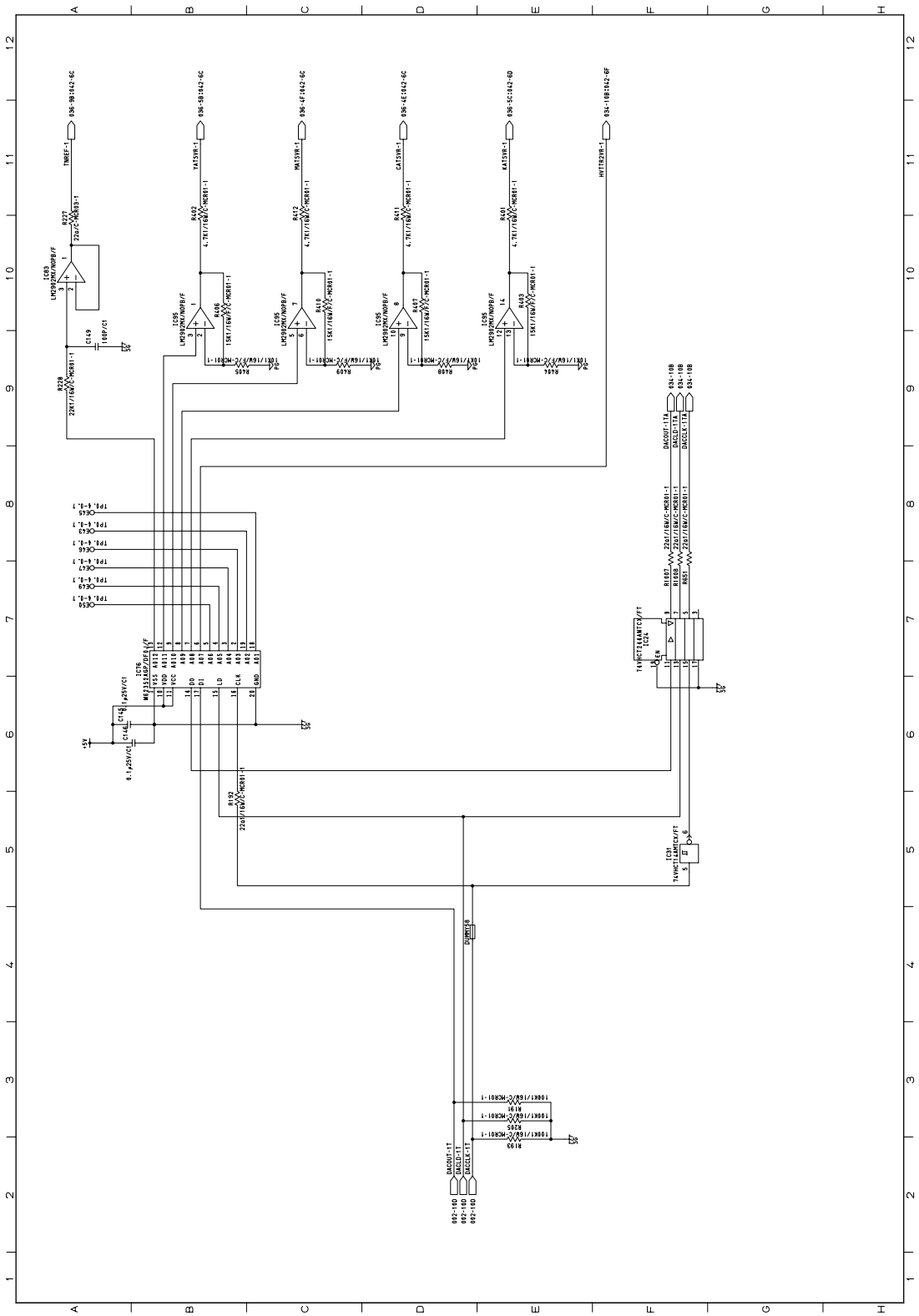

Fig. 3-33

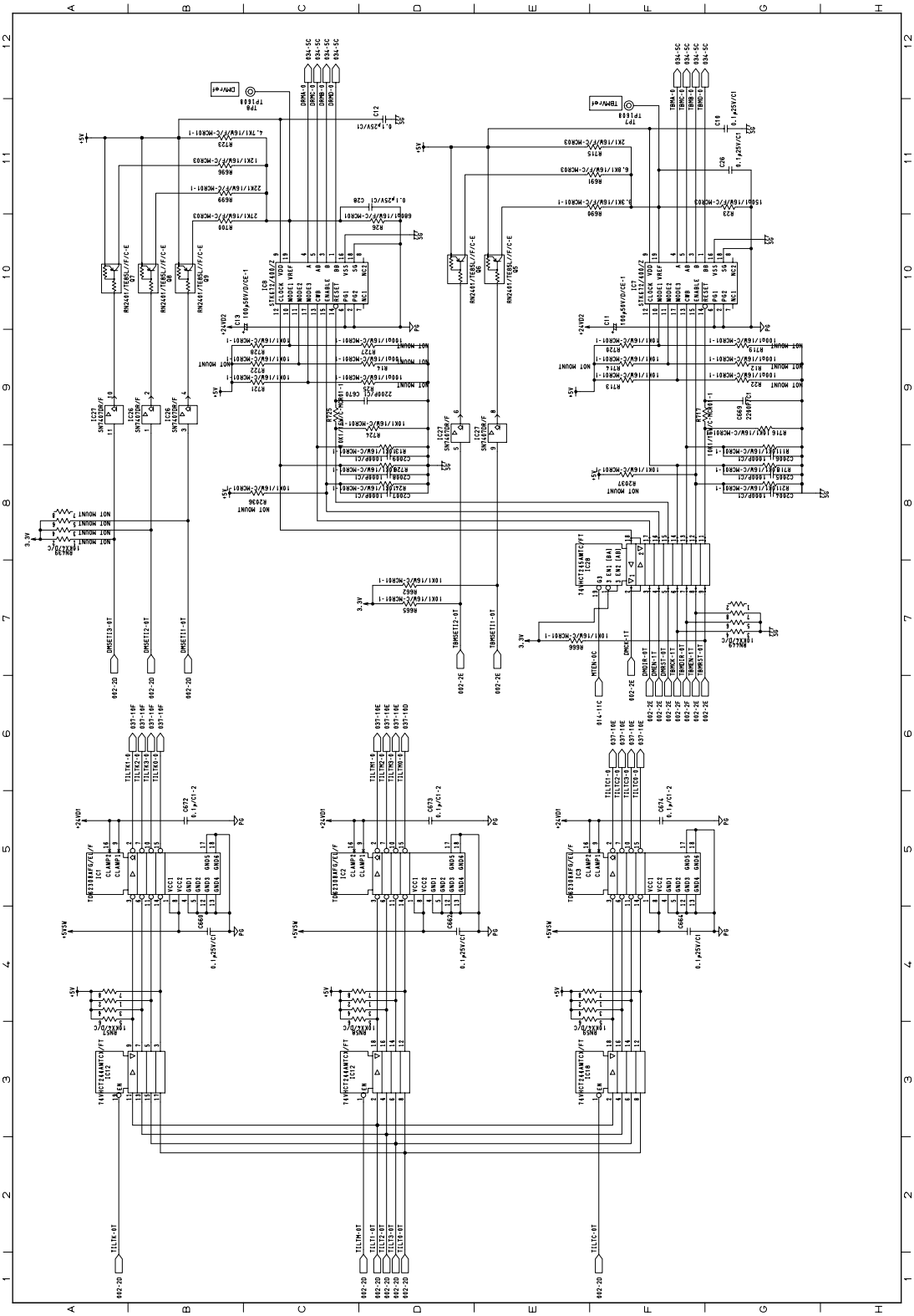

Fig. 3-34

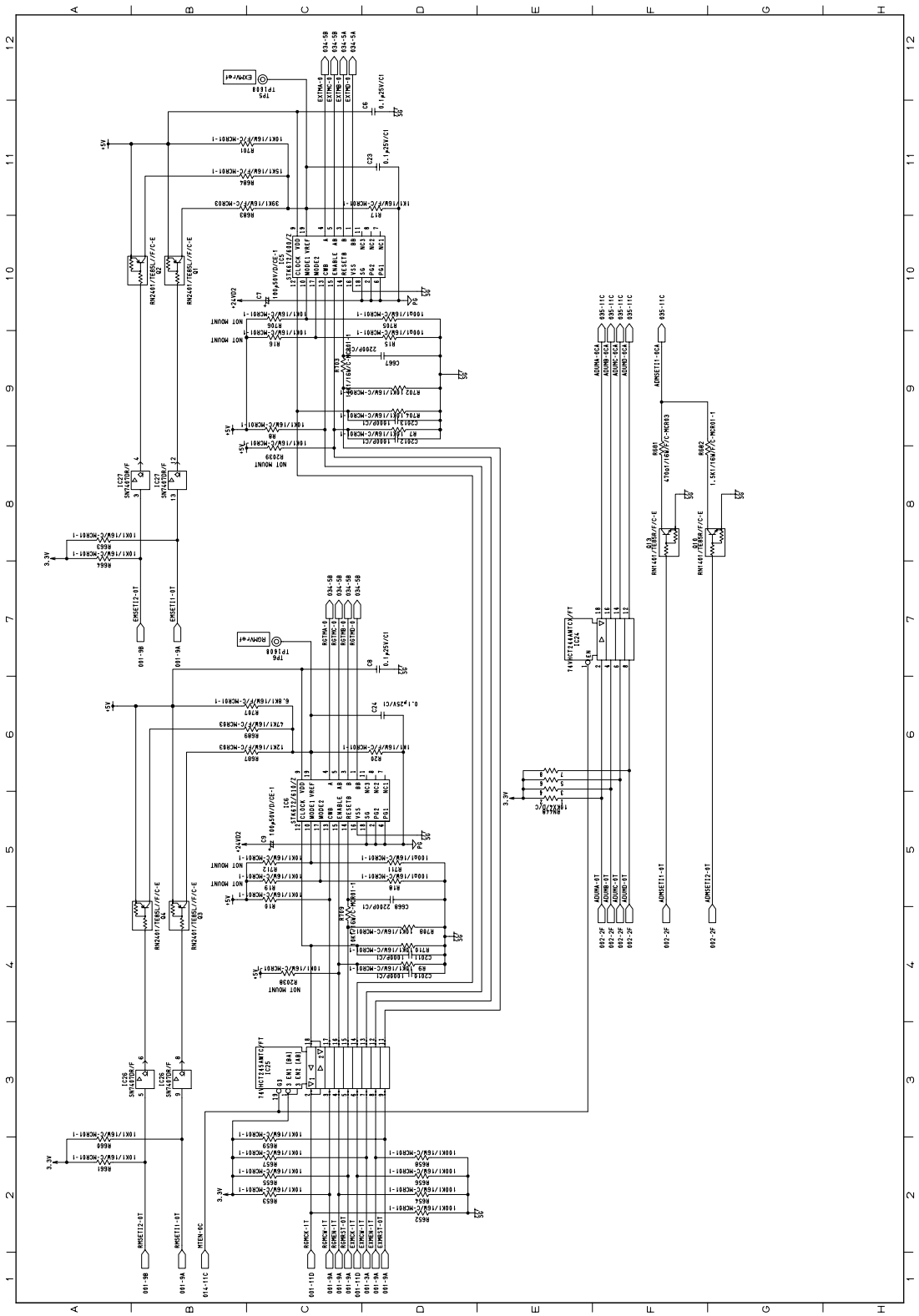

Fig. 3-35

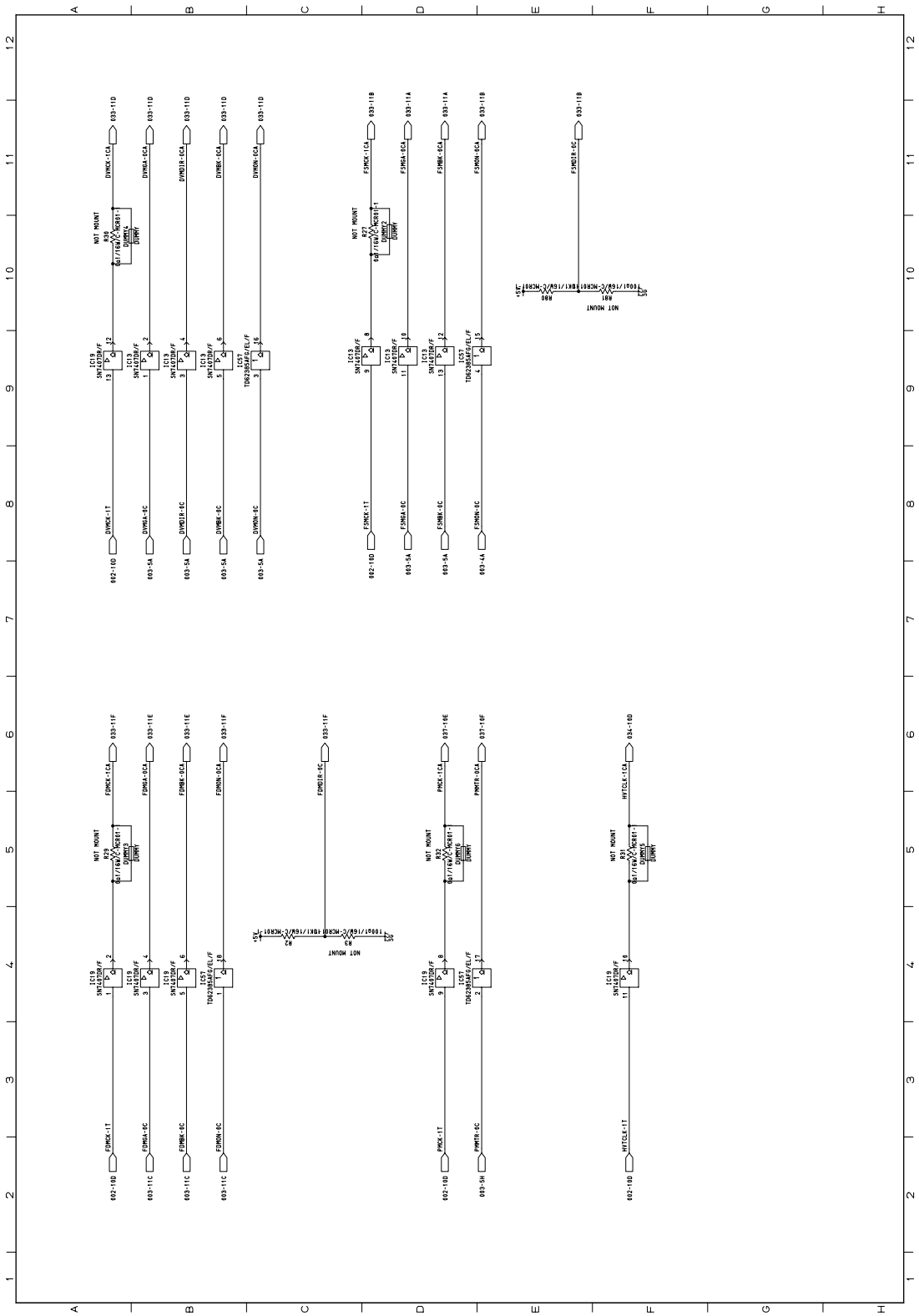

Fig. 3-36

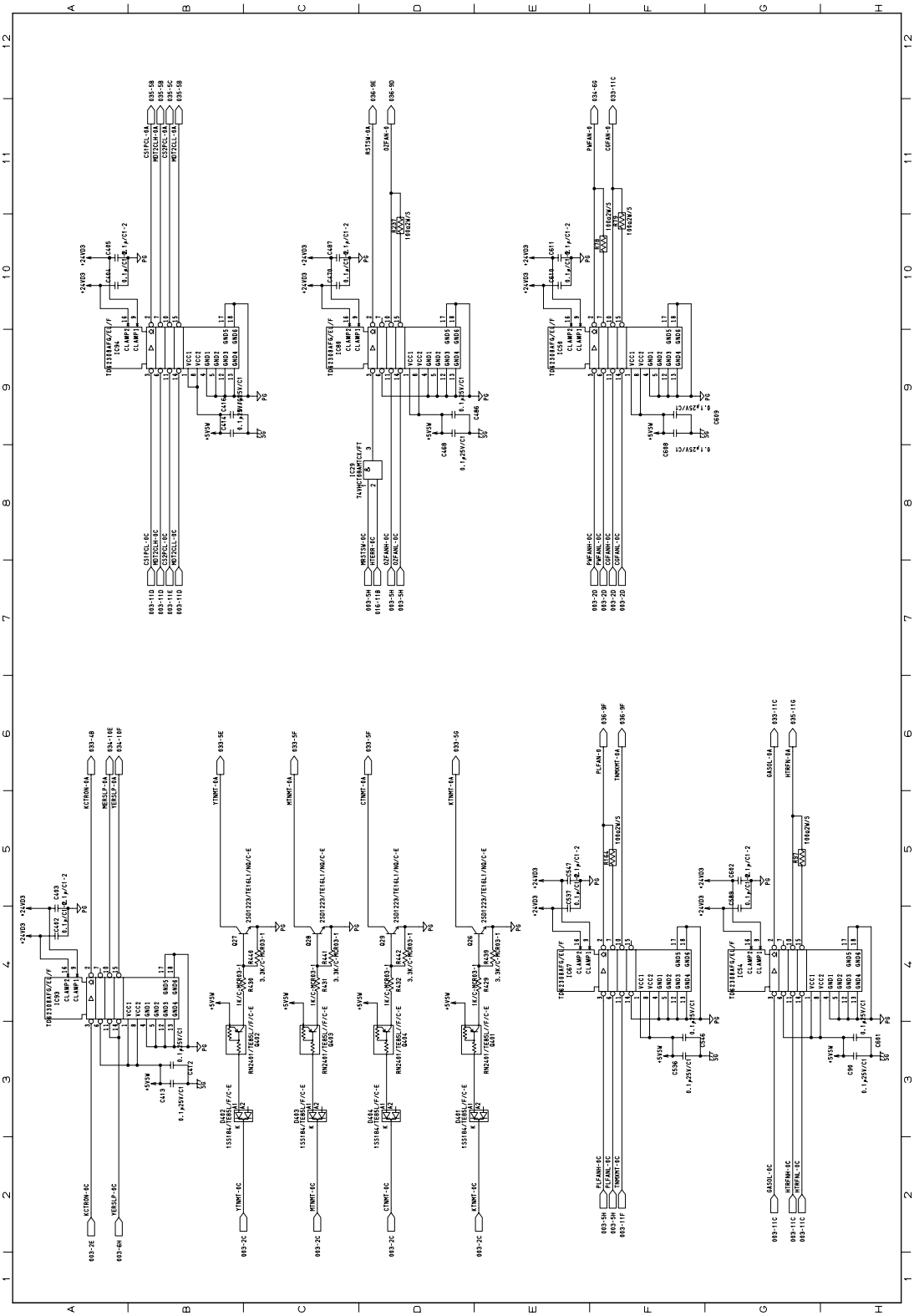

Fig. 3-37

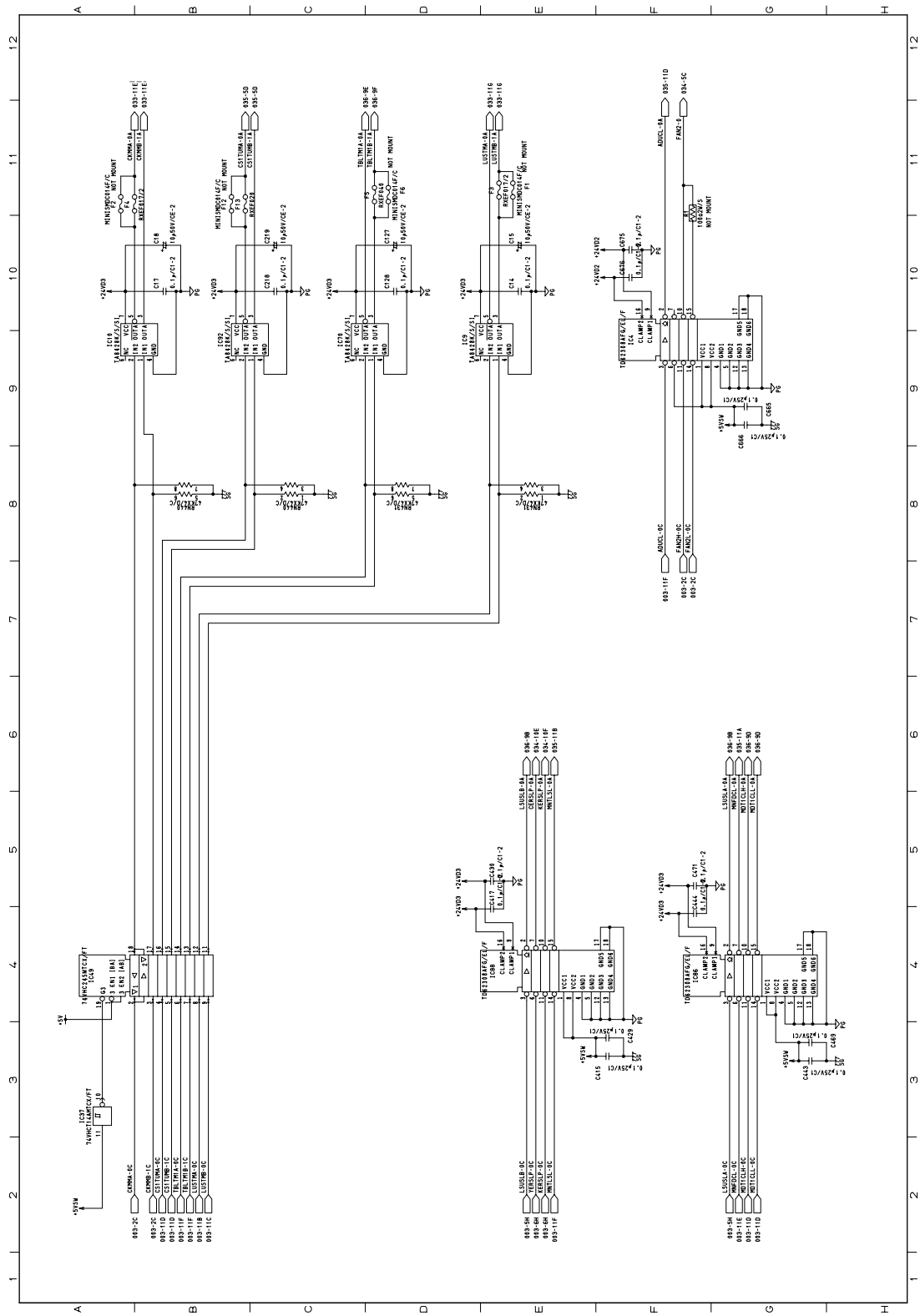

Fig. 3-38

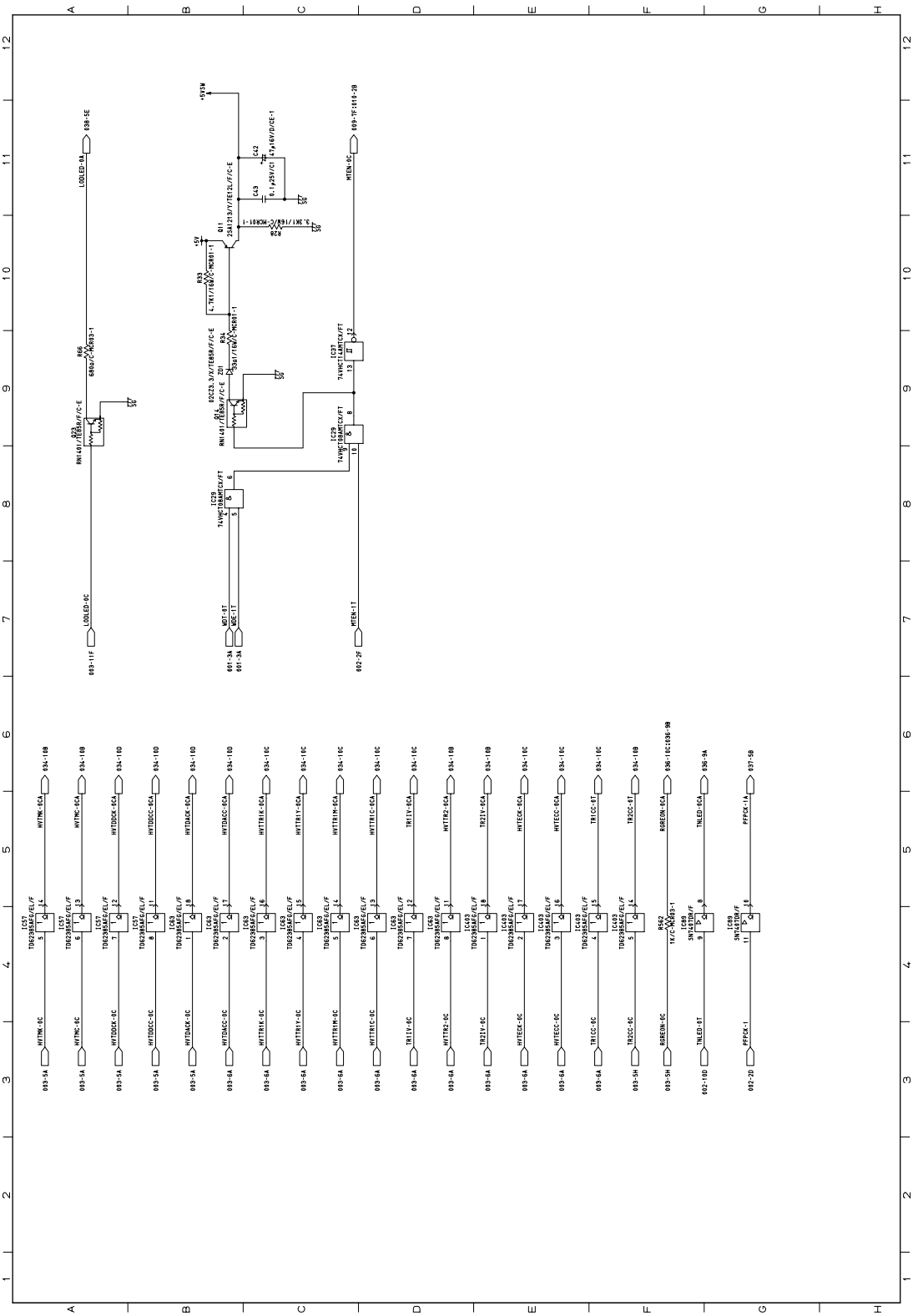

Fig. 3-39

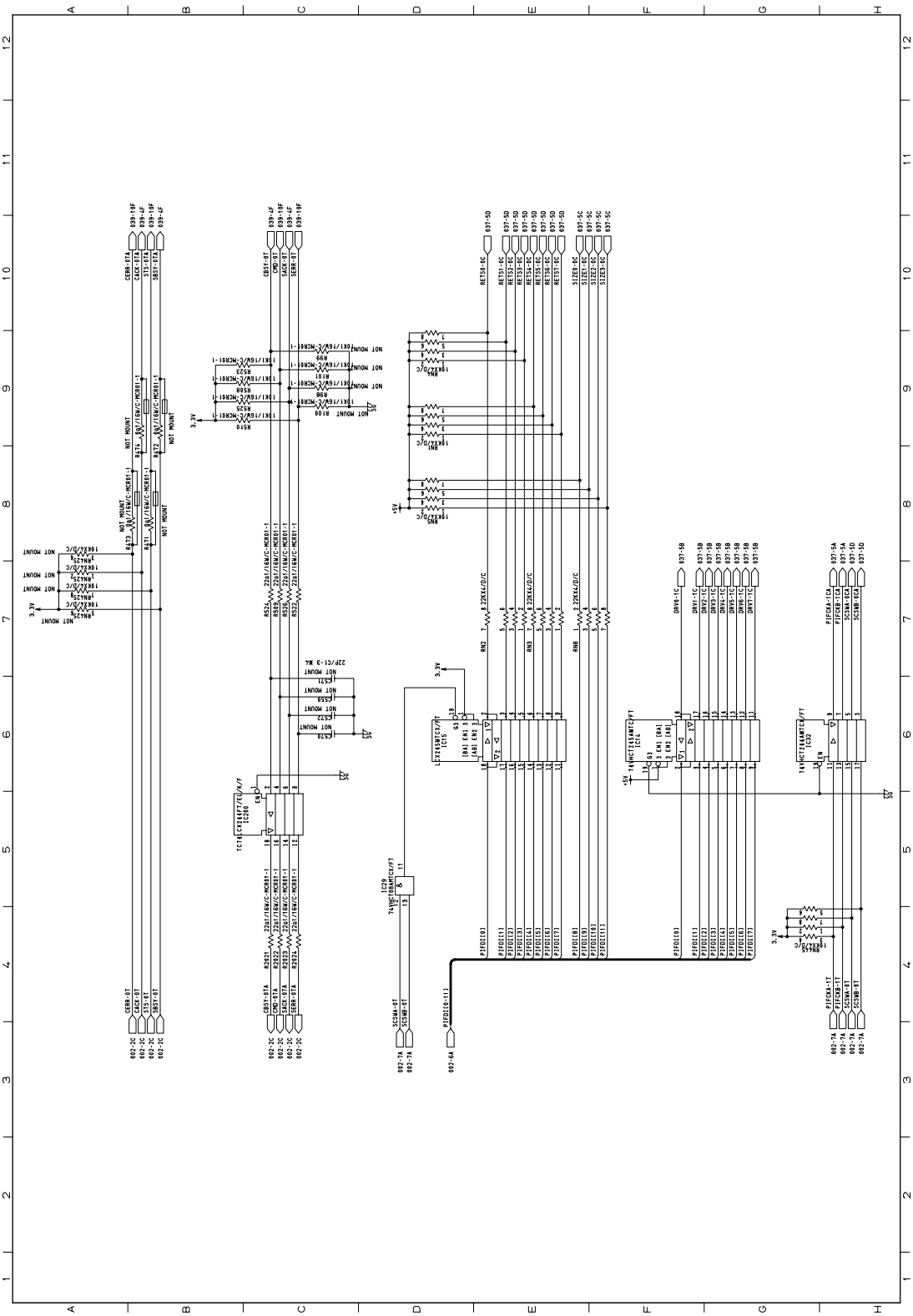

Fig. 3-40

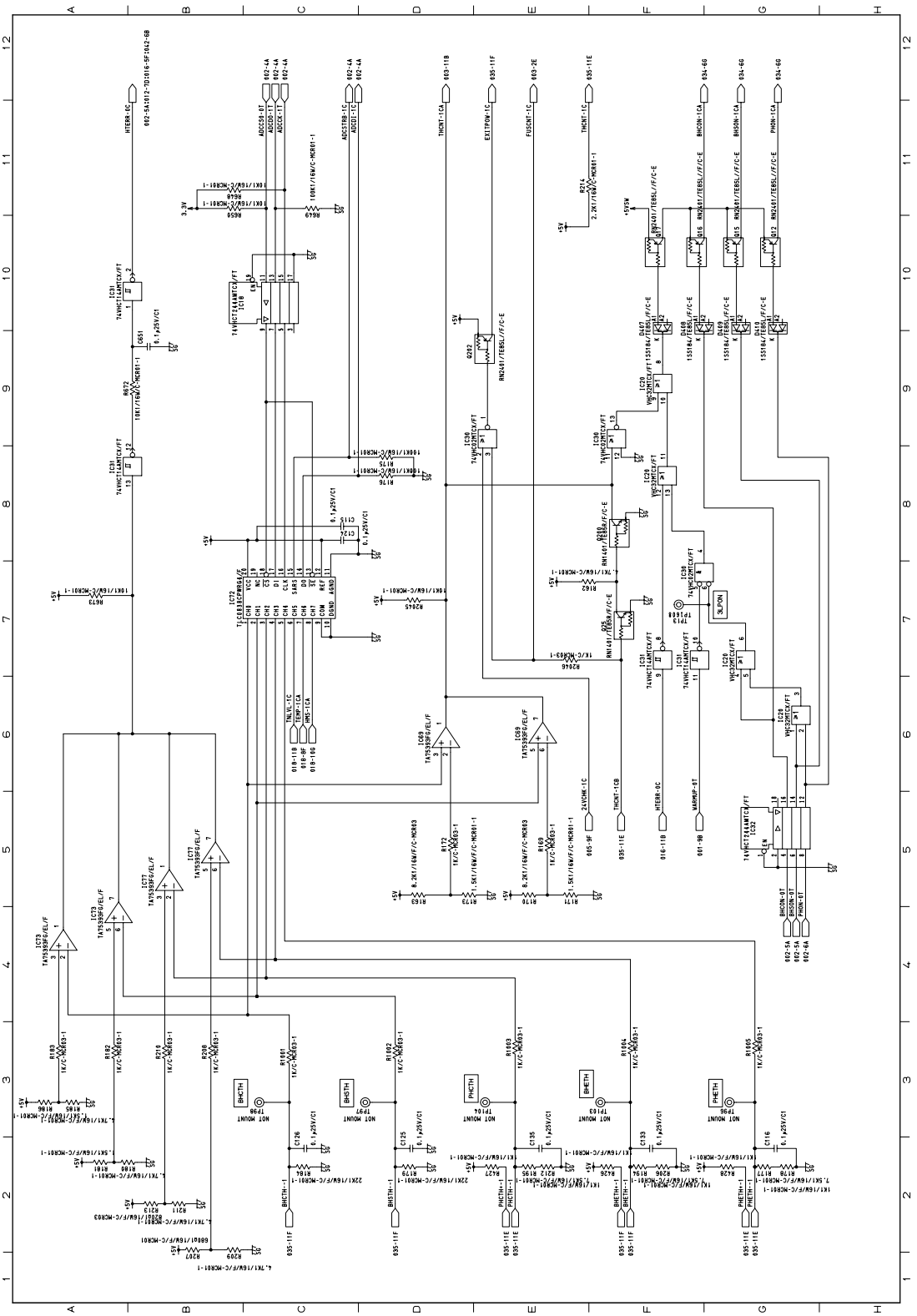

Fig. 3-41

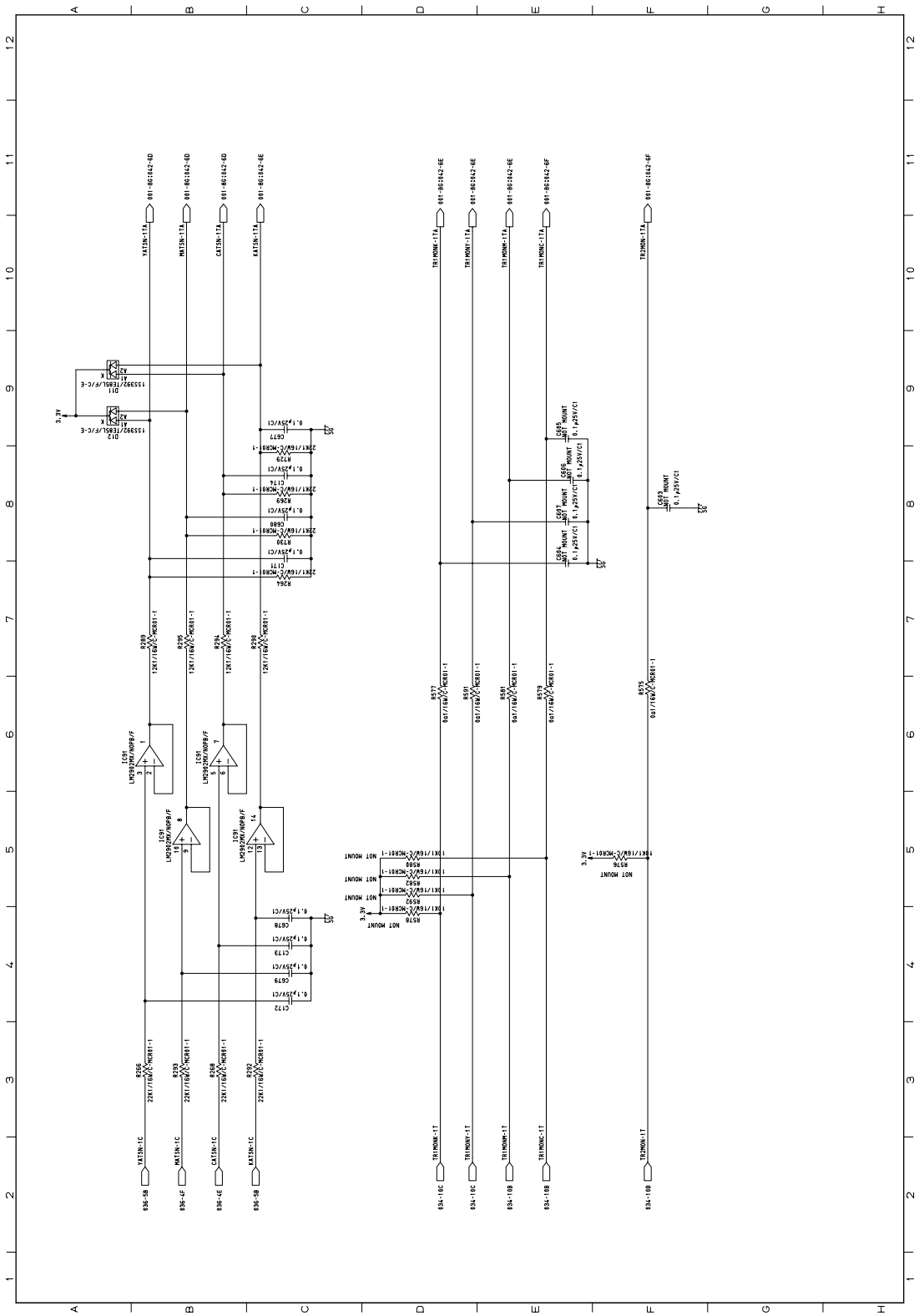

Fig. 3-42

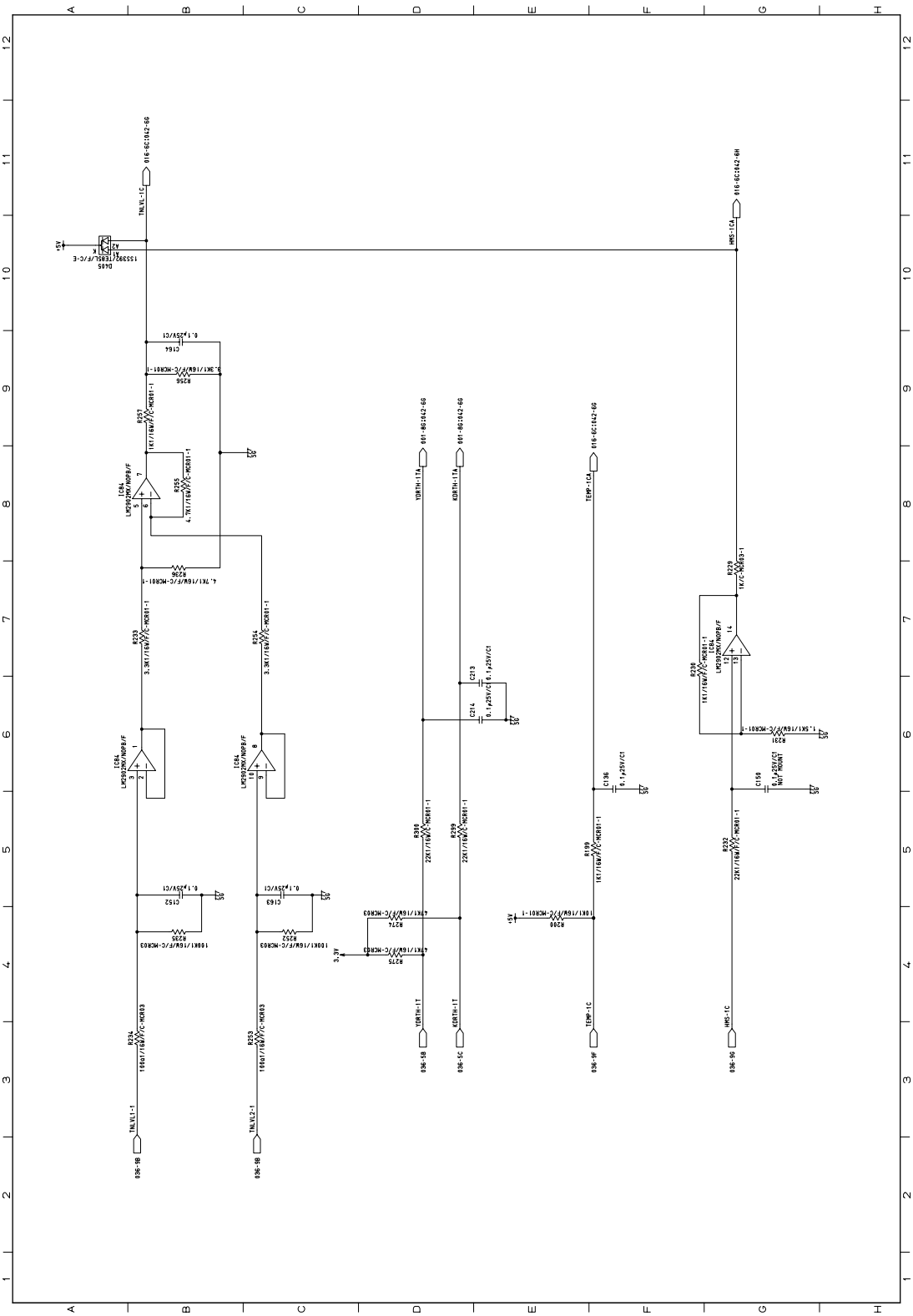

Fig. 3-43

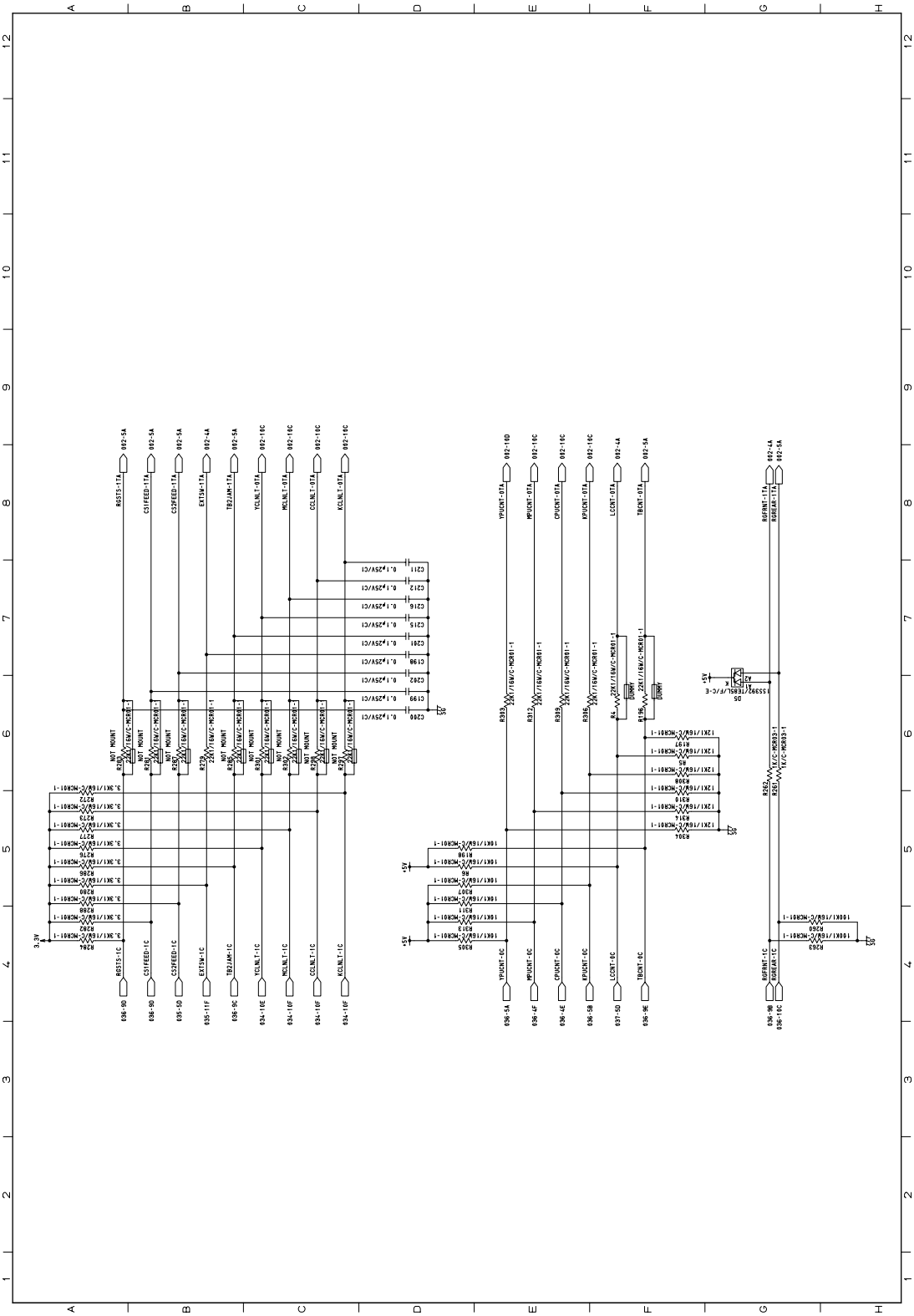

Fig. 3-44

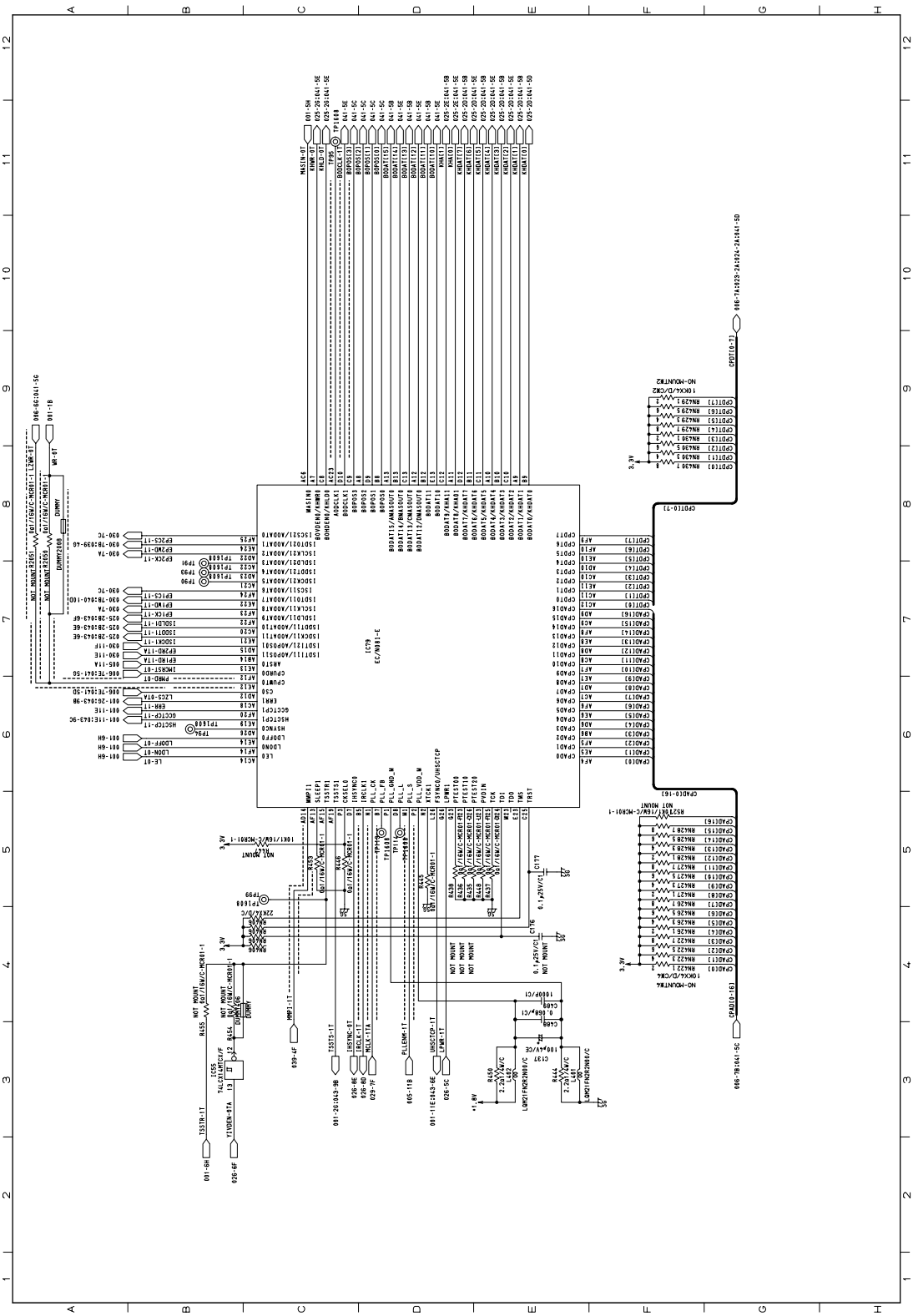

Fig. 3-45

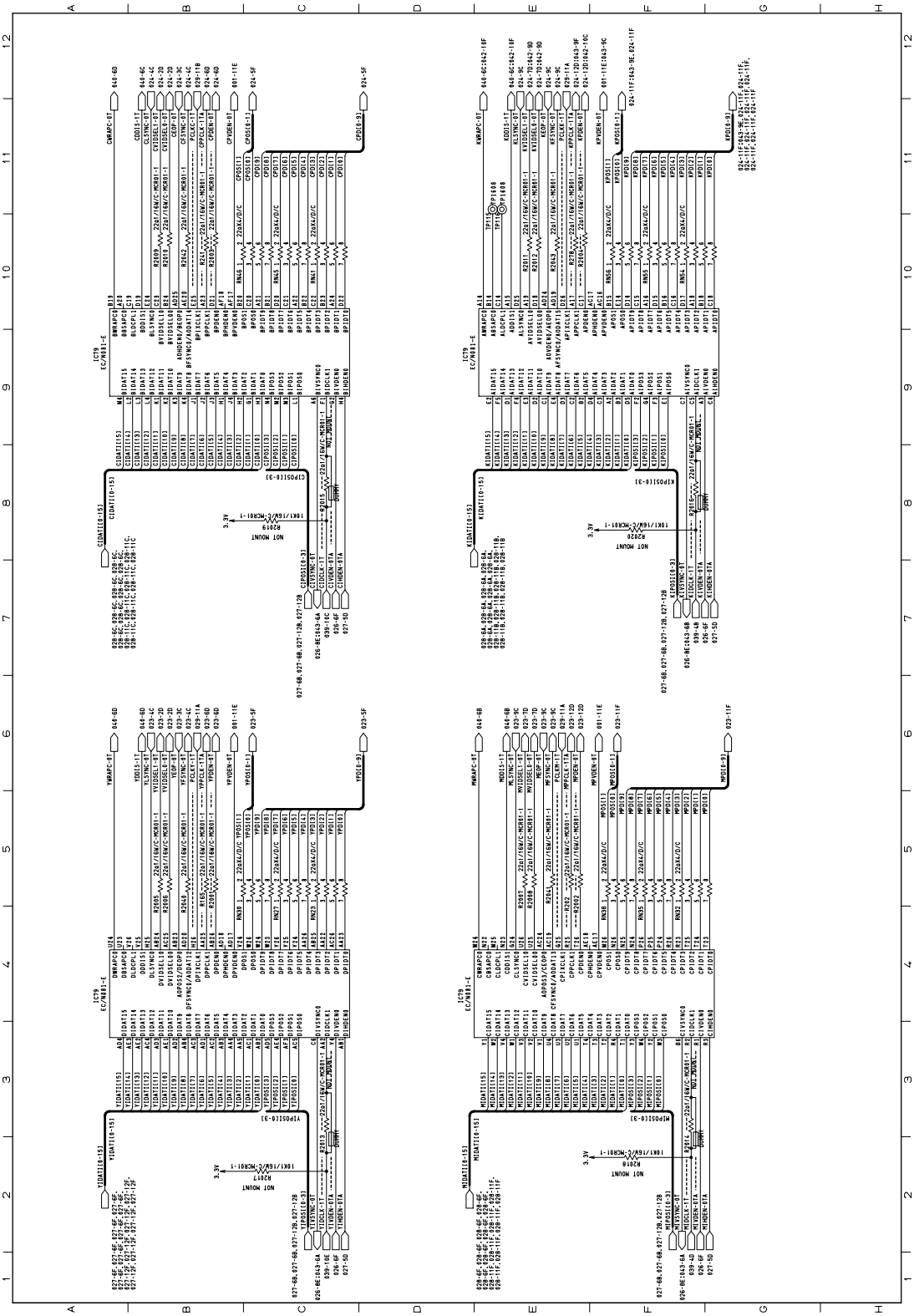

Fig. 3-46

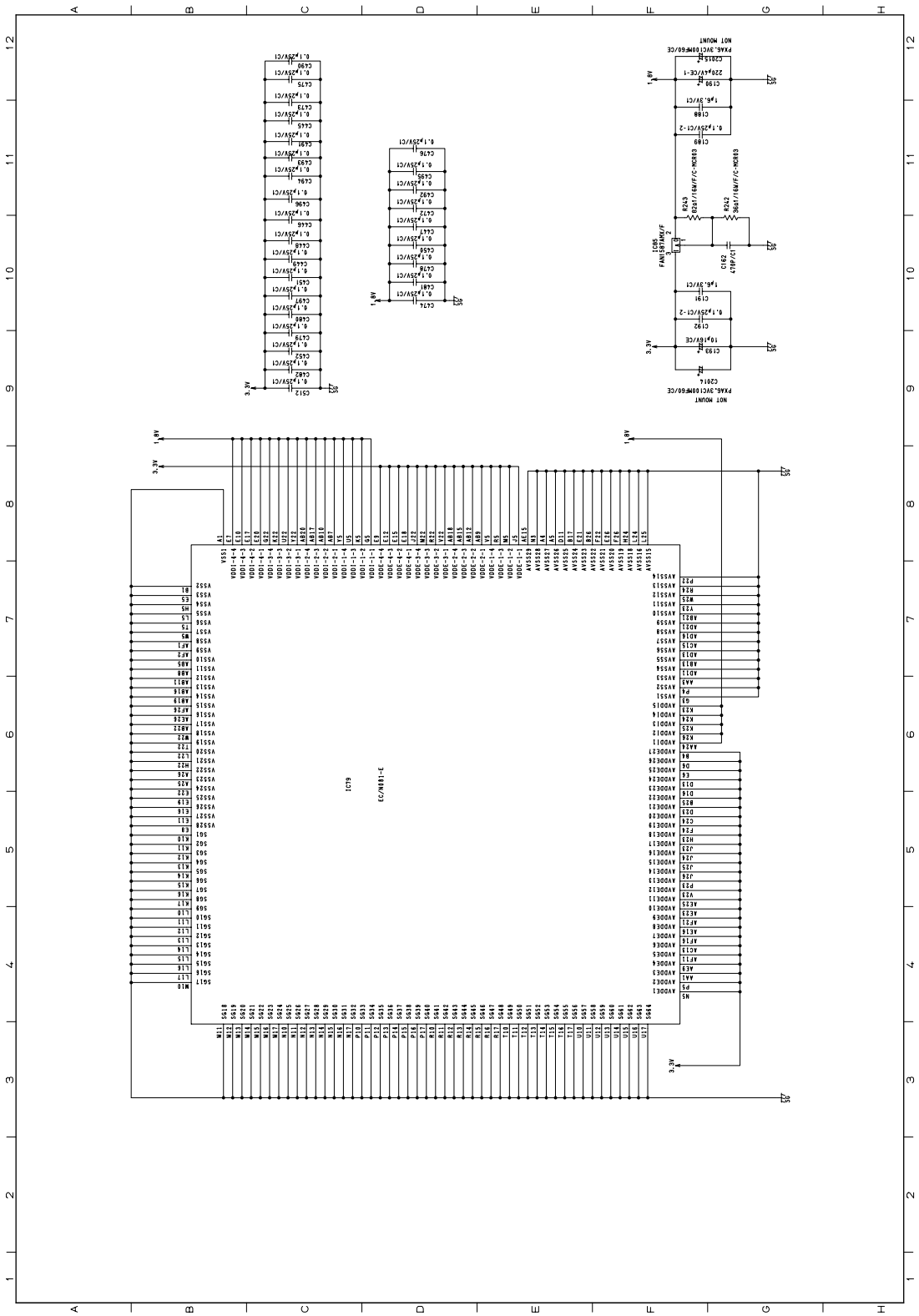

Fig. 3-47

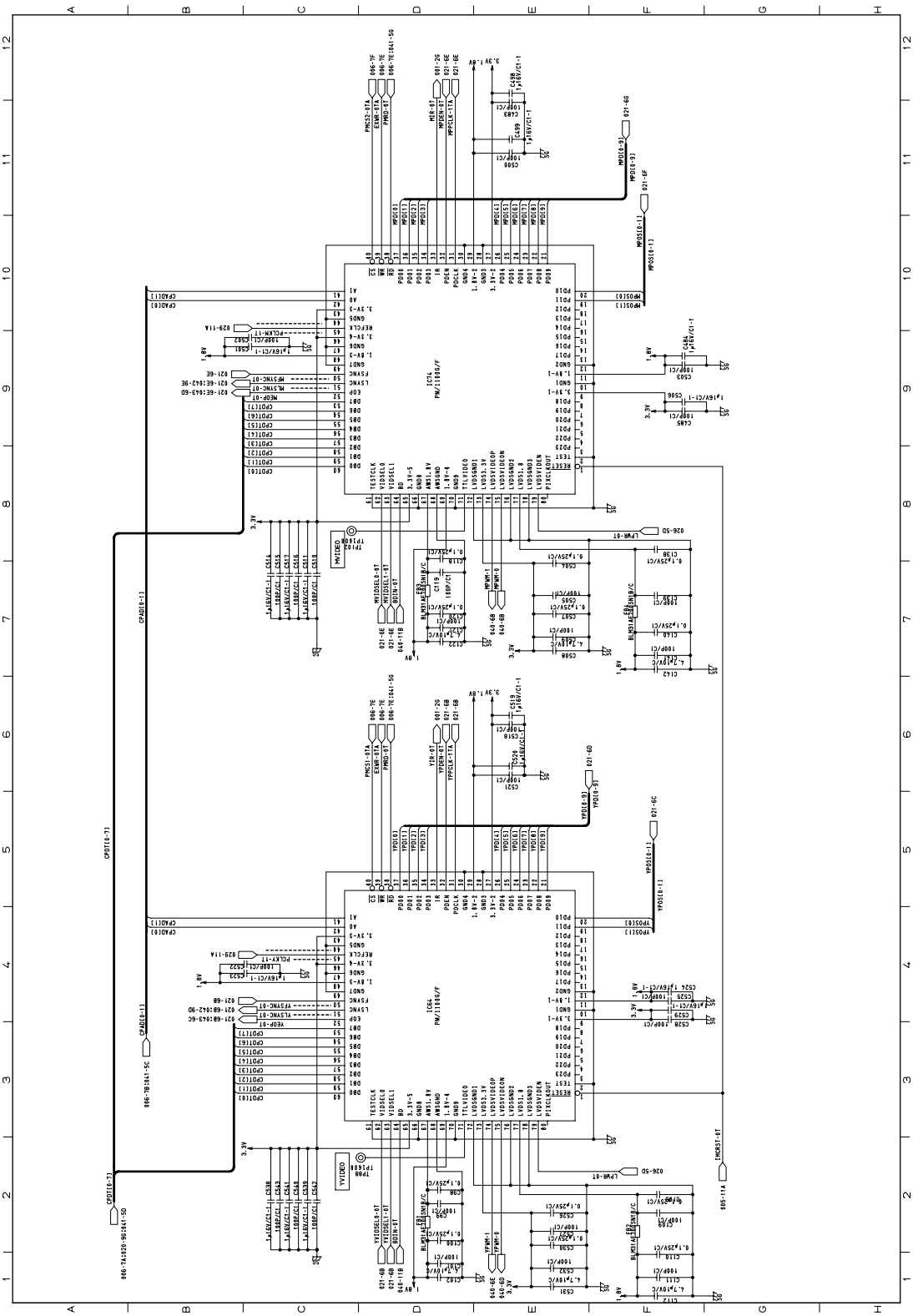

Fig. 3-48

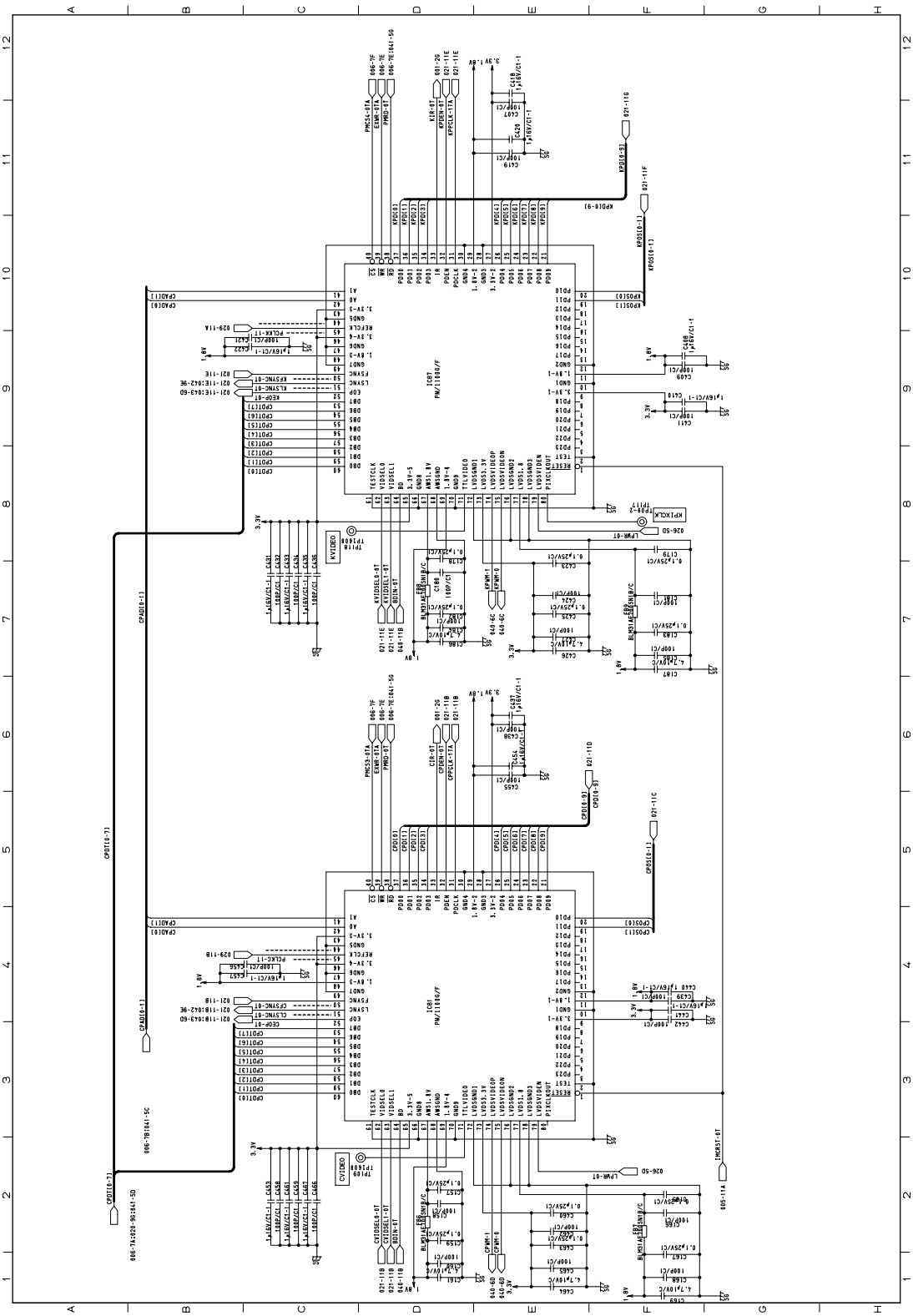

Fig. 3-49

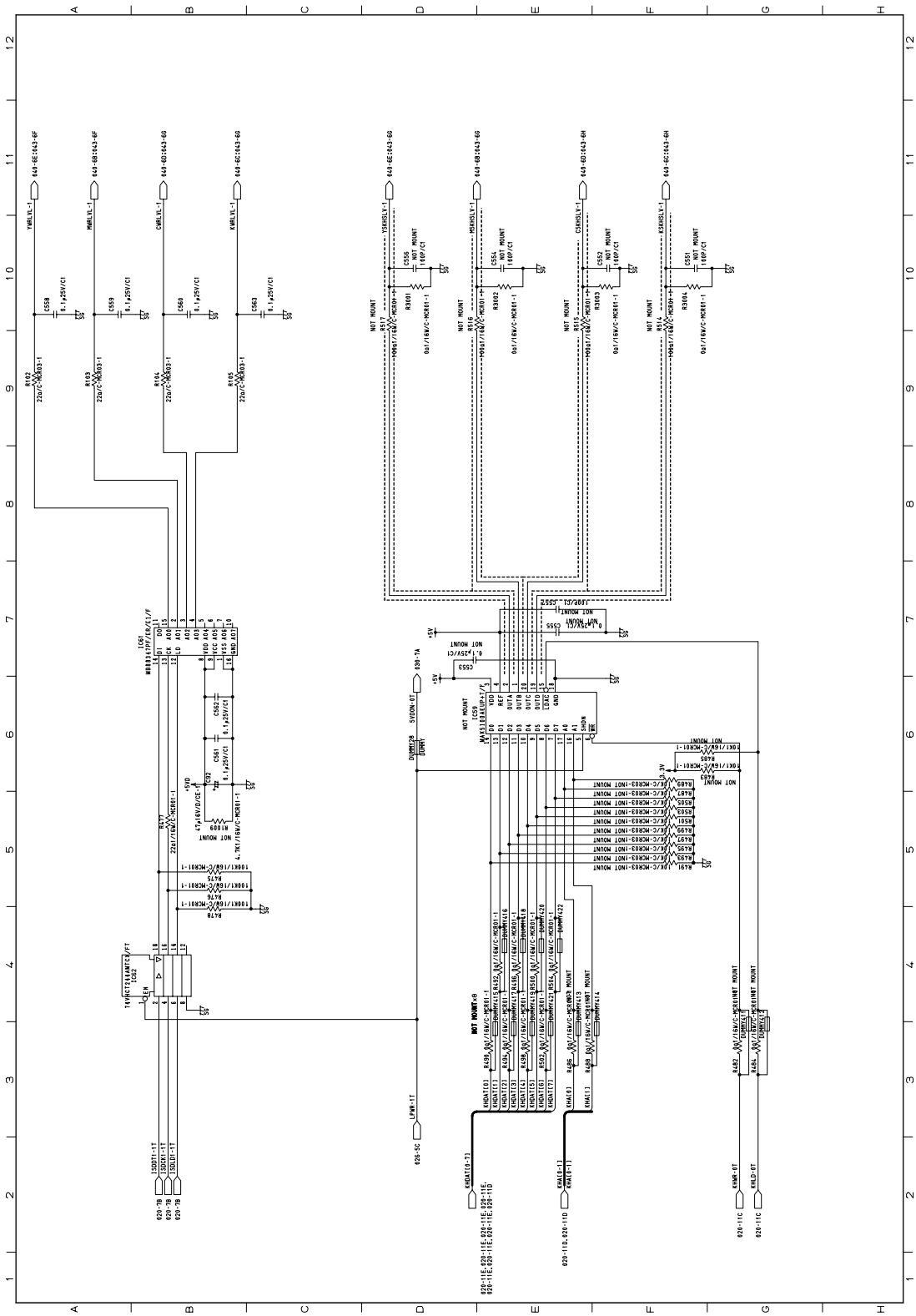

Fig. 3-50

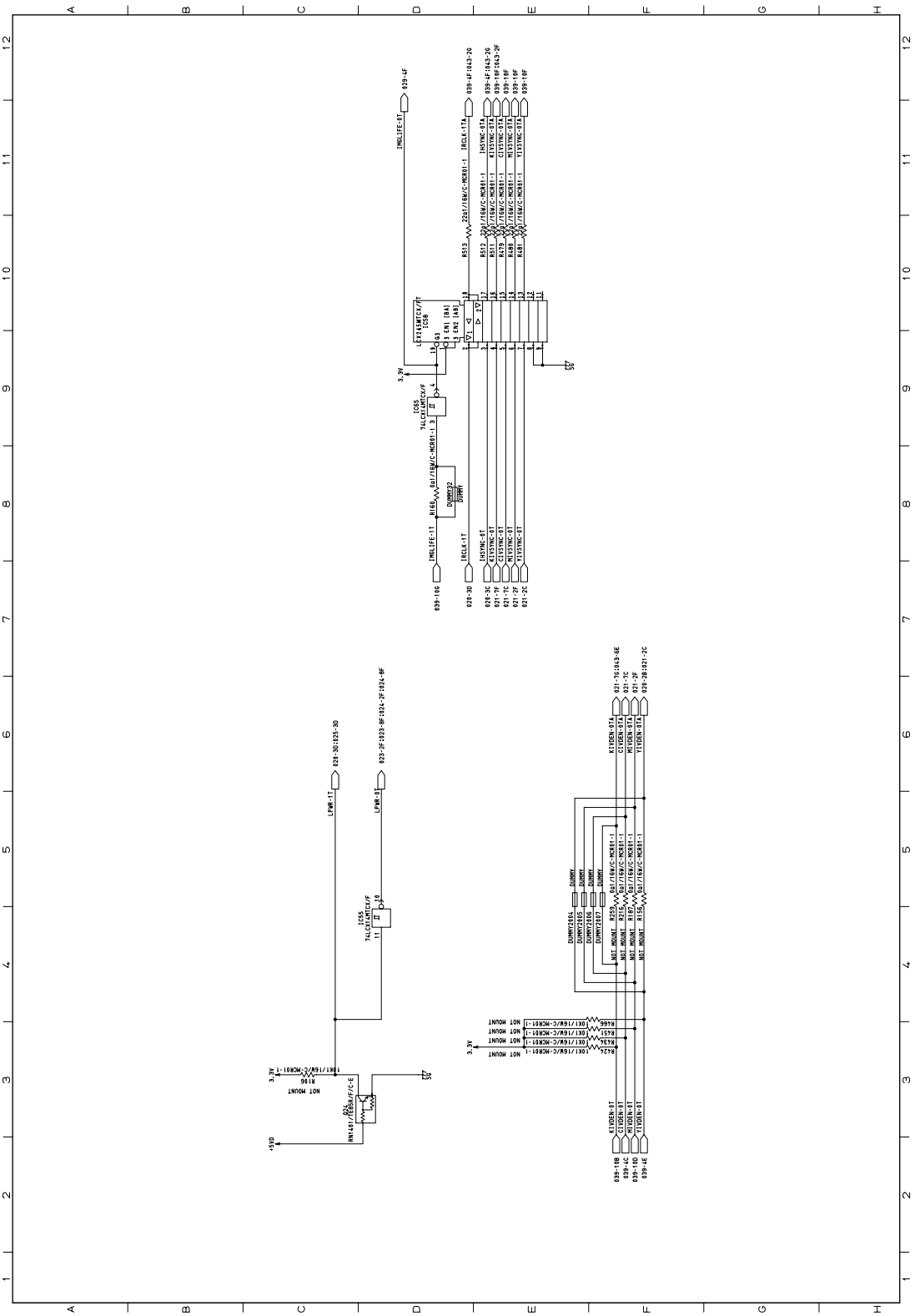

Fig. 3-51

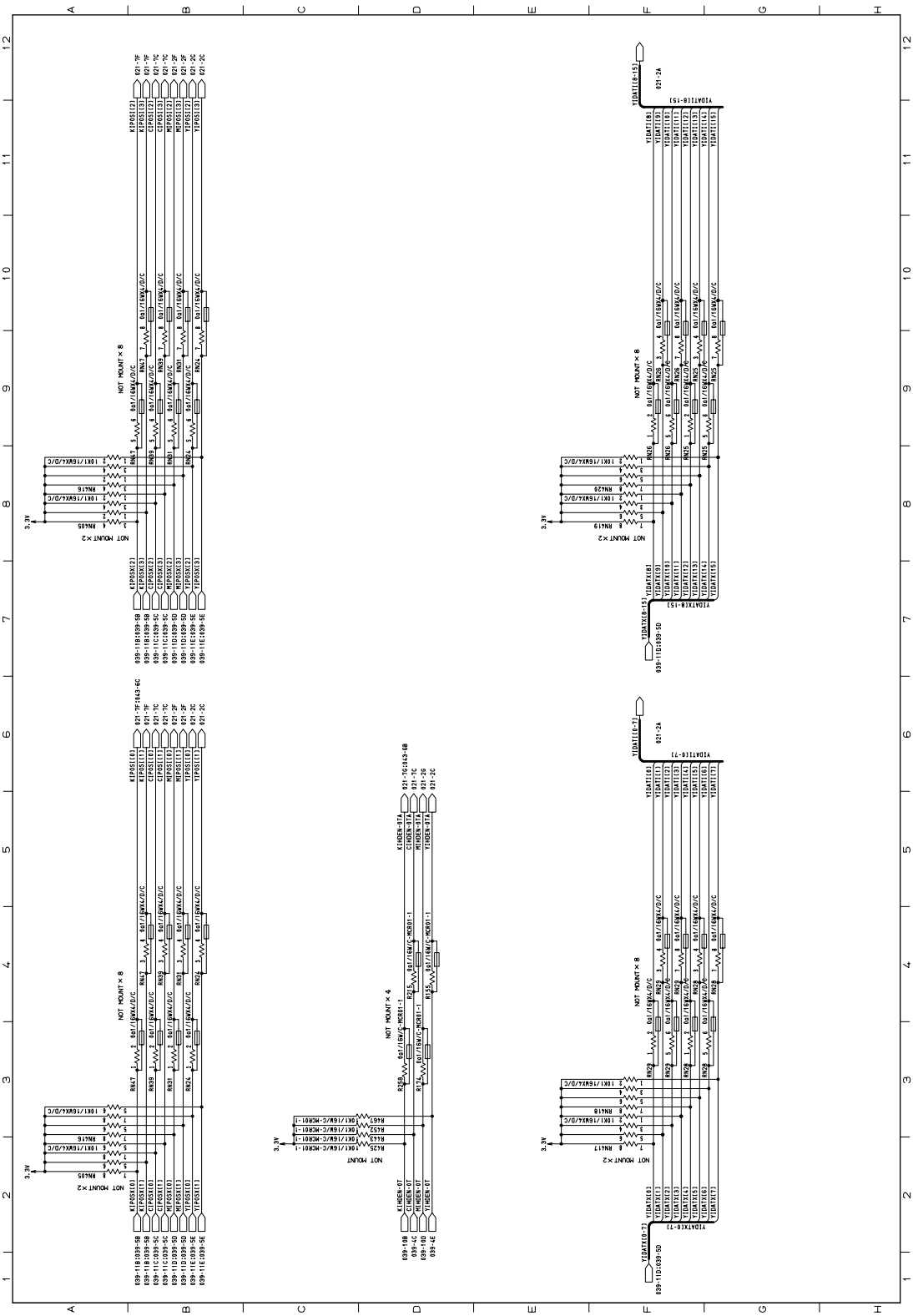

Fig. 3-52

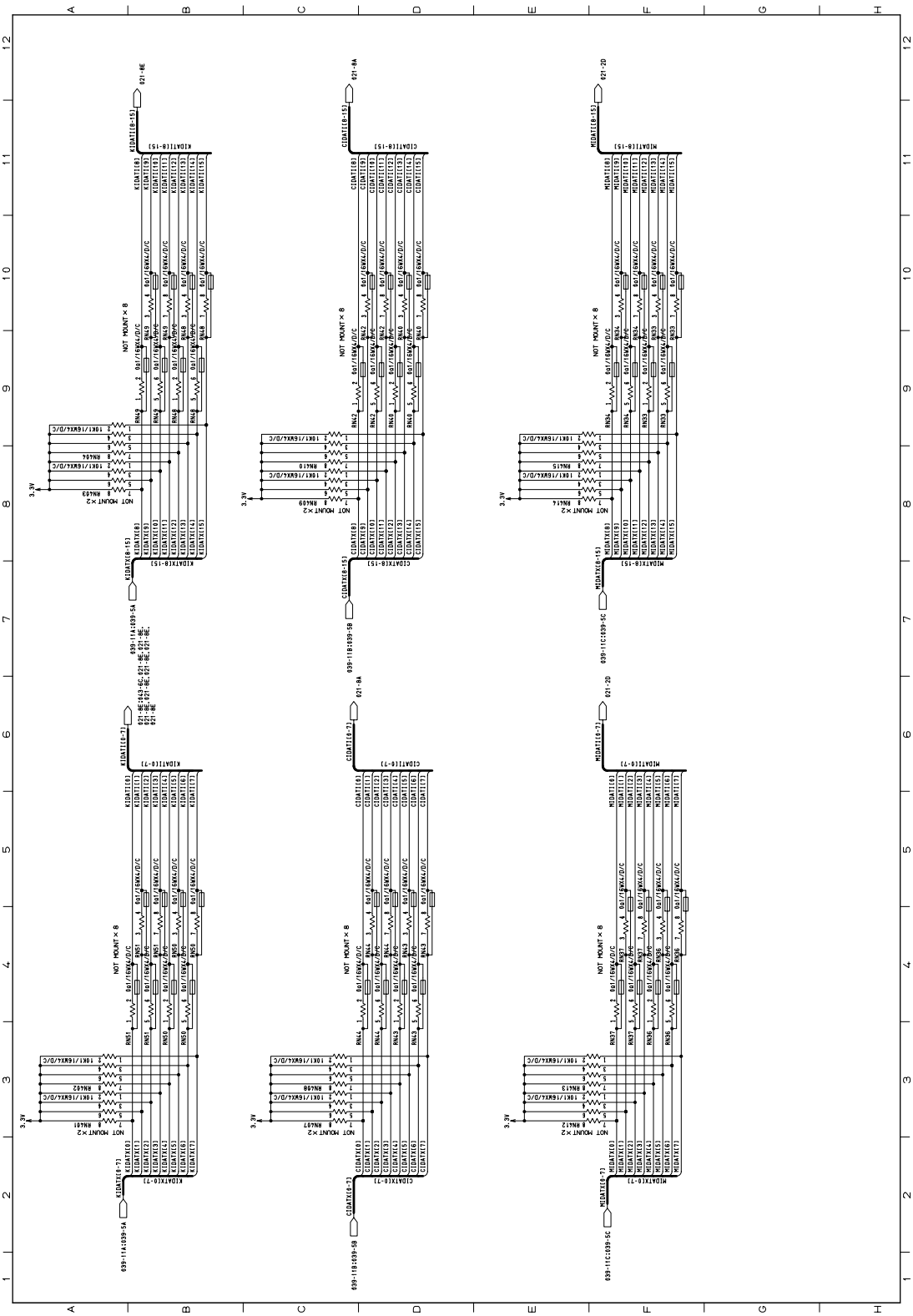

Fig. 3-53

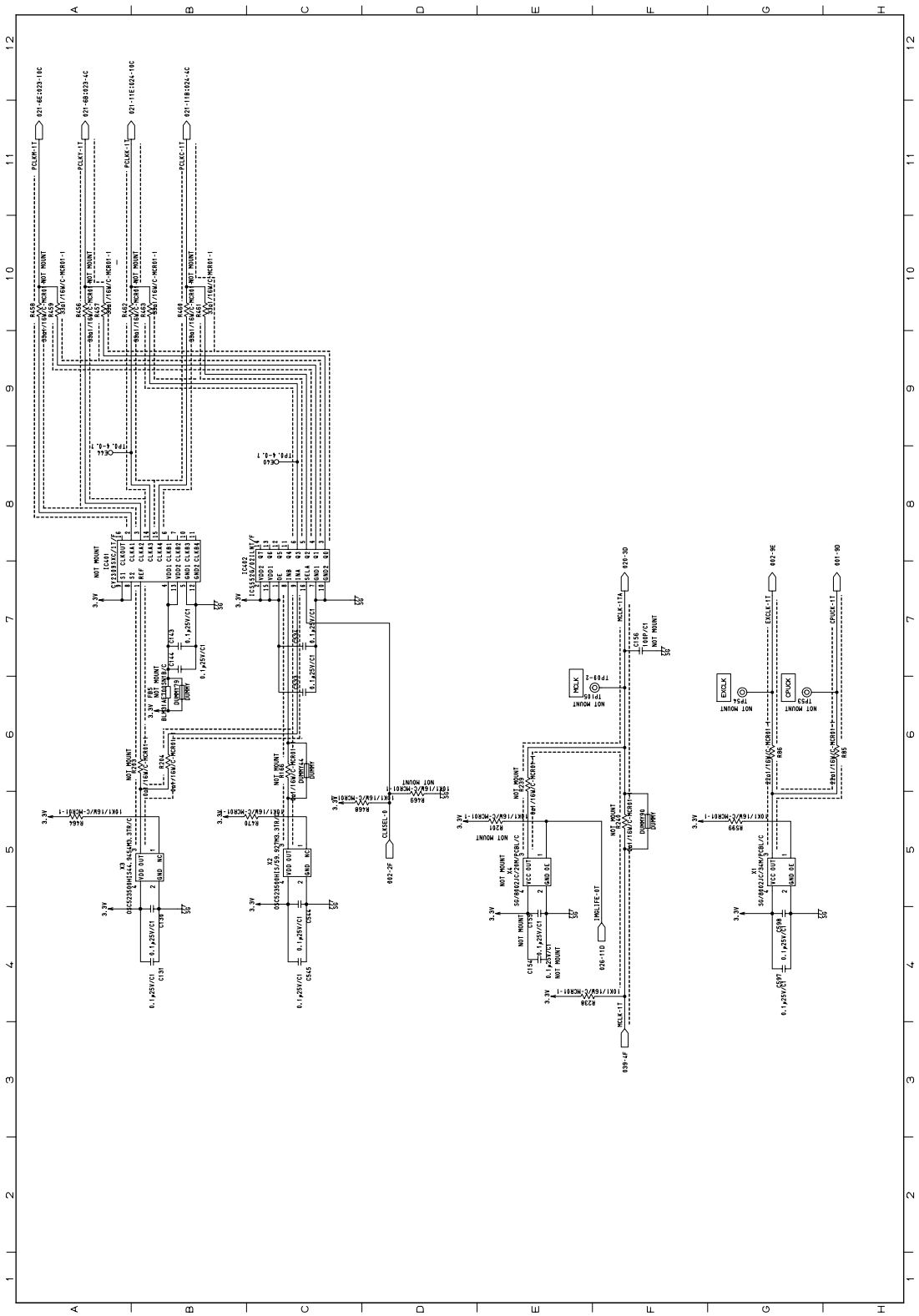

Fig. 3-54

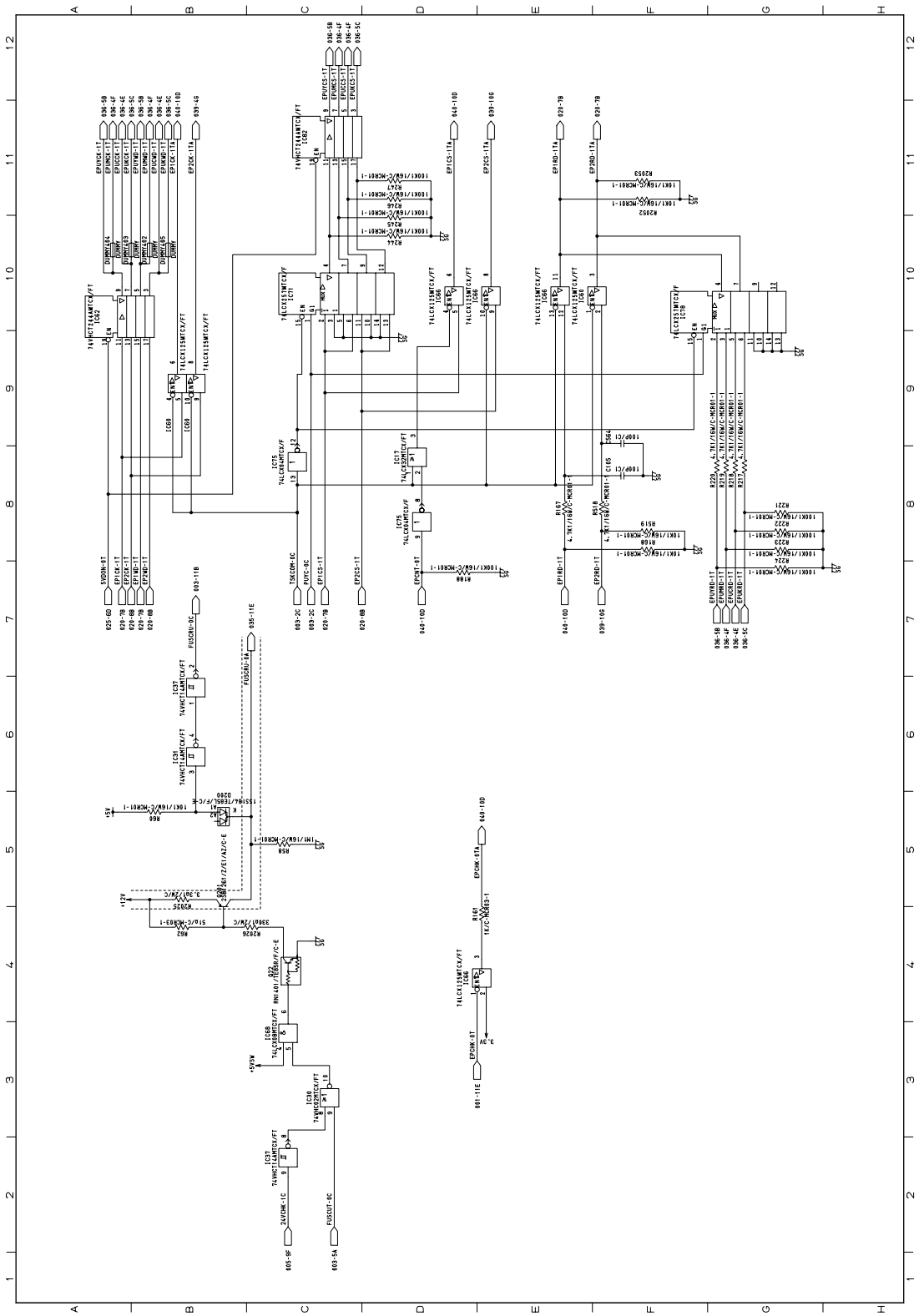

Fig. 3-55

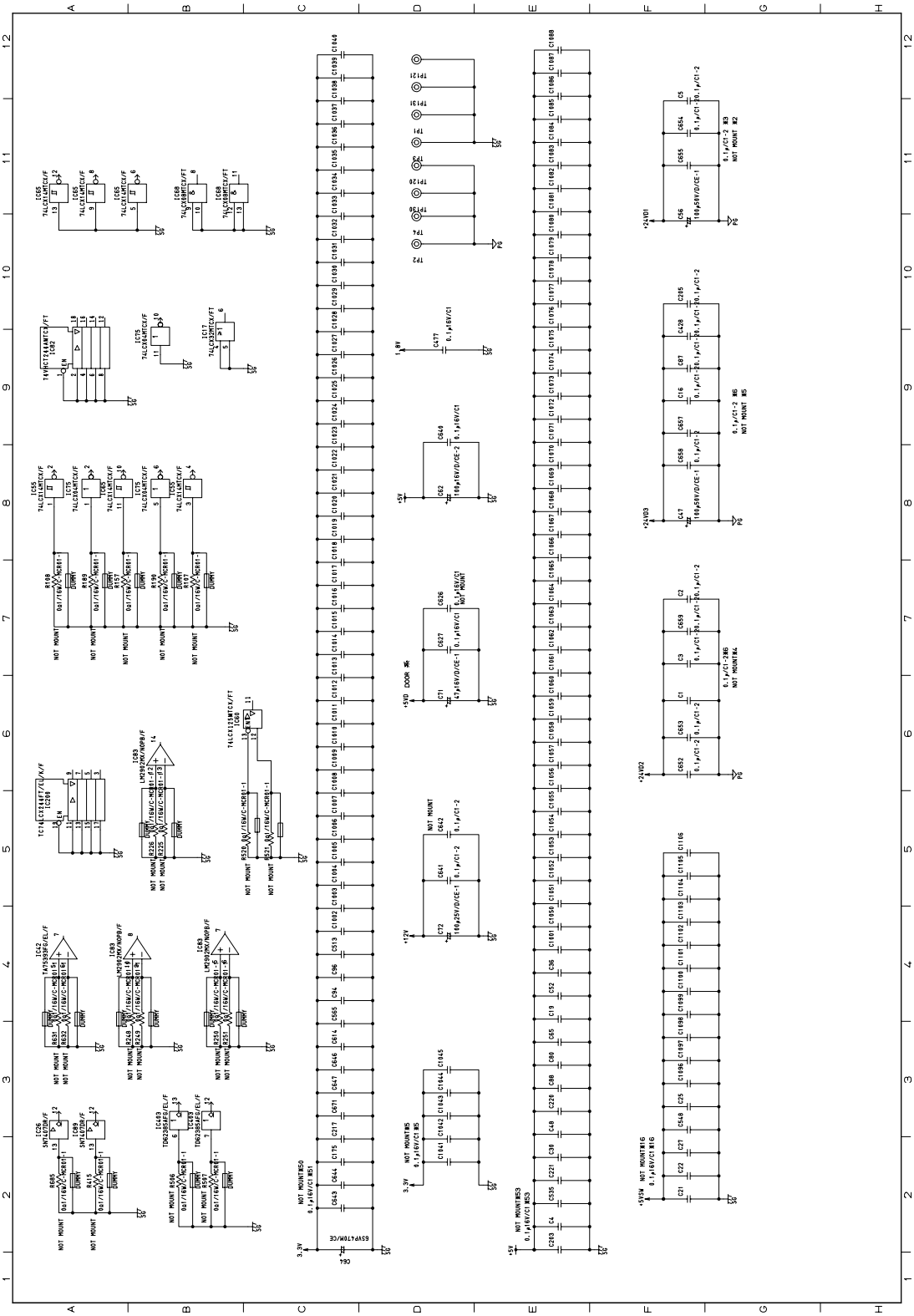

Fig. 3-56

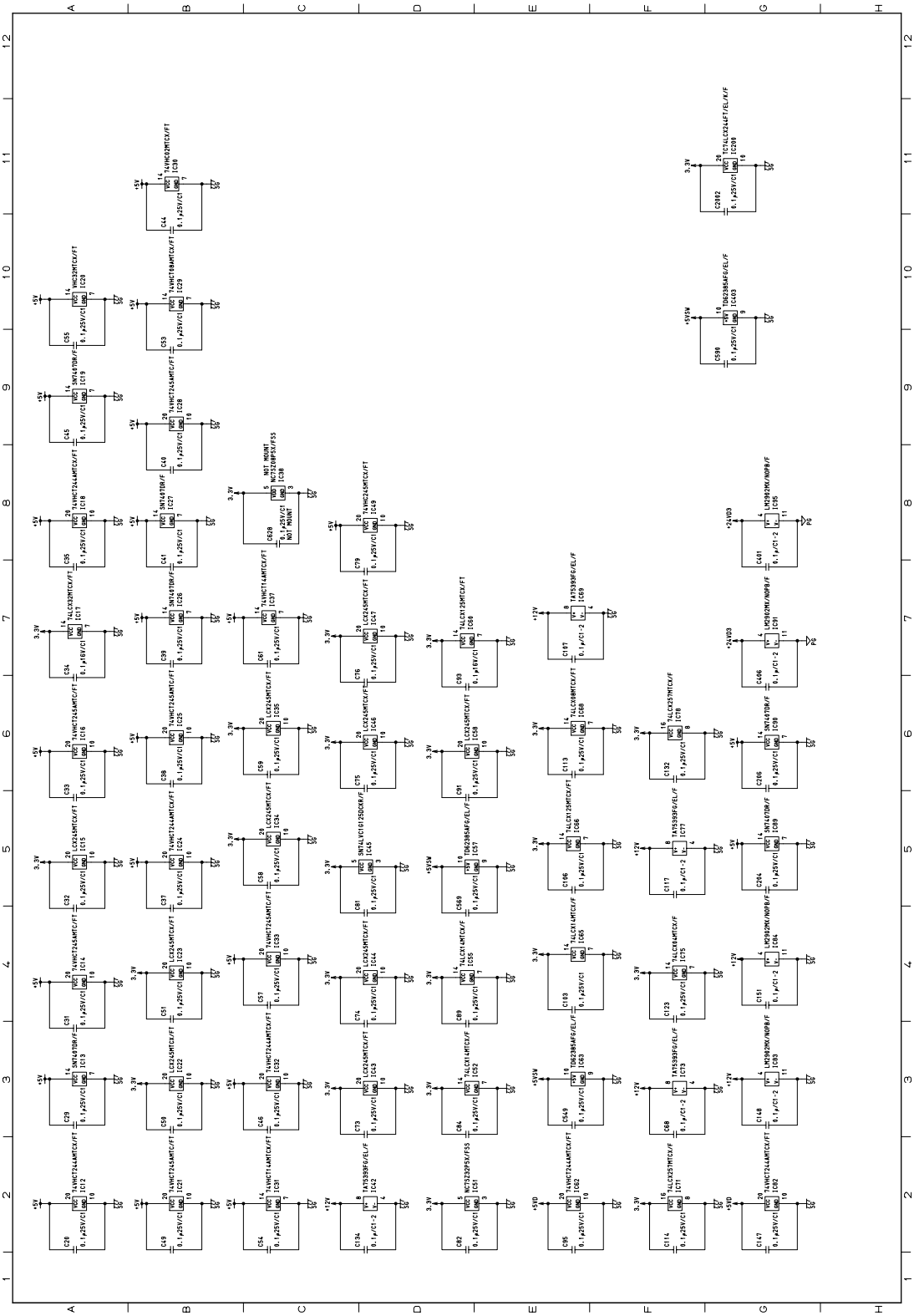

Fig. 3-57

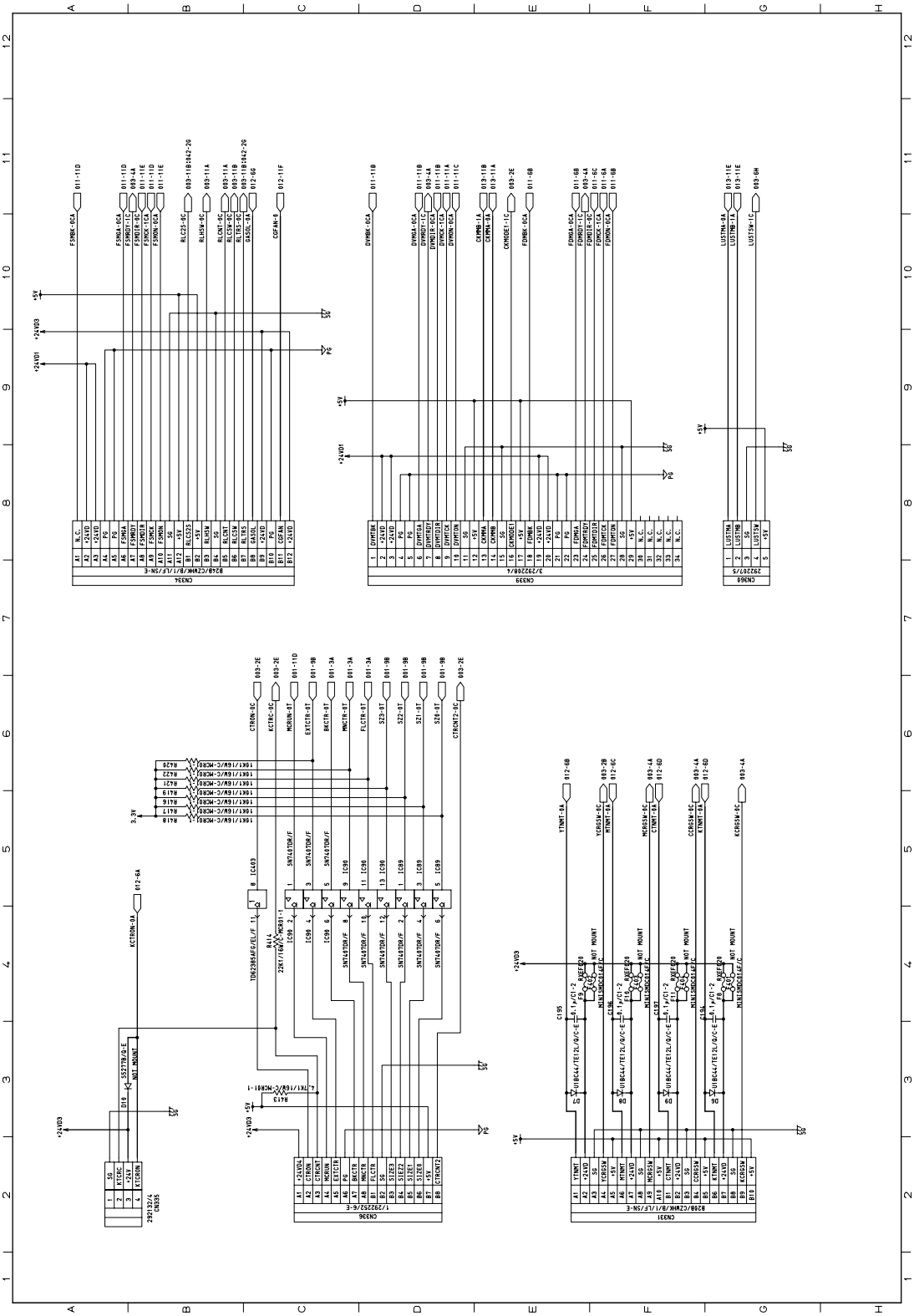

Fig. 3-58

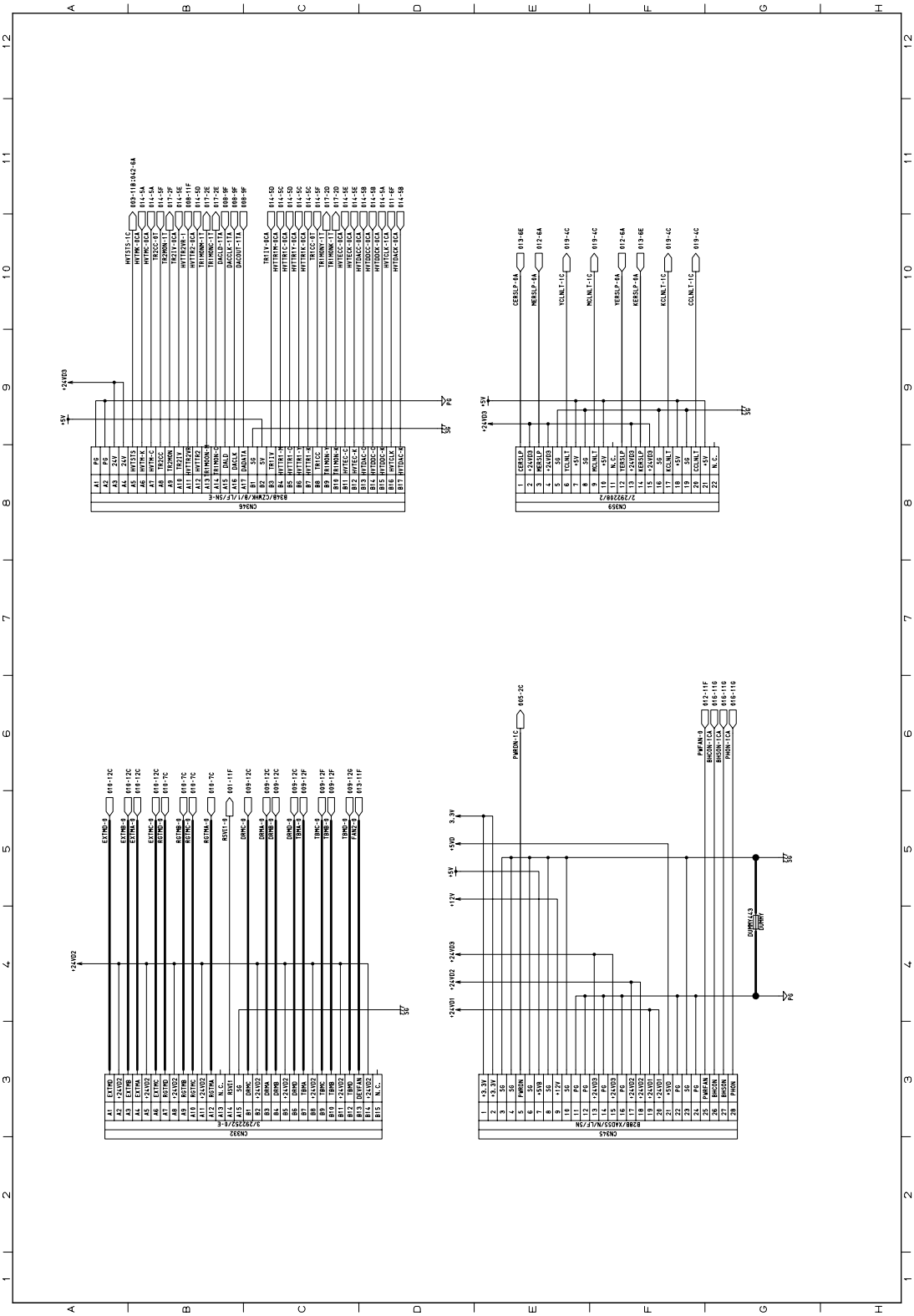

Fig. 3-59

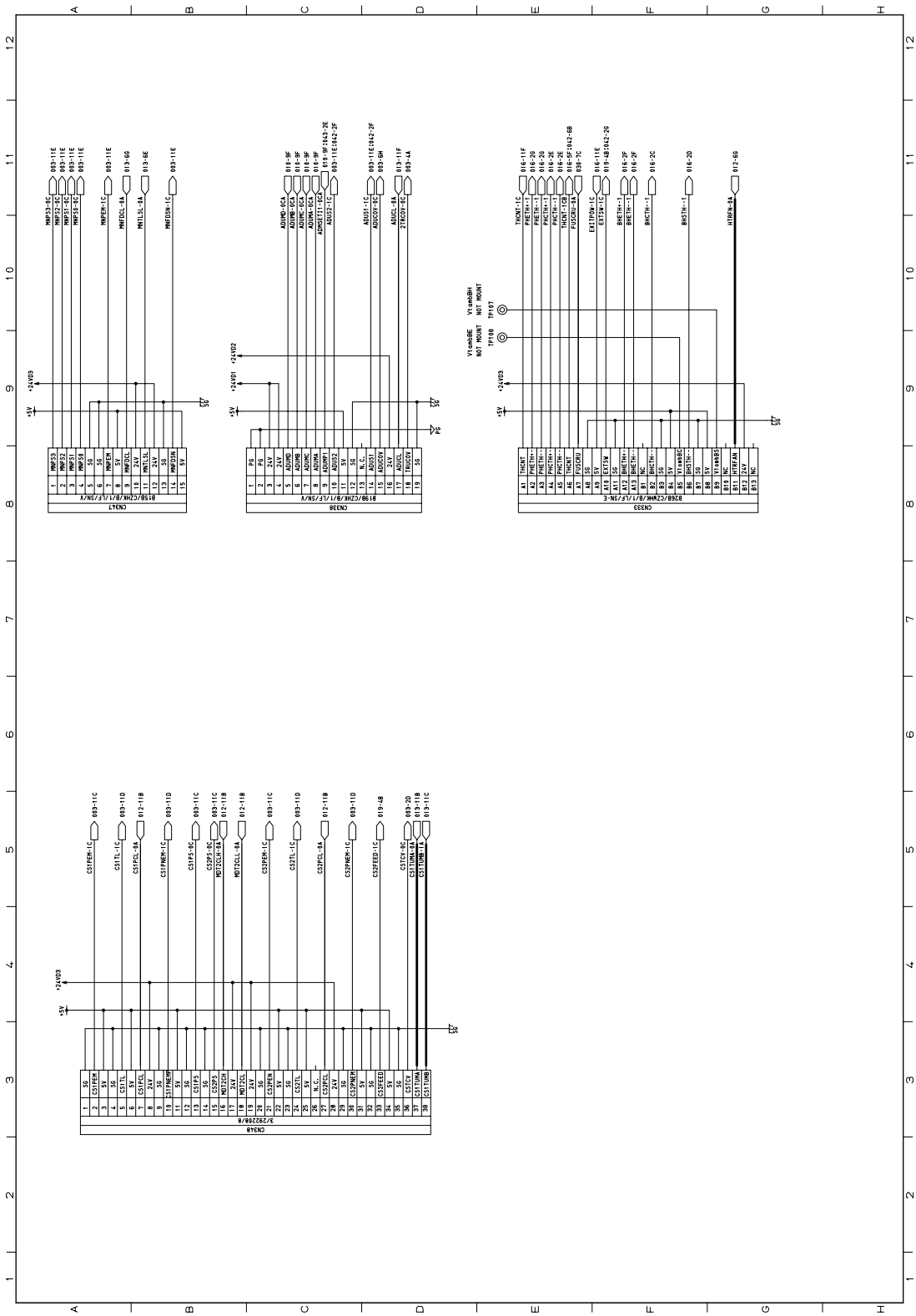

Fig. 3-60

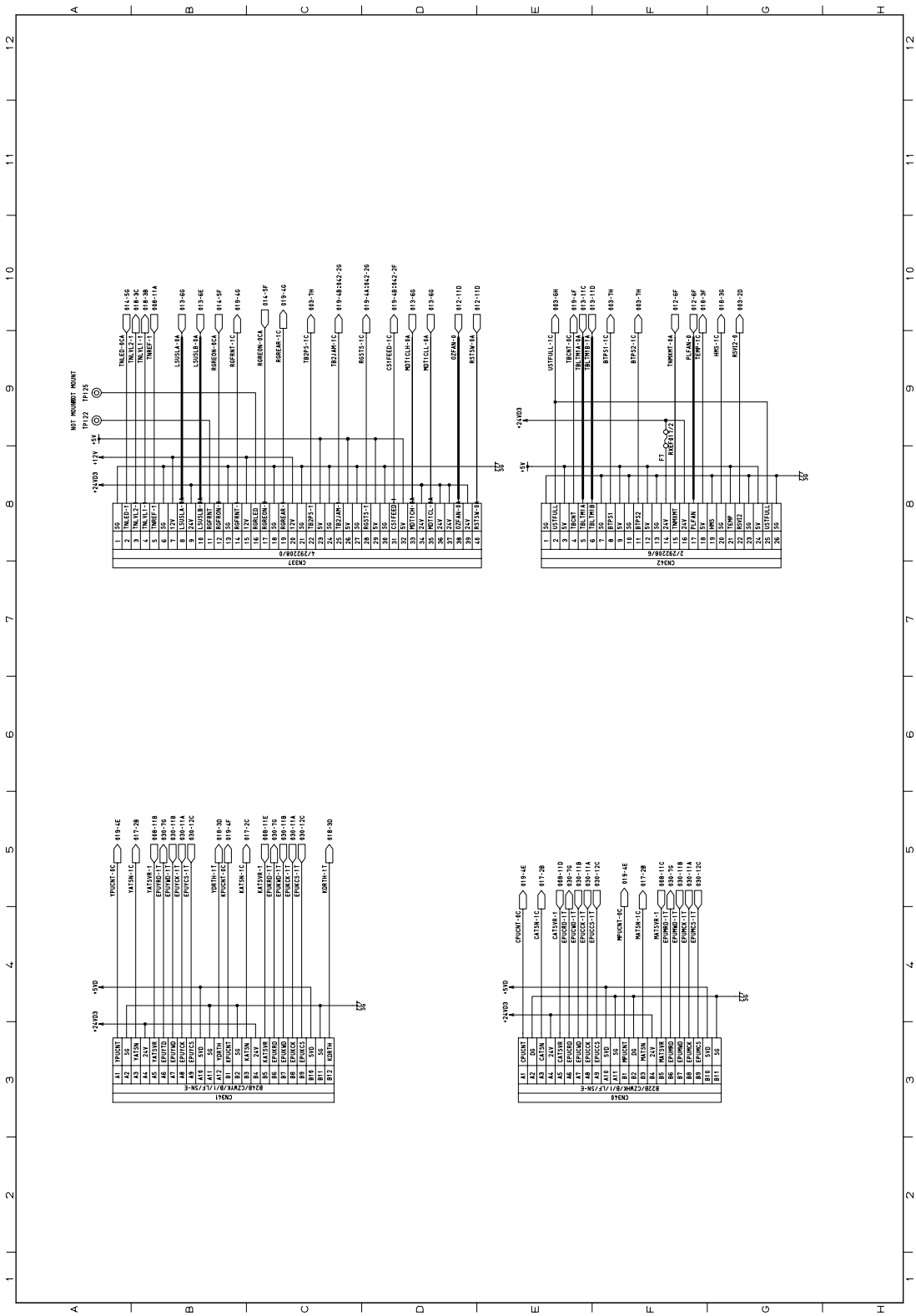

Fig. 3-61

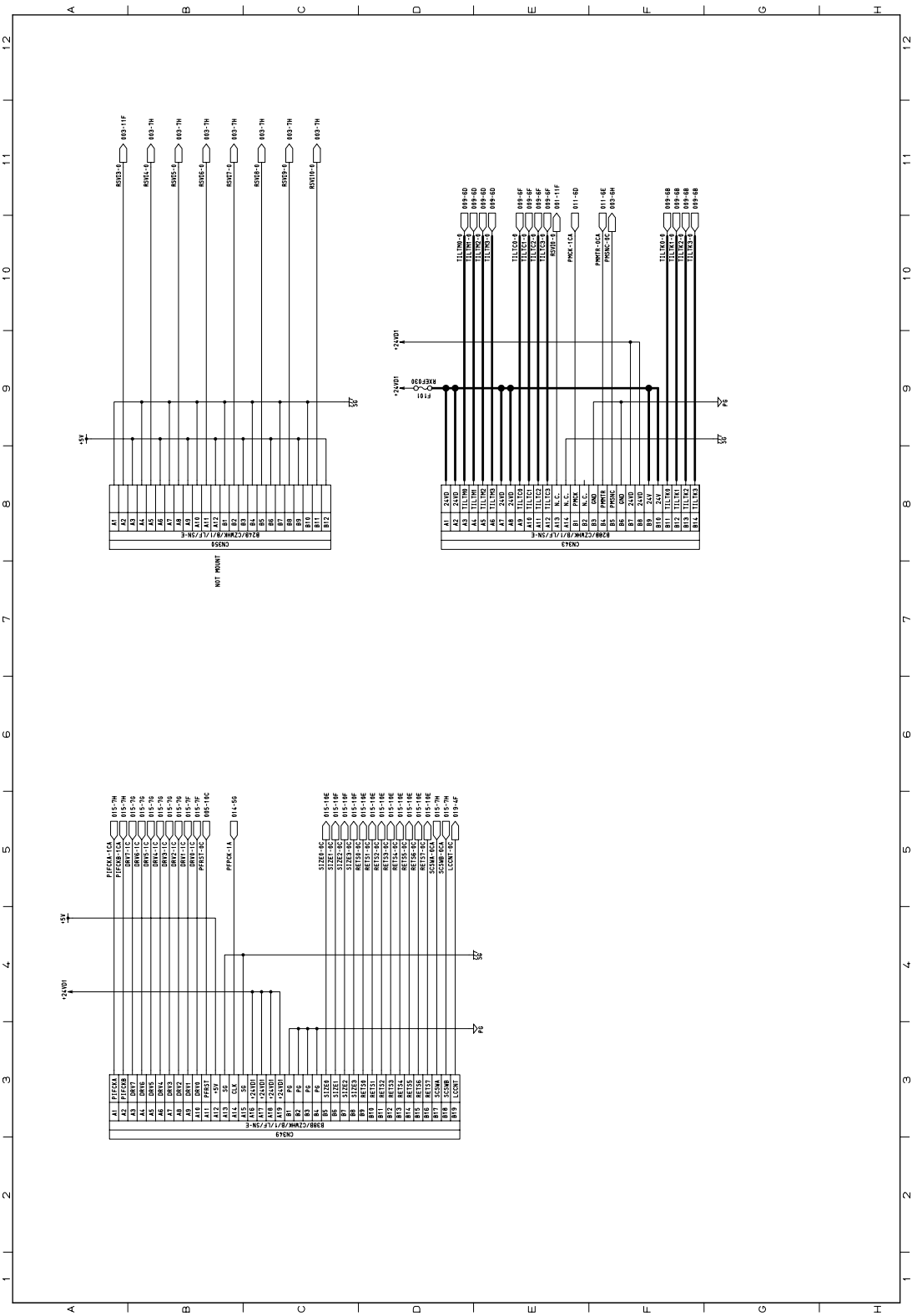

Fig. 3-62

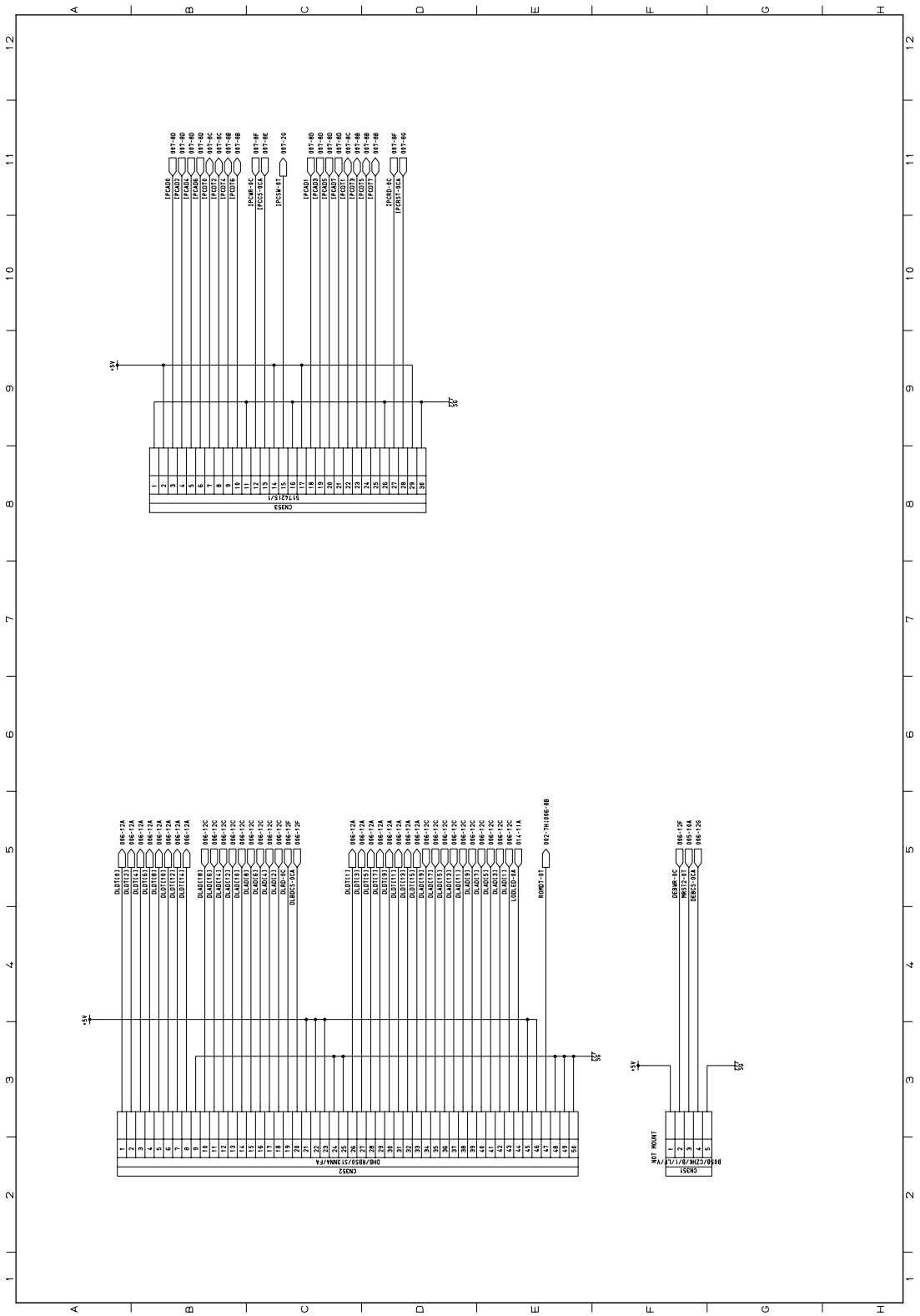

Fig. 3-63

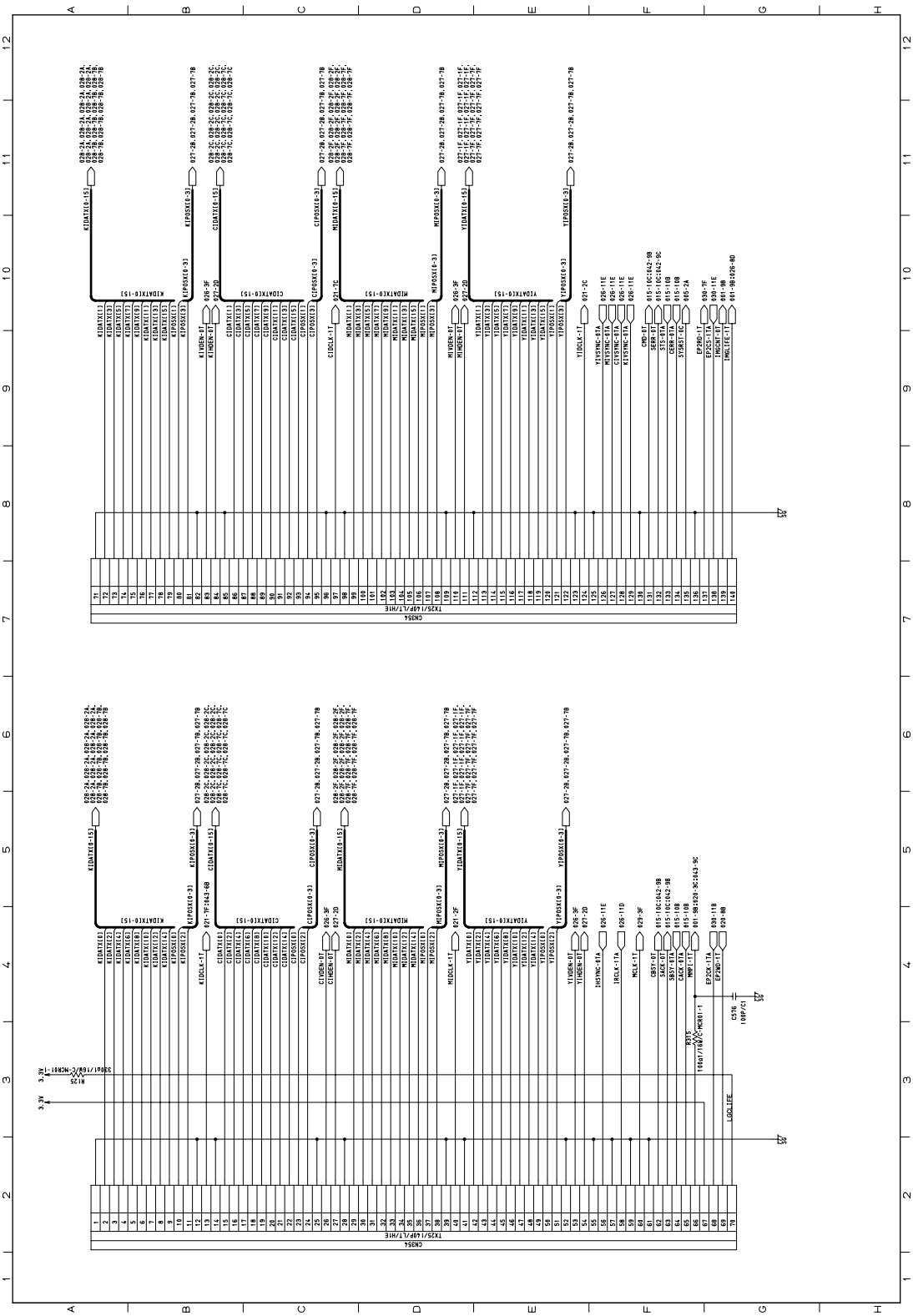

Fig. 3-64

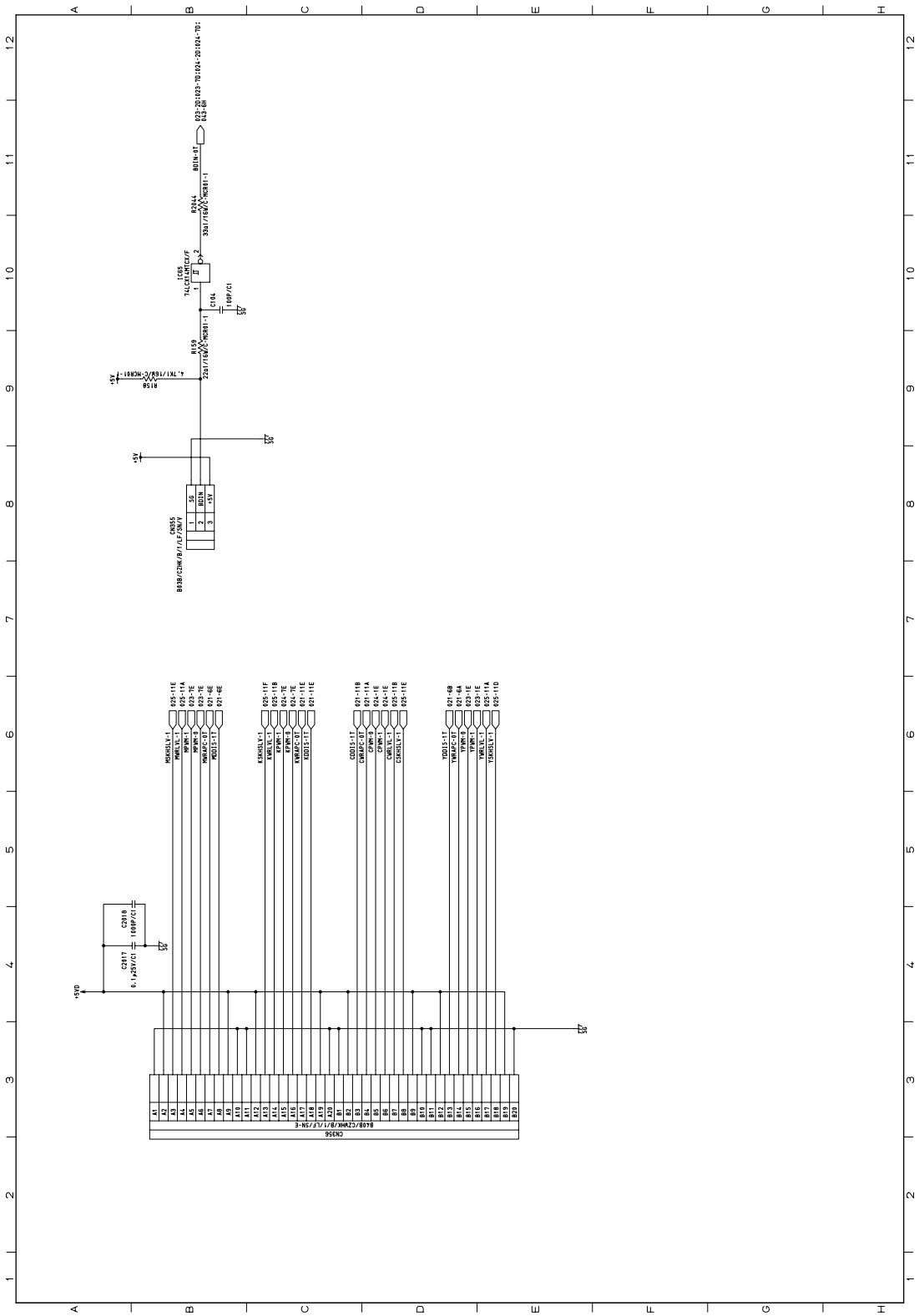

Fig. 3-65

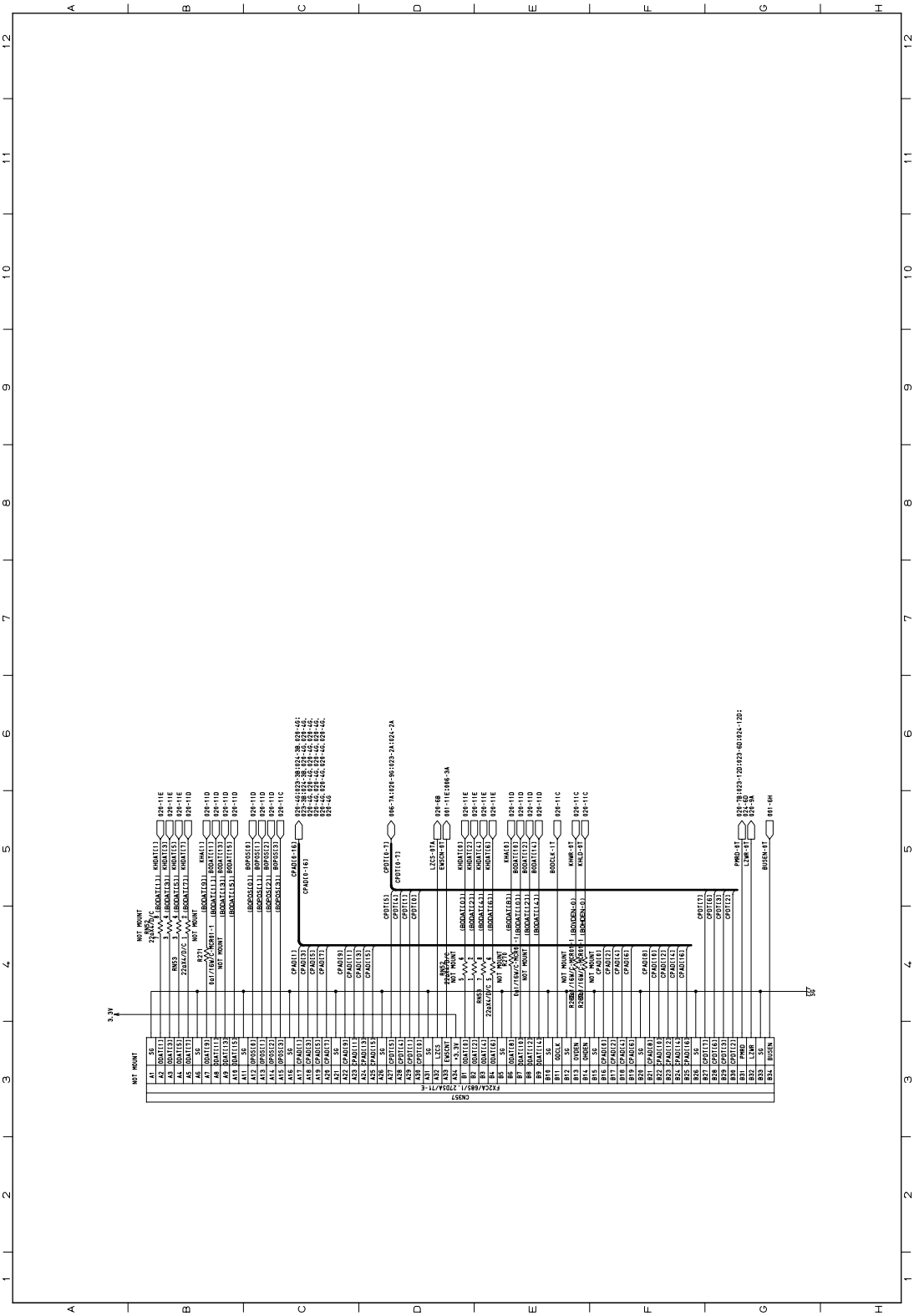

Fig. 3-66

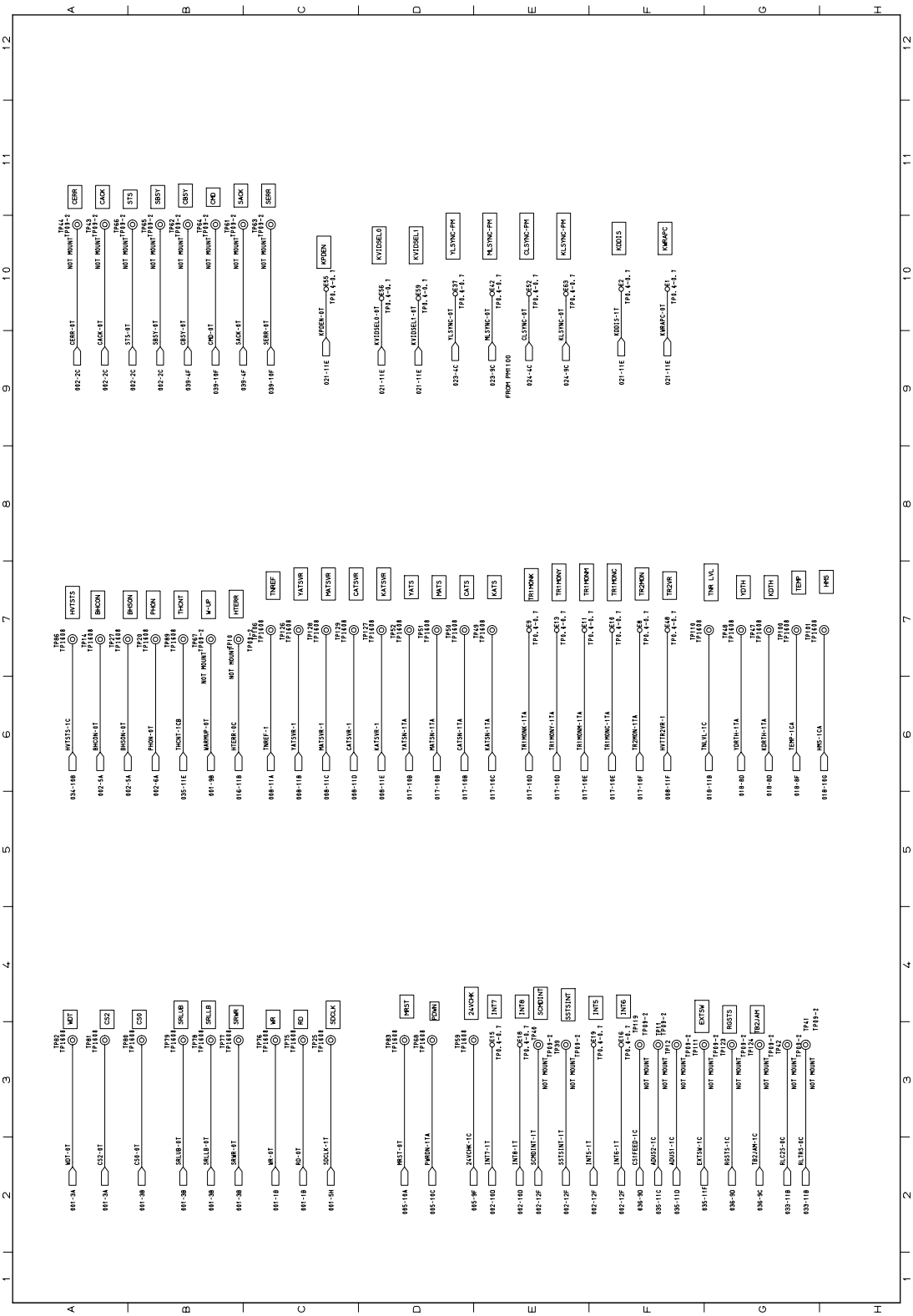

Fig. 3-67

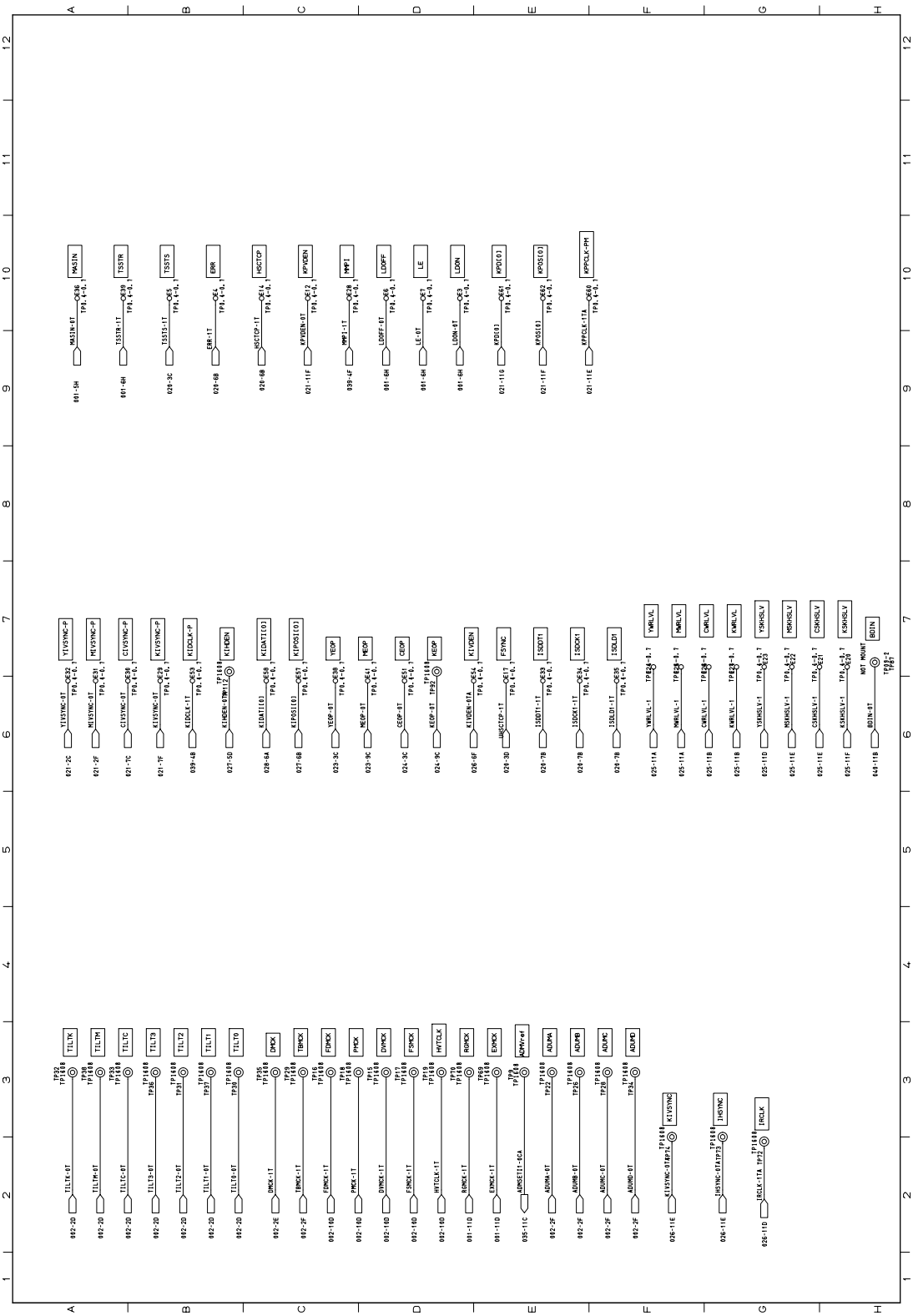

Fig. 3-68

3.4 Imaging processing circuit (IMG board)

IMG board 1/23

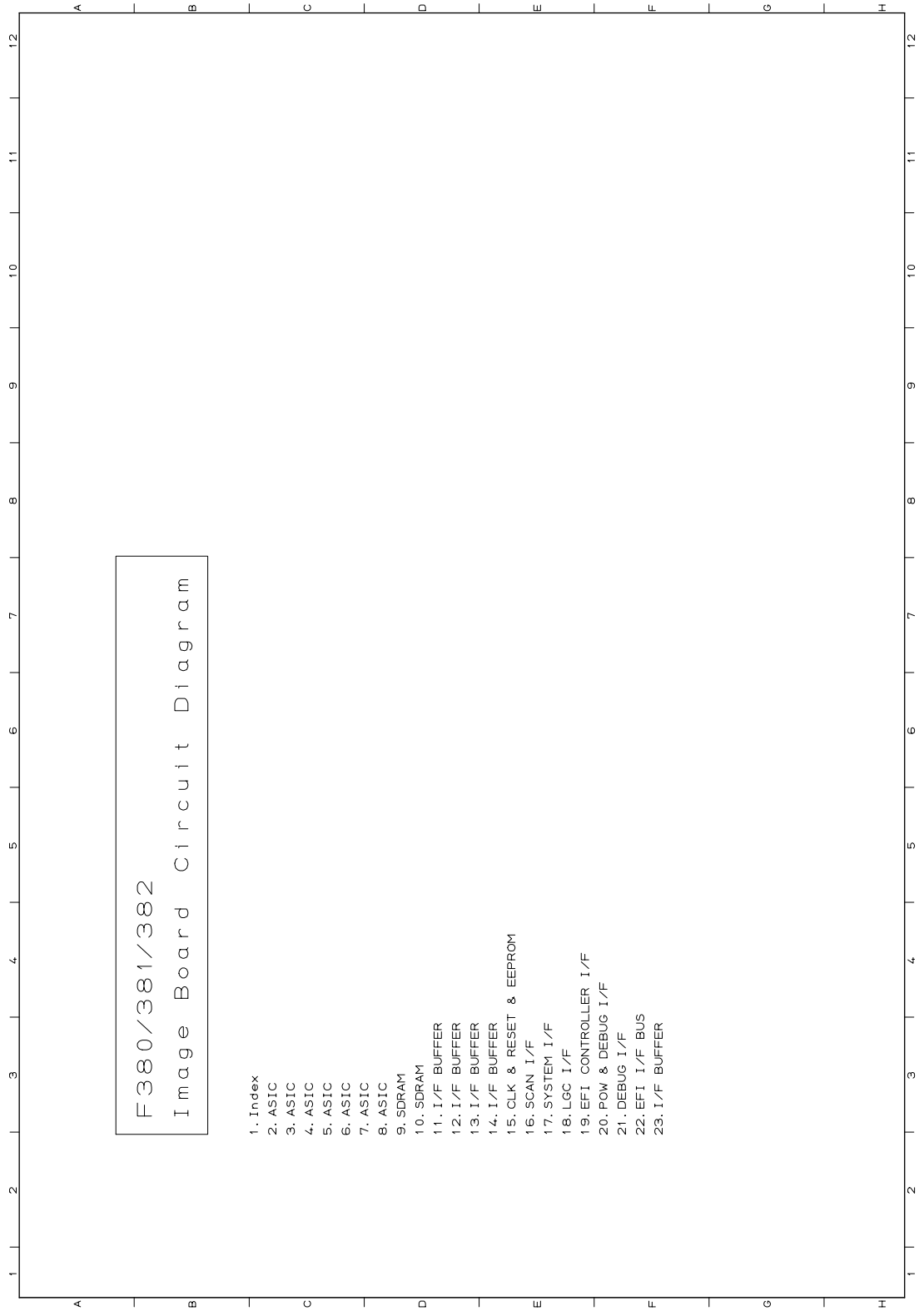

Fig. 3-69

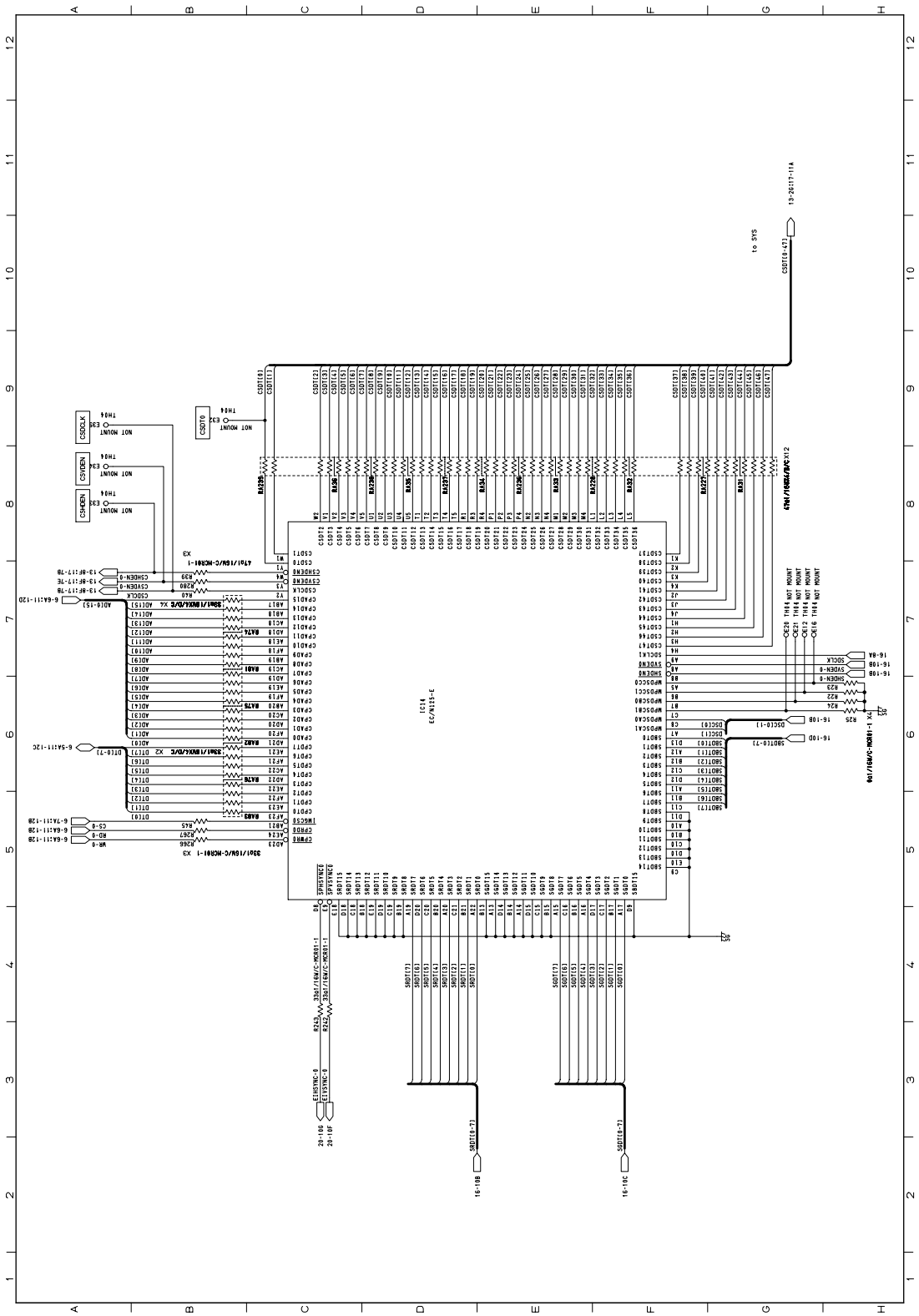

Fig. 3-70

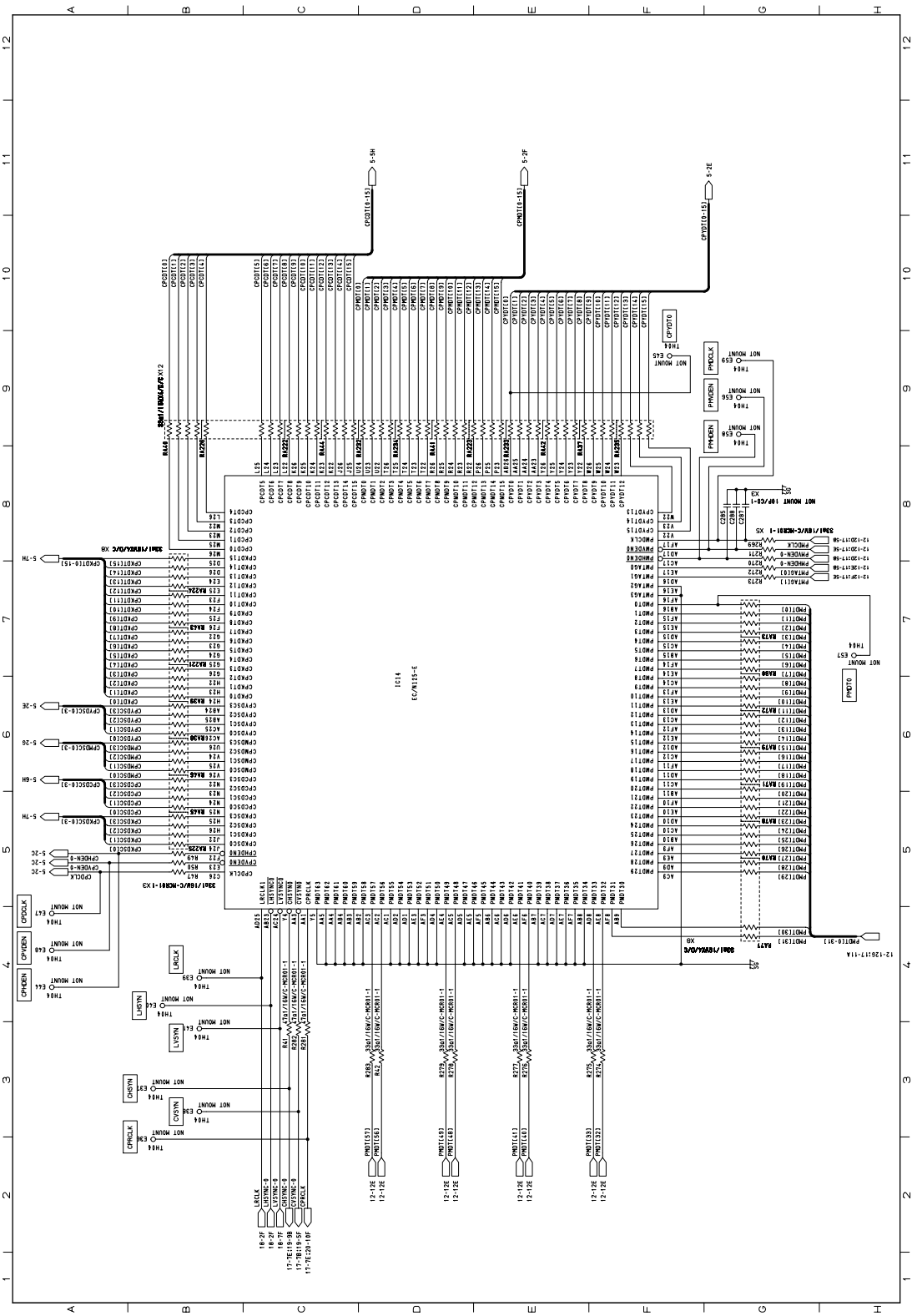

Fig. 3-71

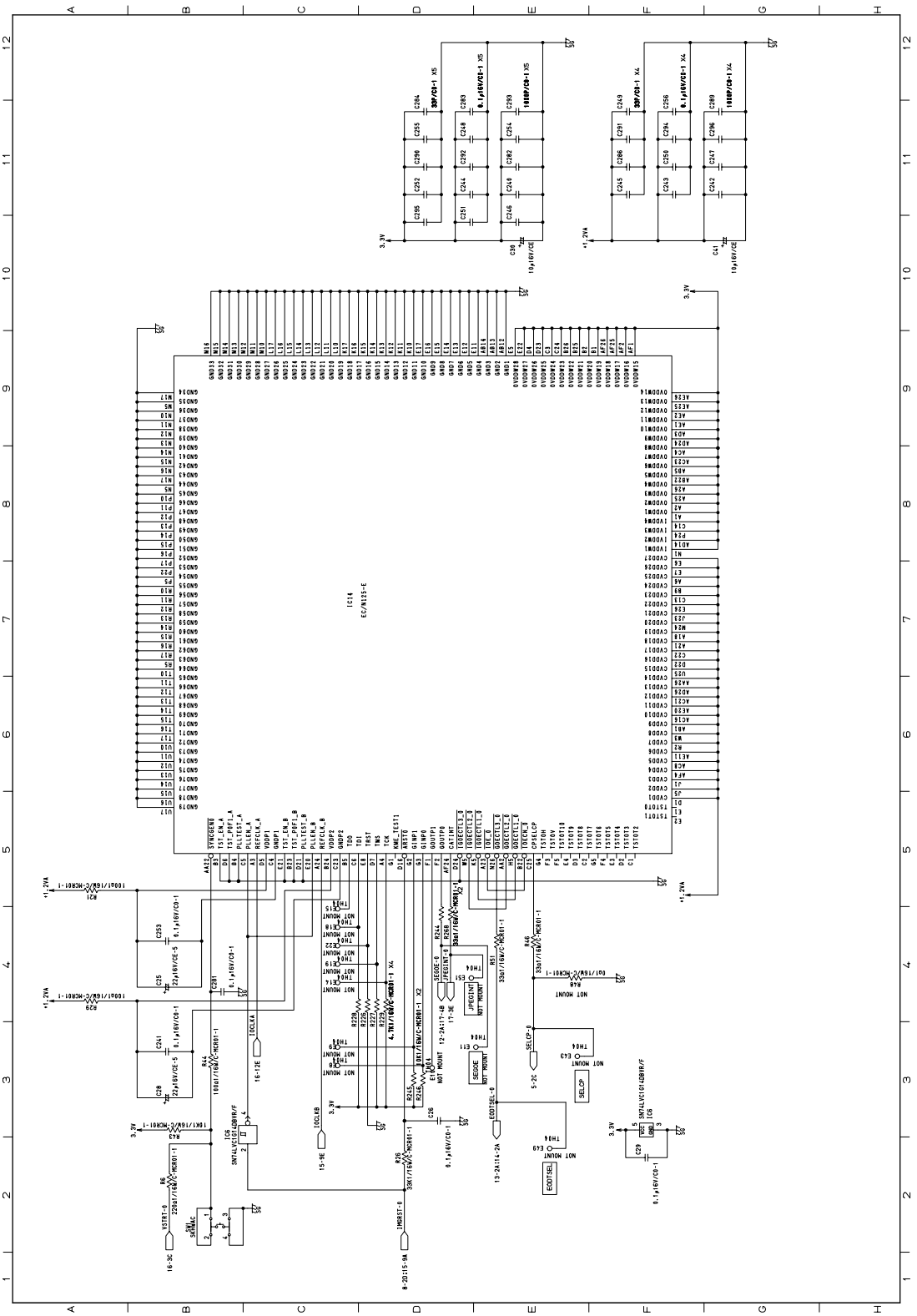

Fig. 3-72

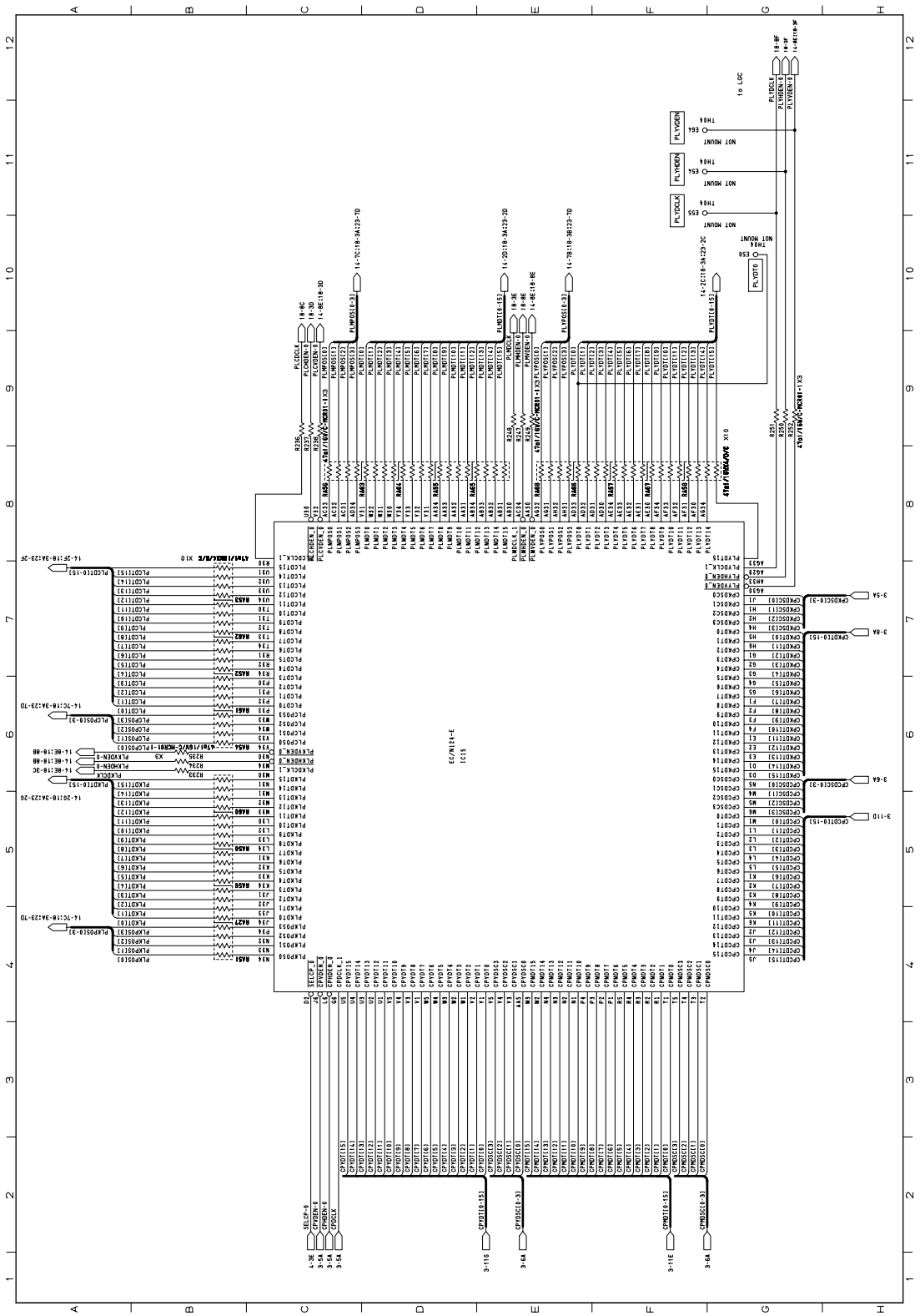

Fig. 3-73

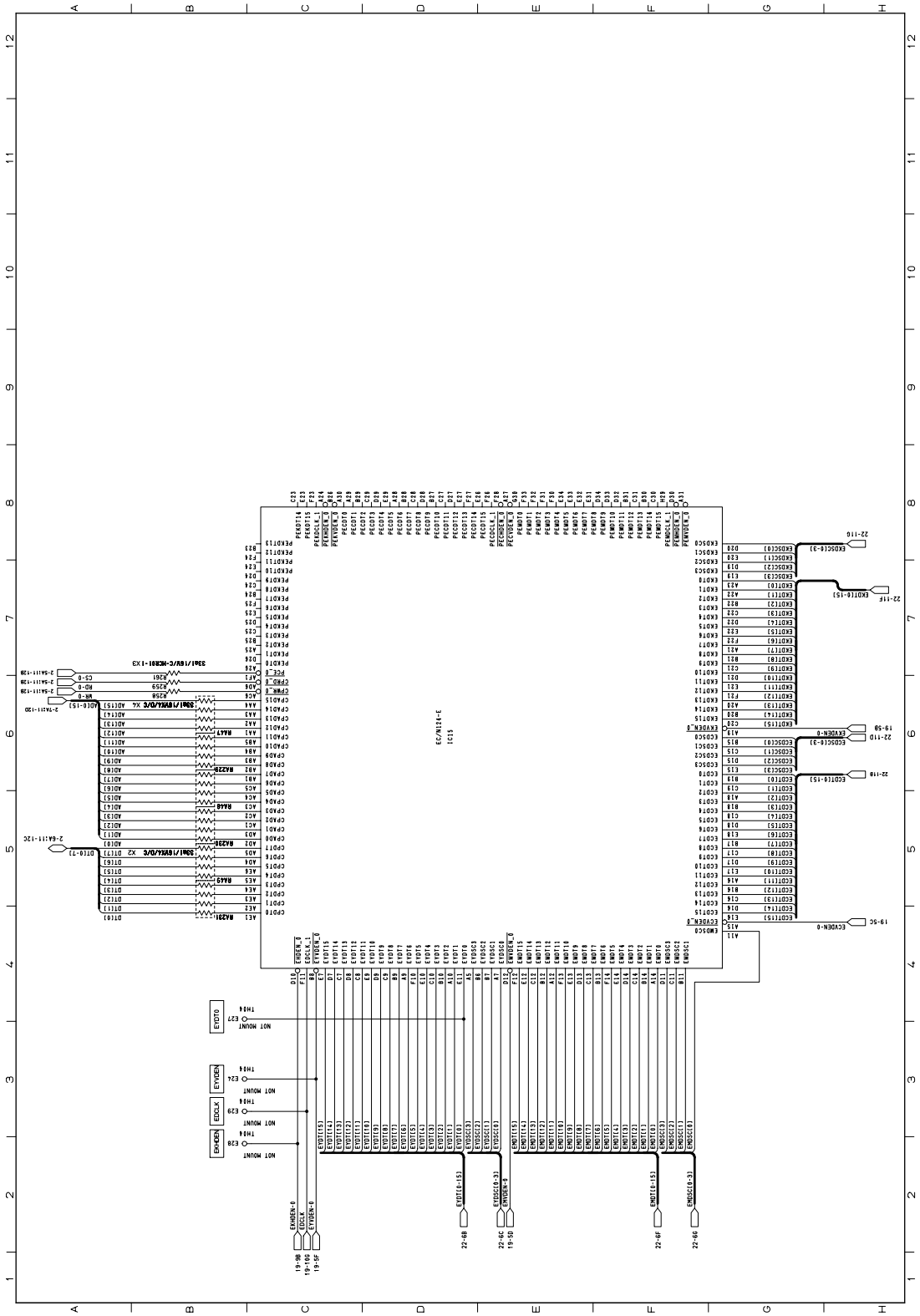

Fig. 3-74

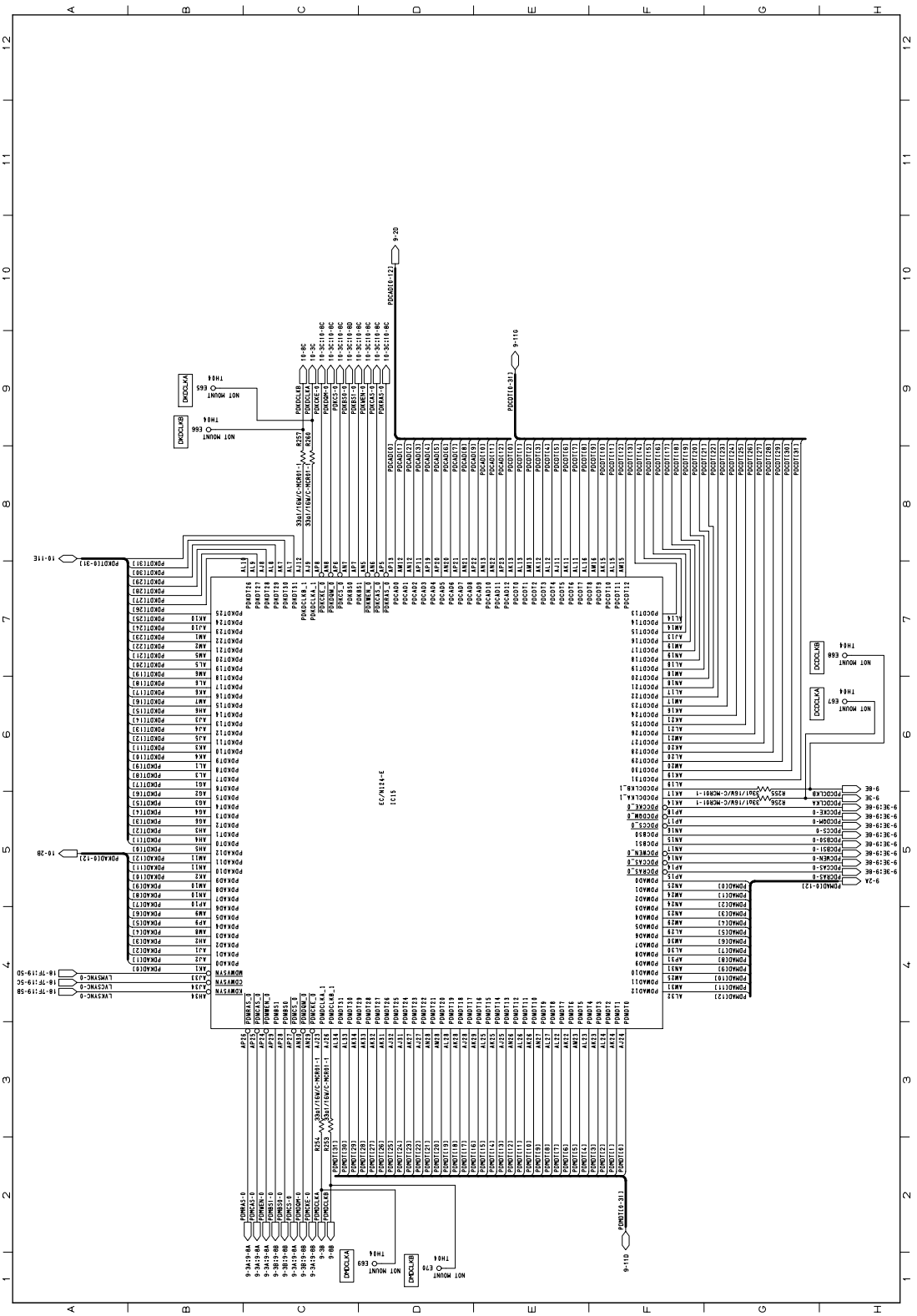

Fig. 3-75

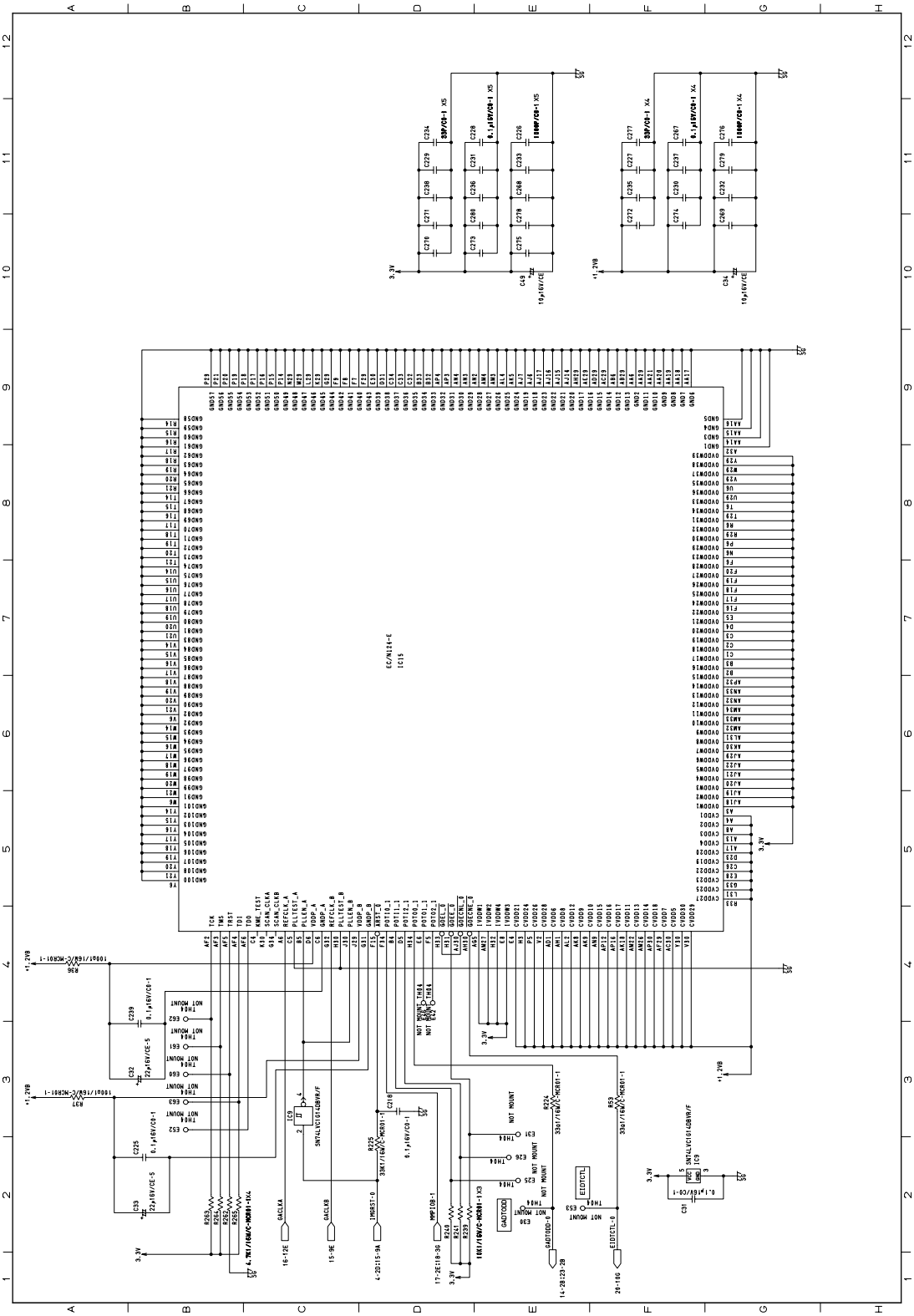

Fig. 3-76

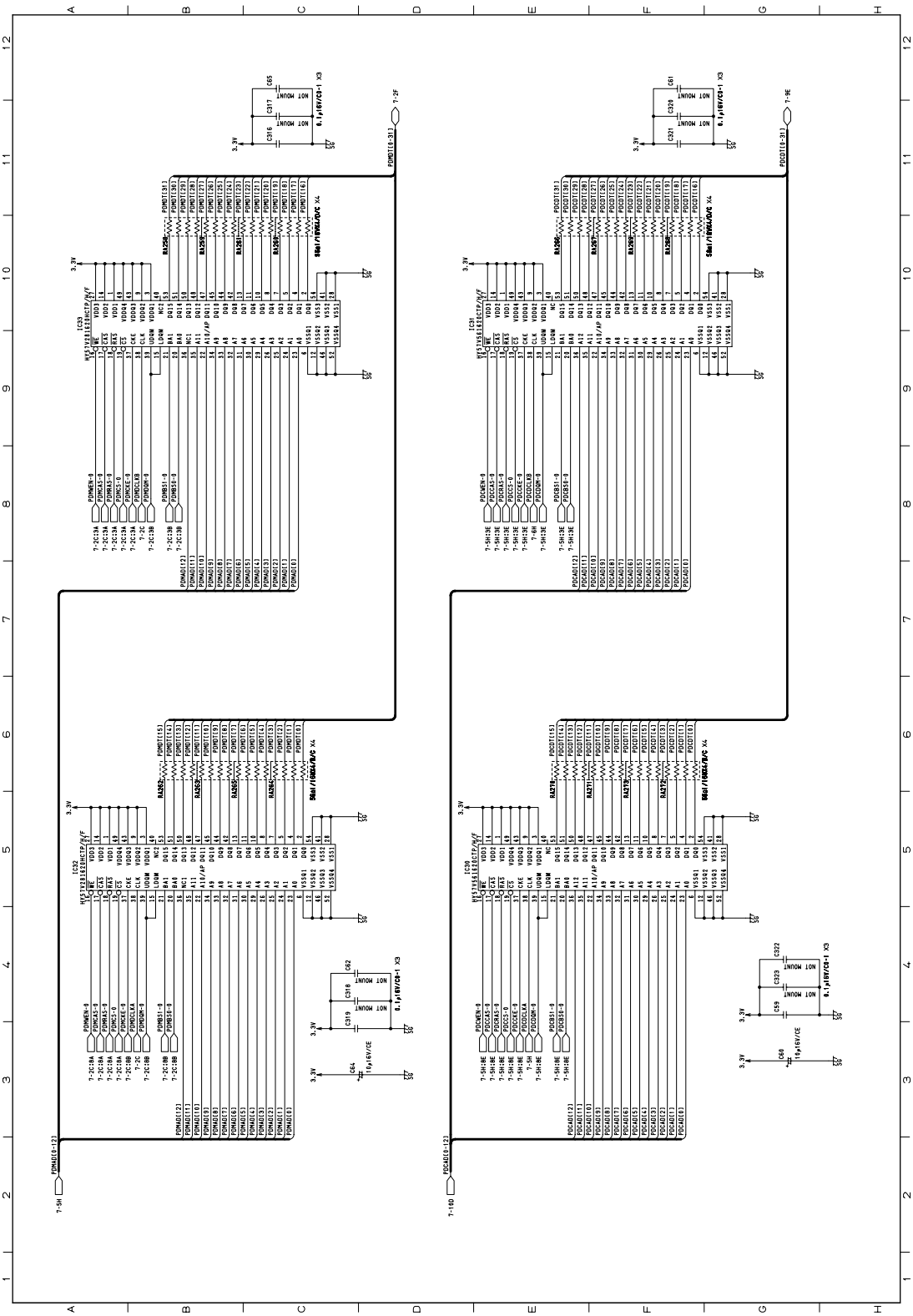

Fig. 3-77

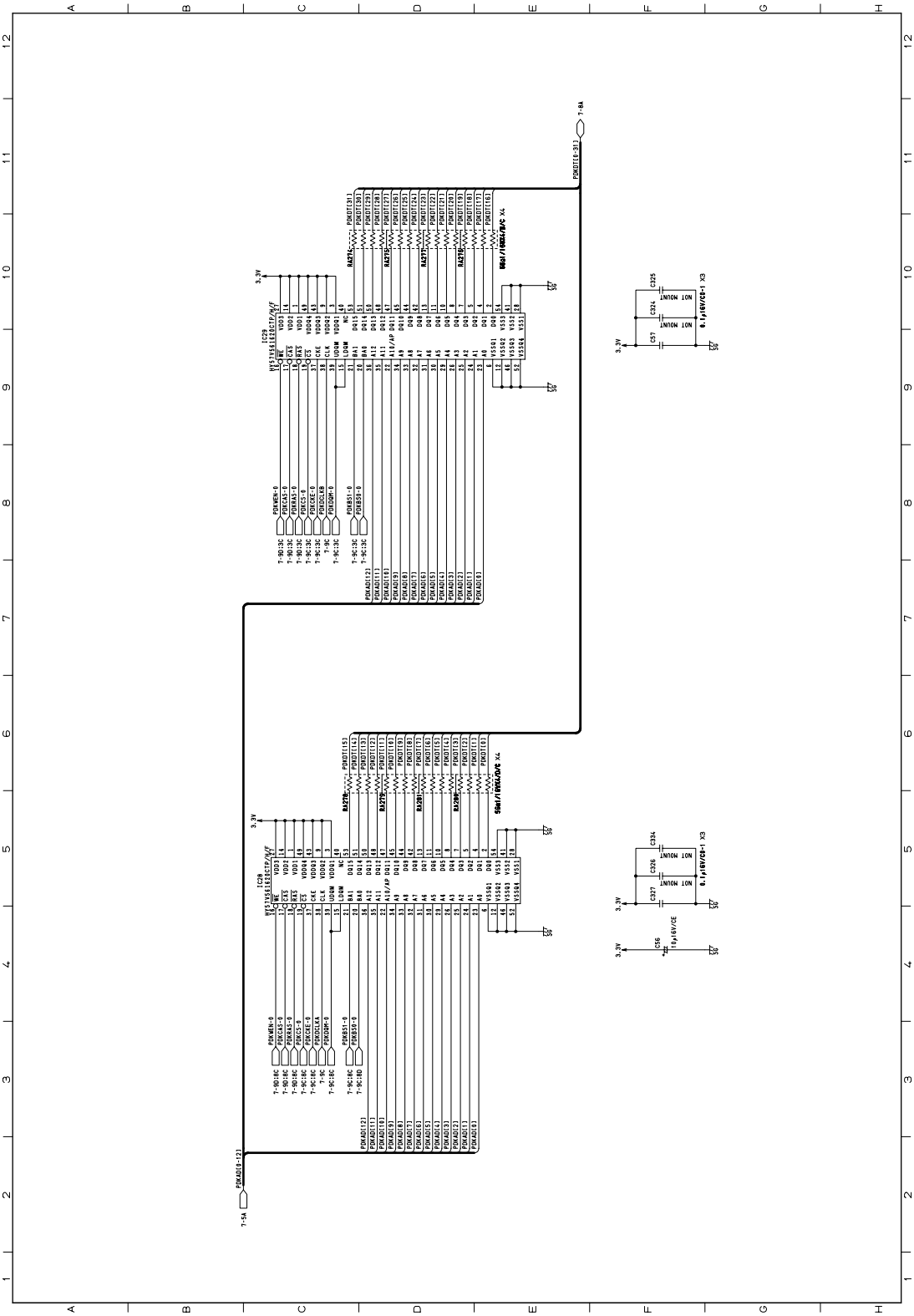

Fig. 3-78

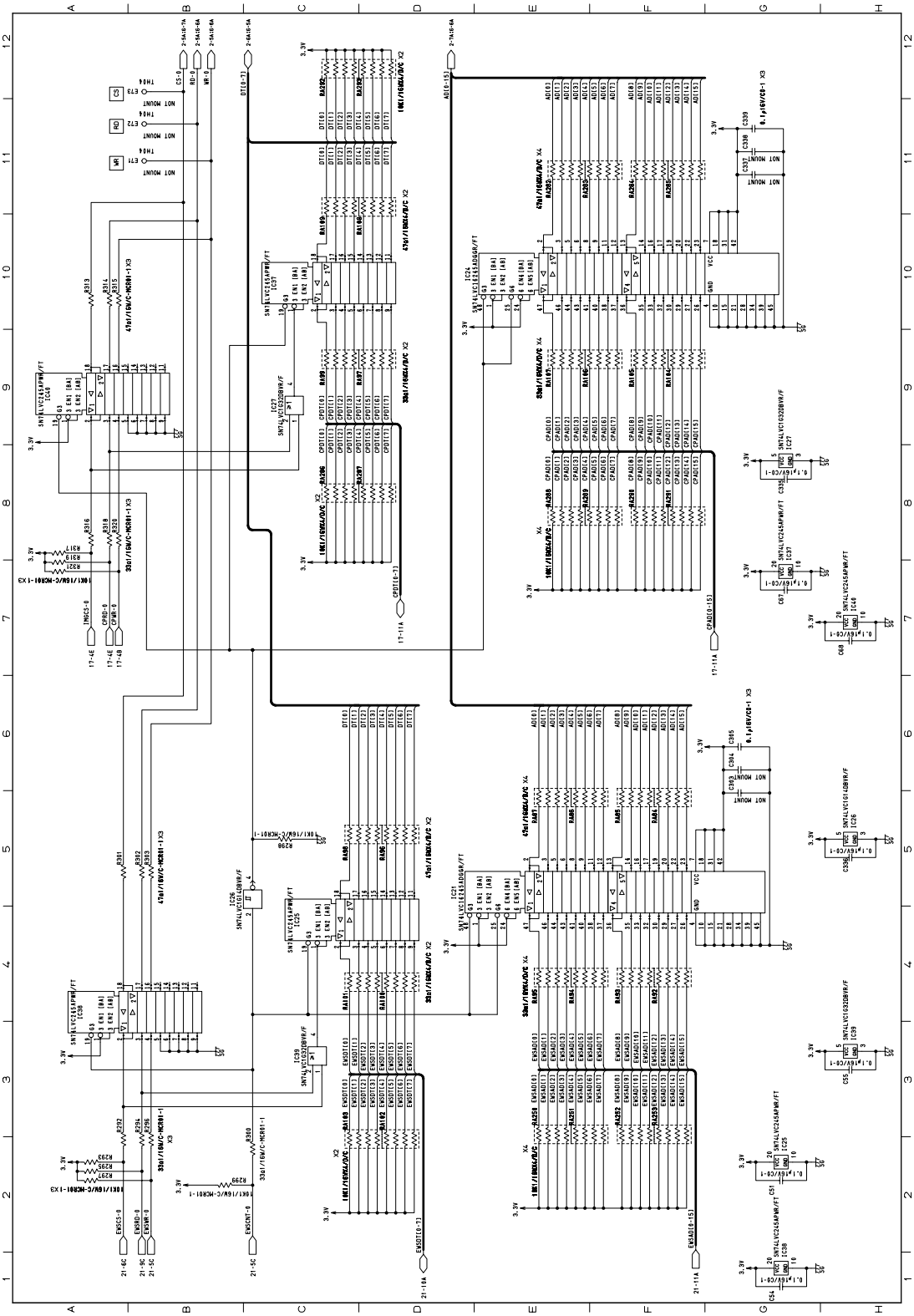

Fig. 3-79

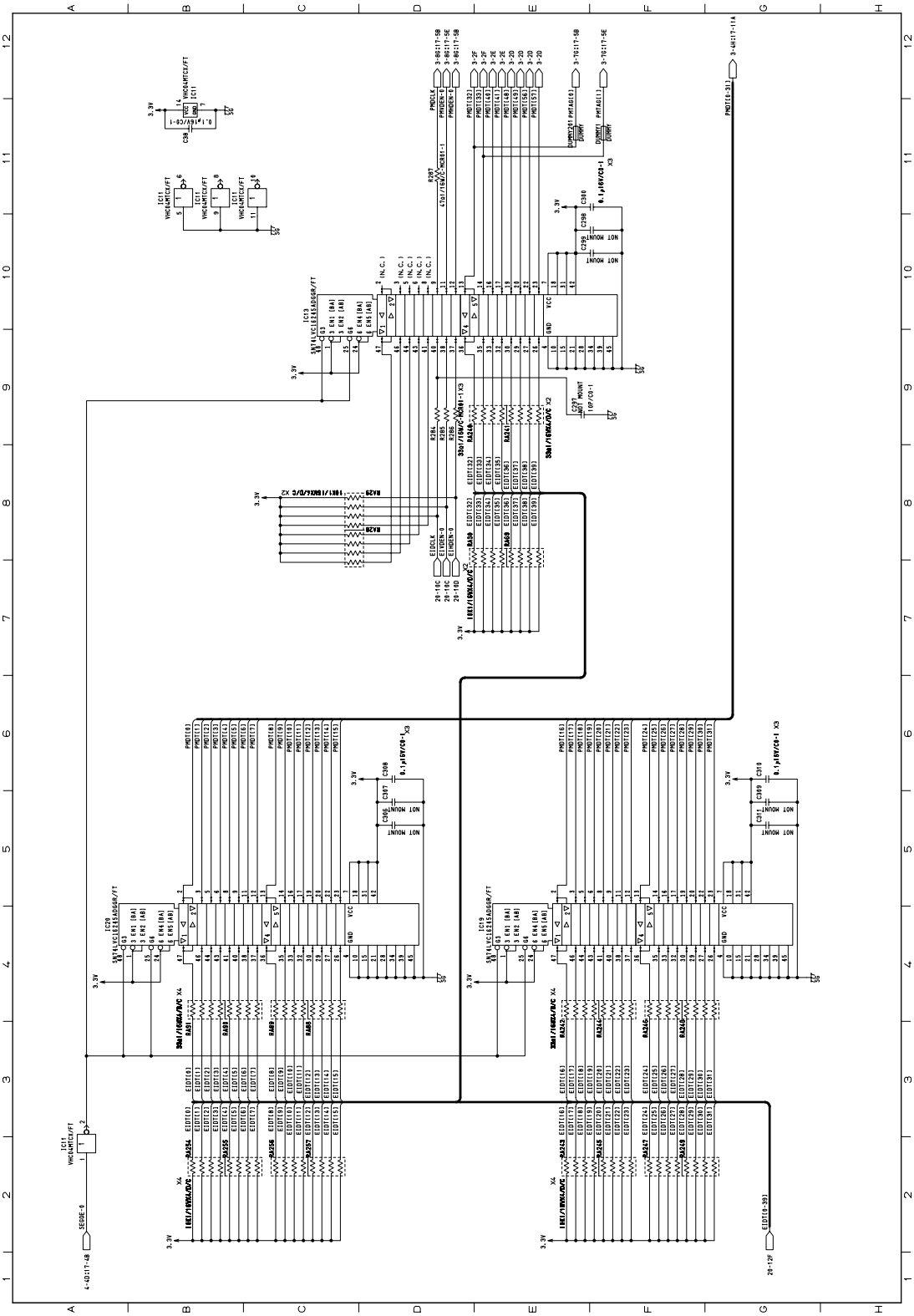

Fig. 3-80

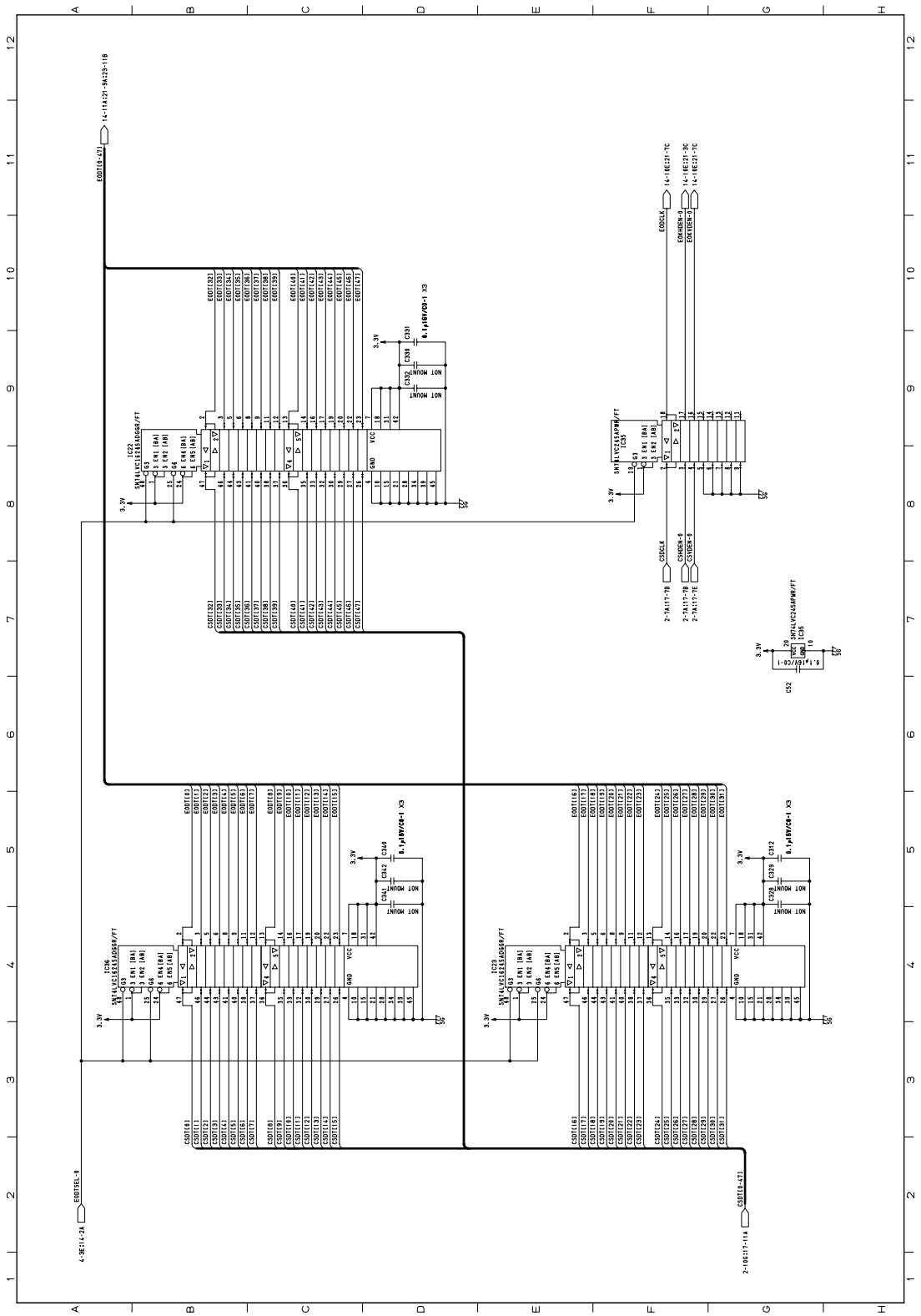

Fig. 3-81

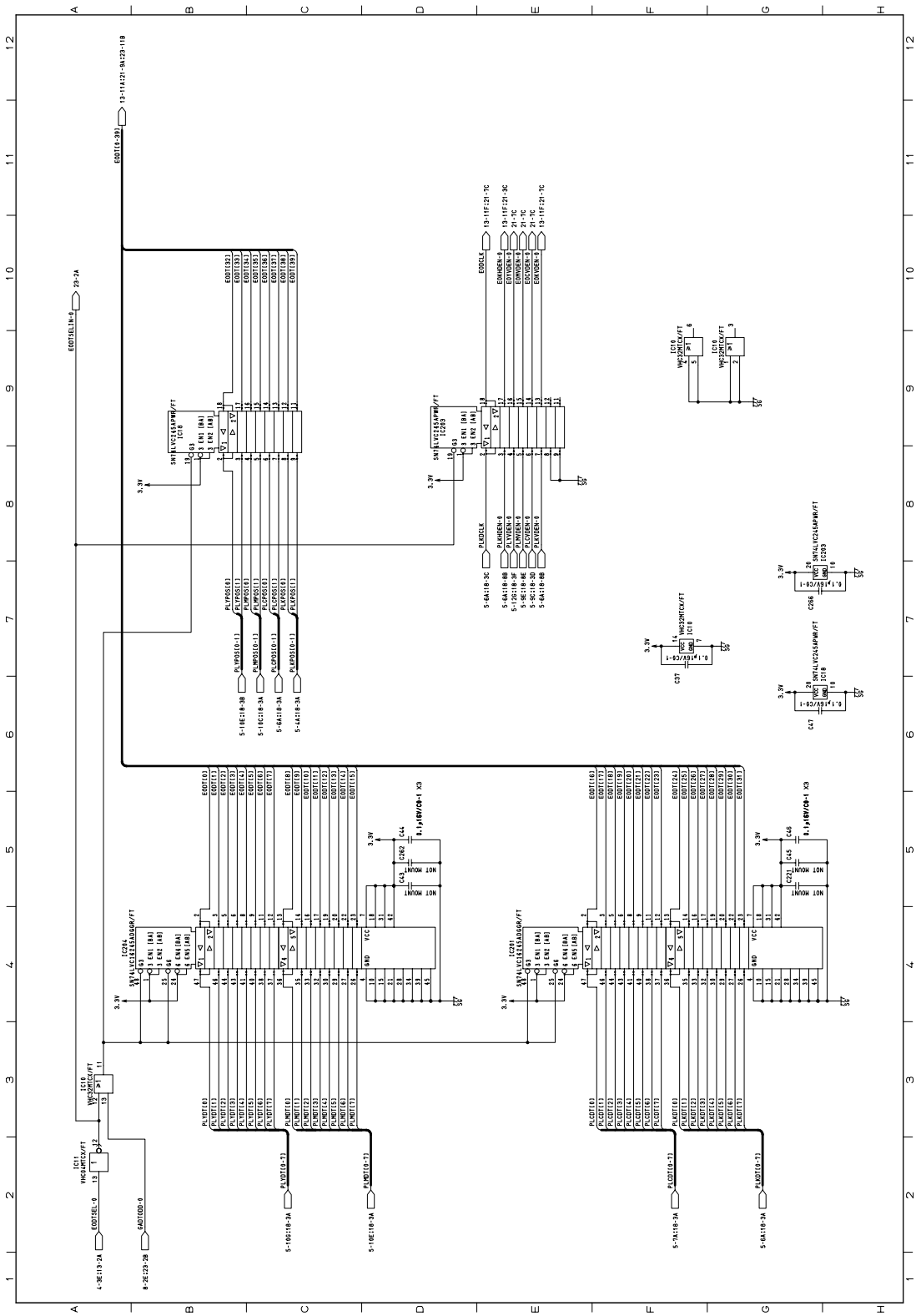

Fig. 3-82

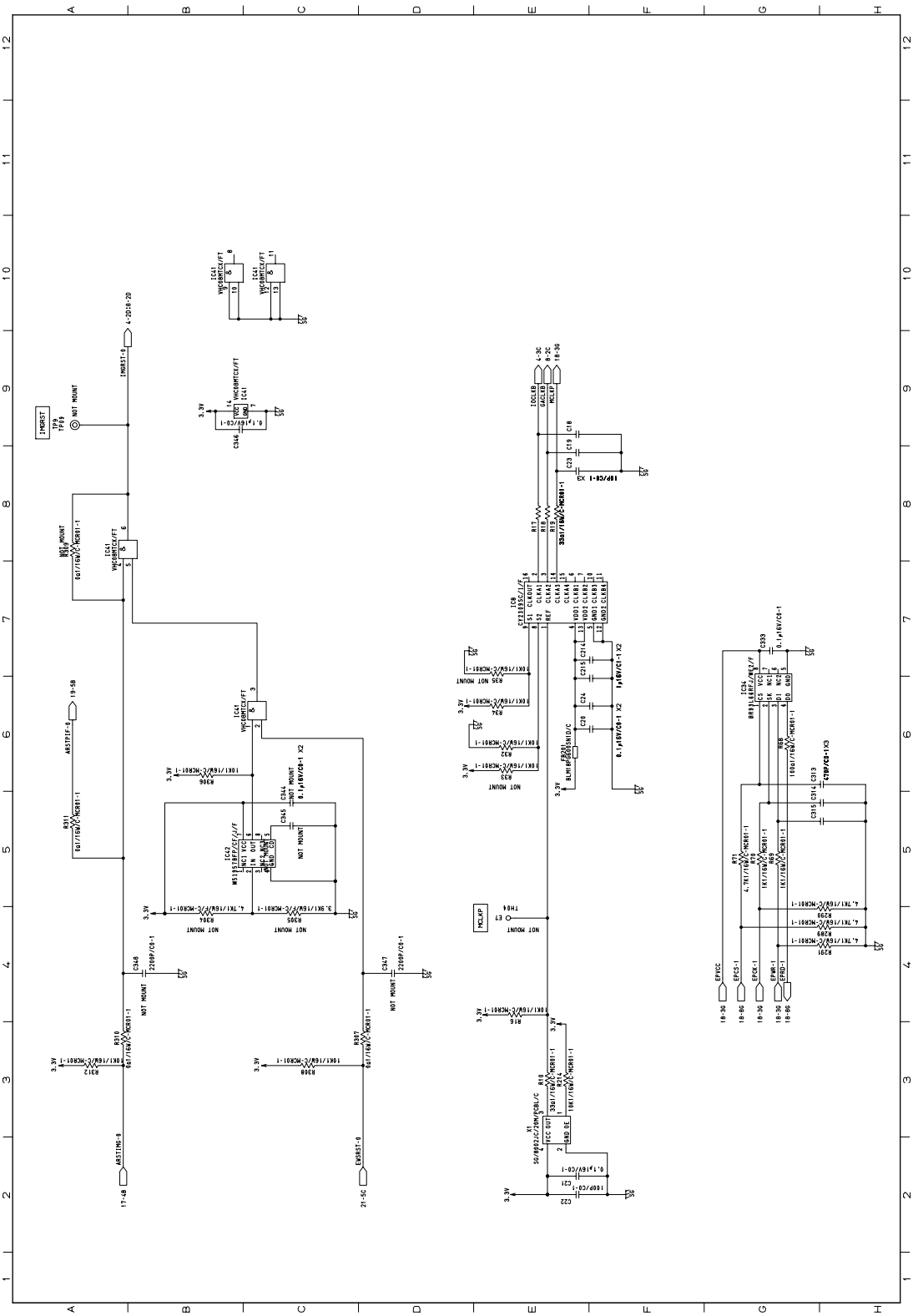

Fig. 3-83

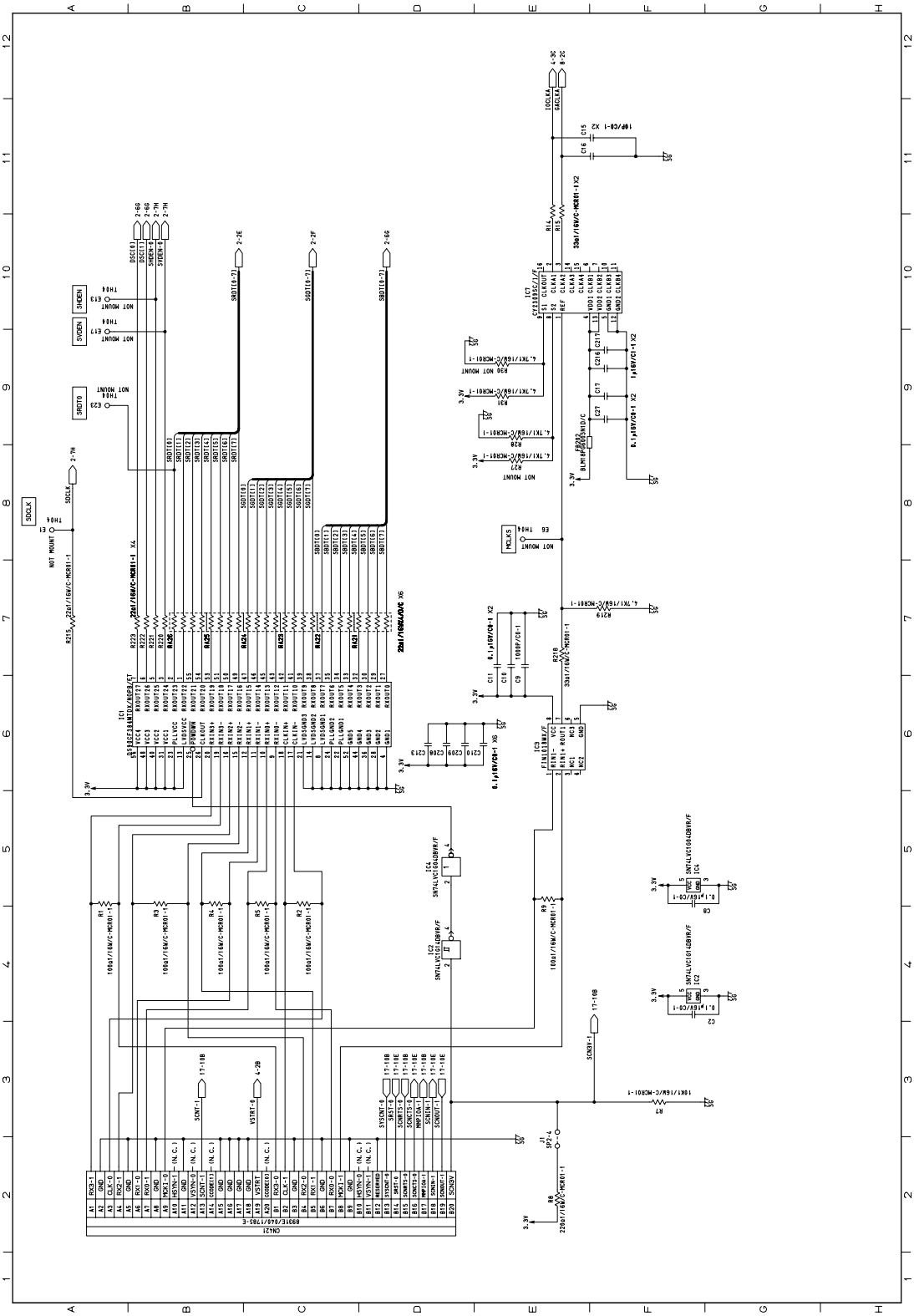

Fig. 3-84

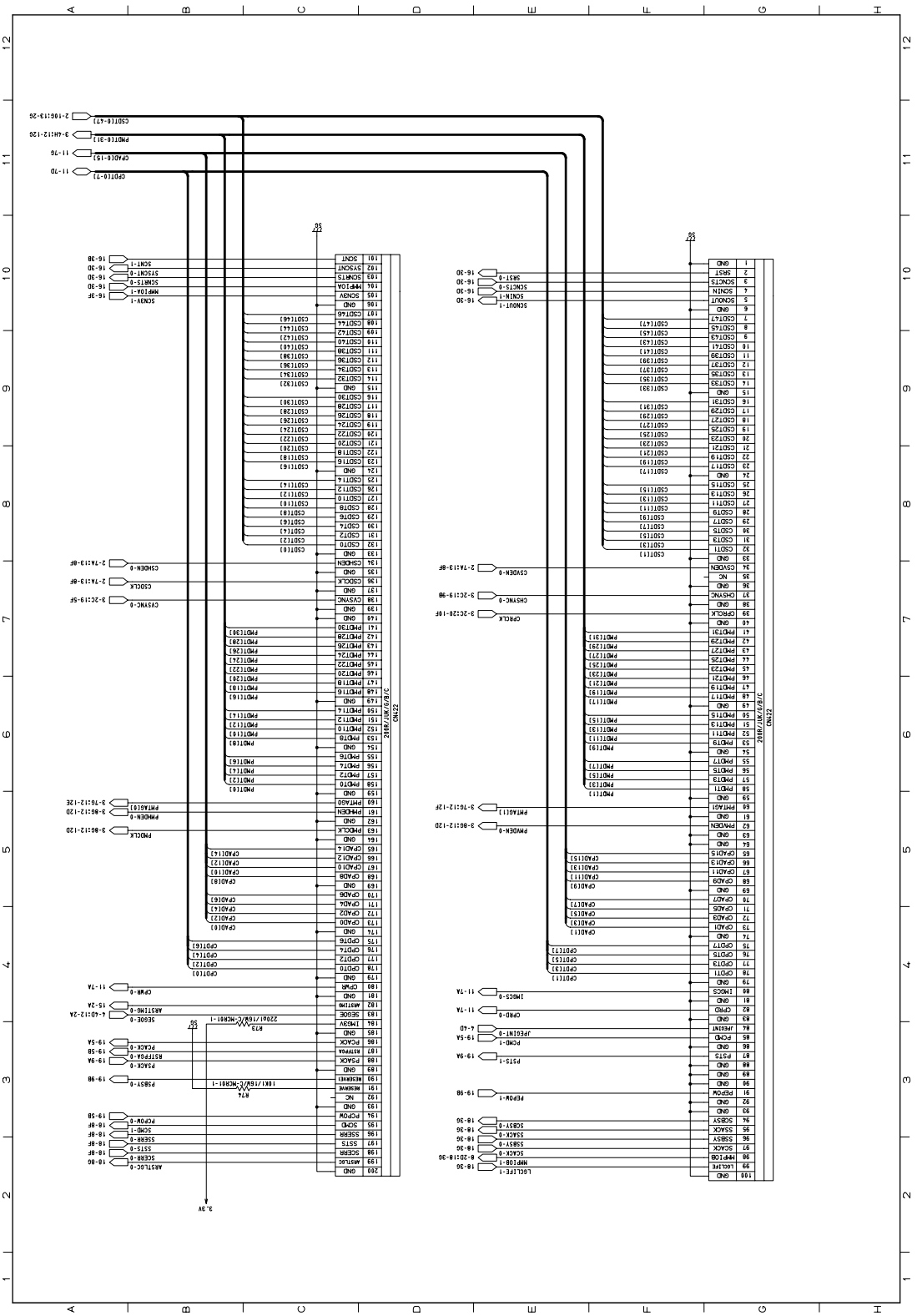

Fig. 3-85

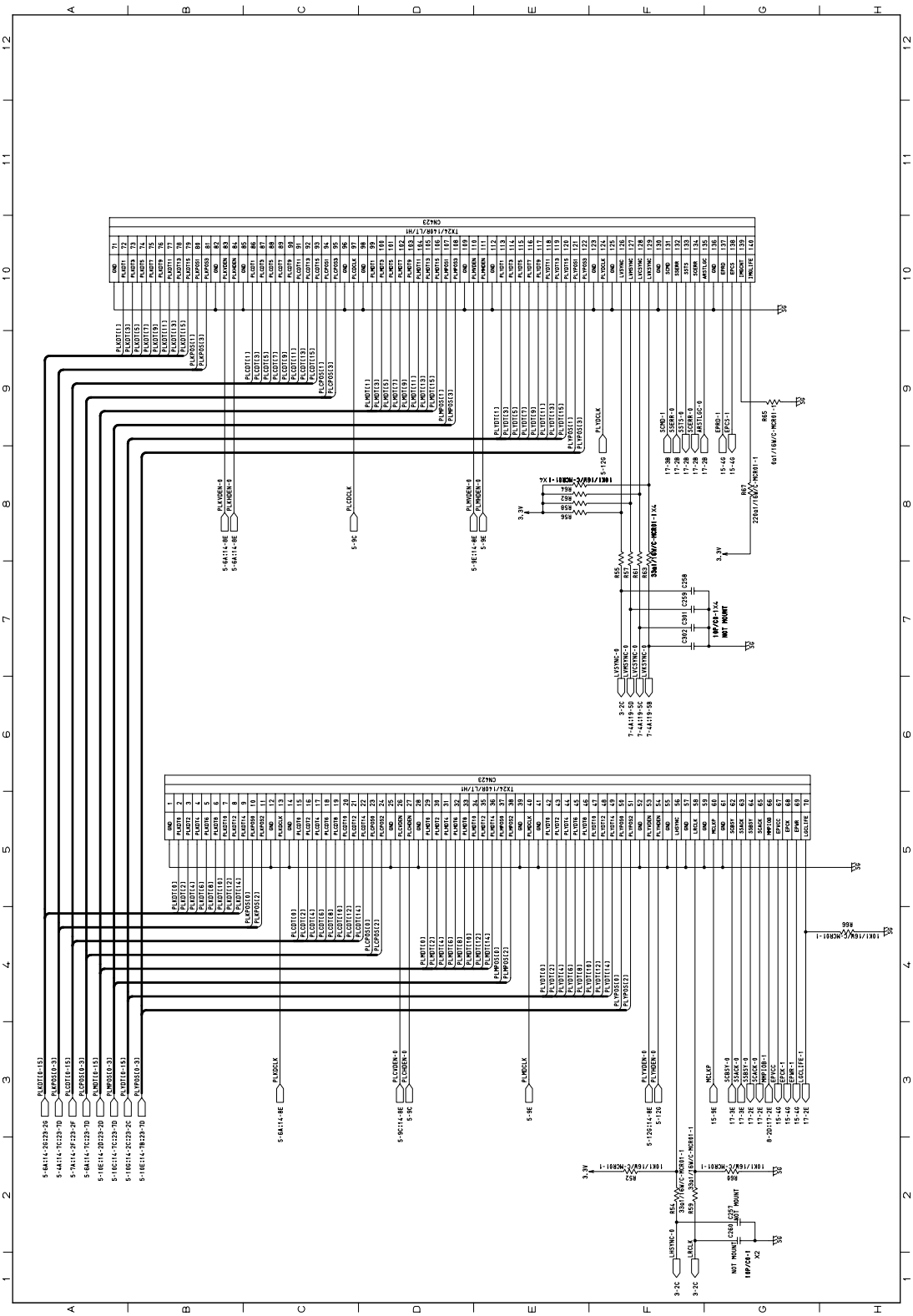

Fig. 3-86

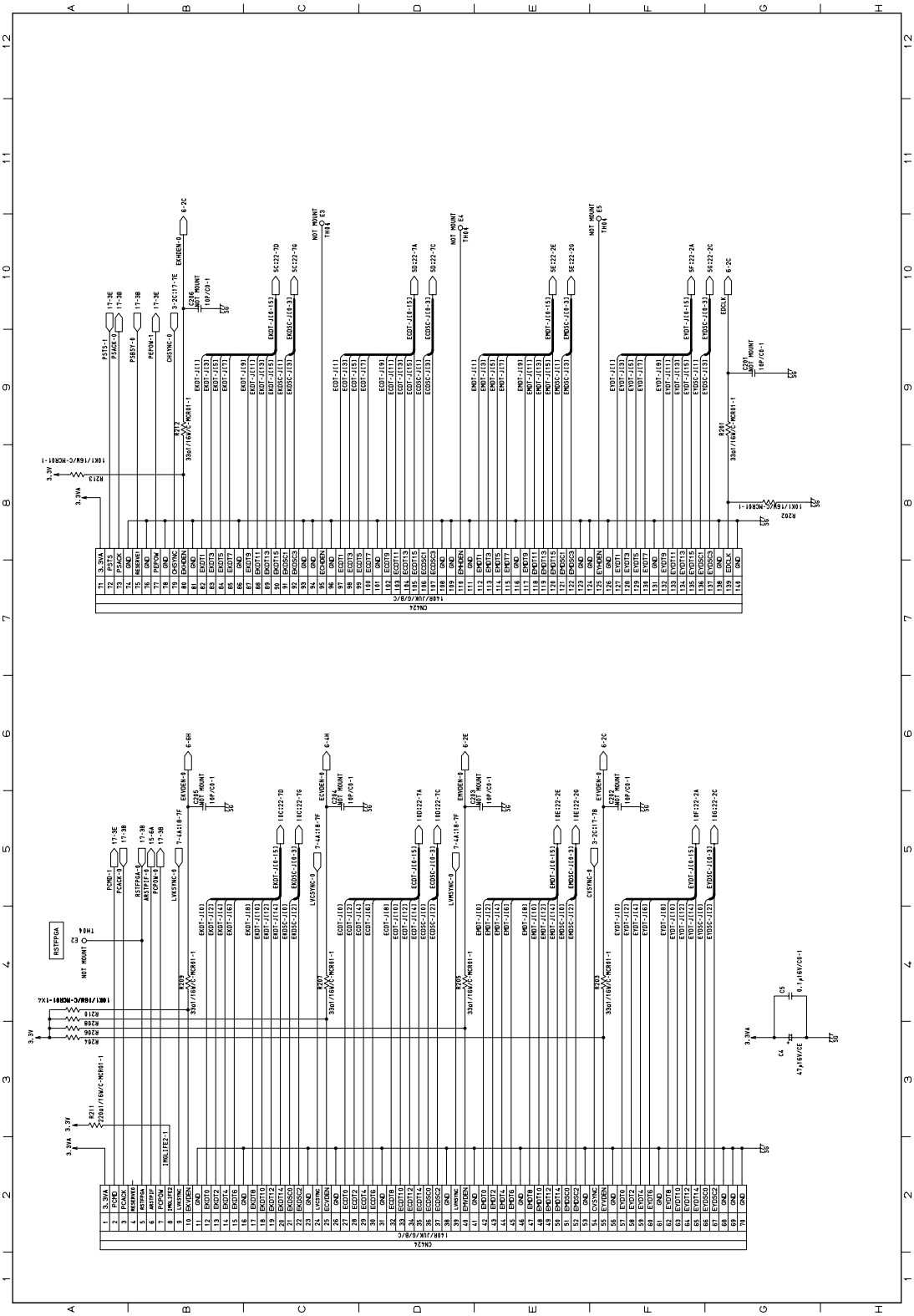

Fig. 3-87

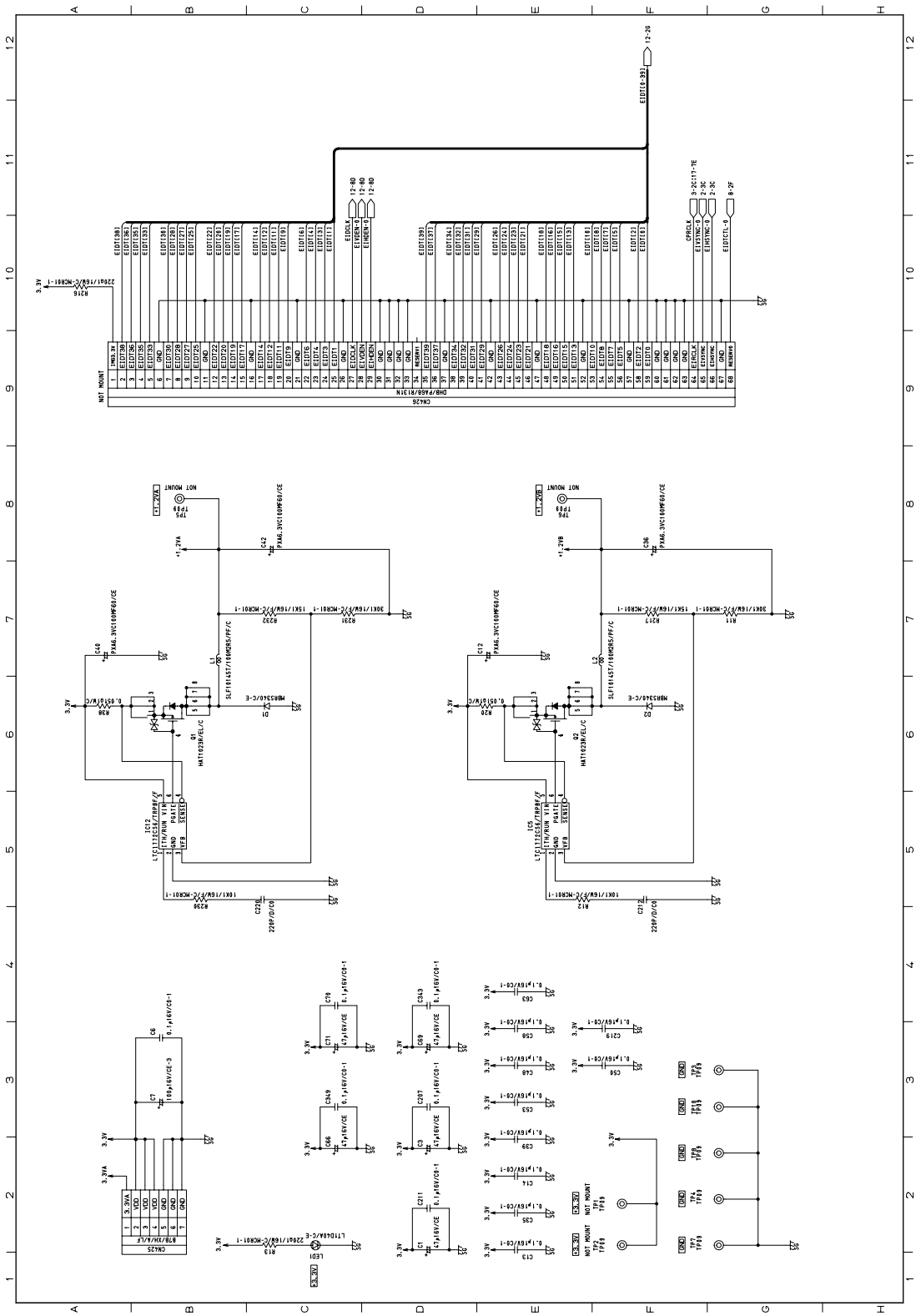

Fig. 3-88

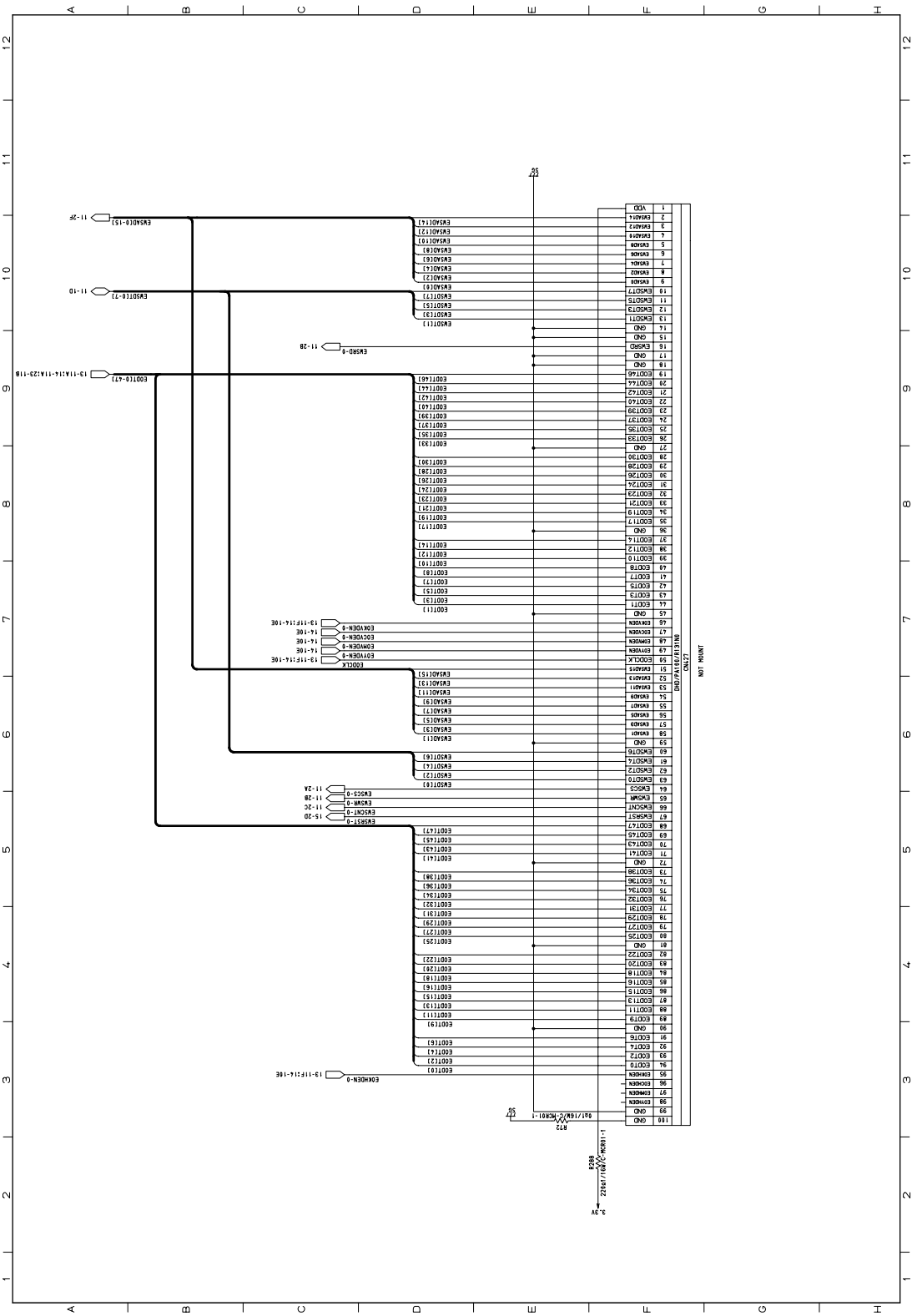

Fig. 3-89

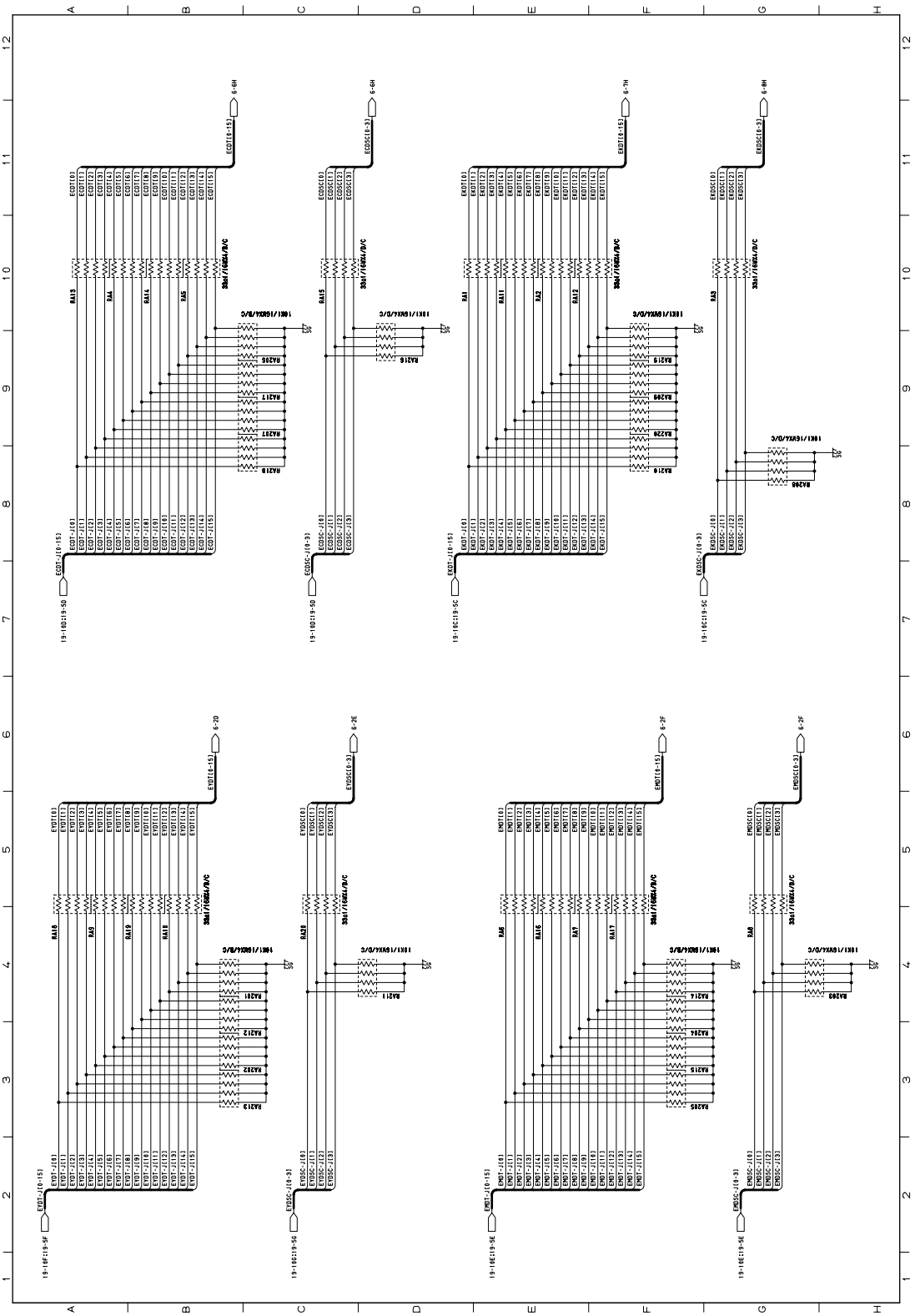

Fig. 3-90

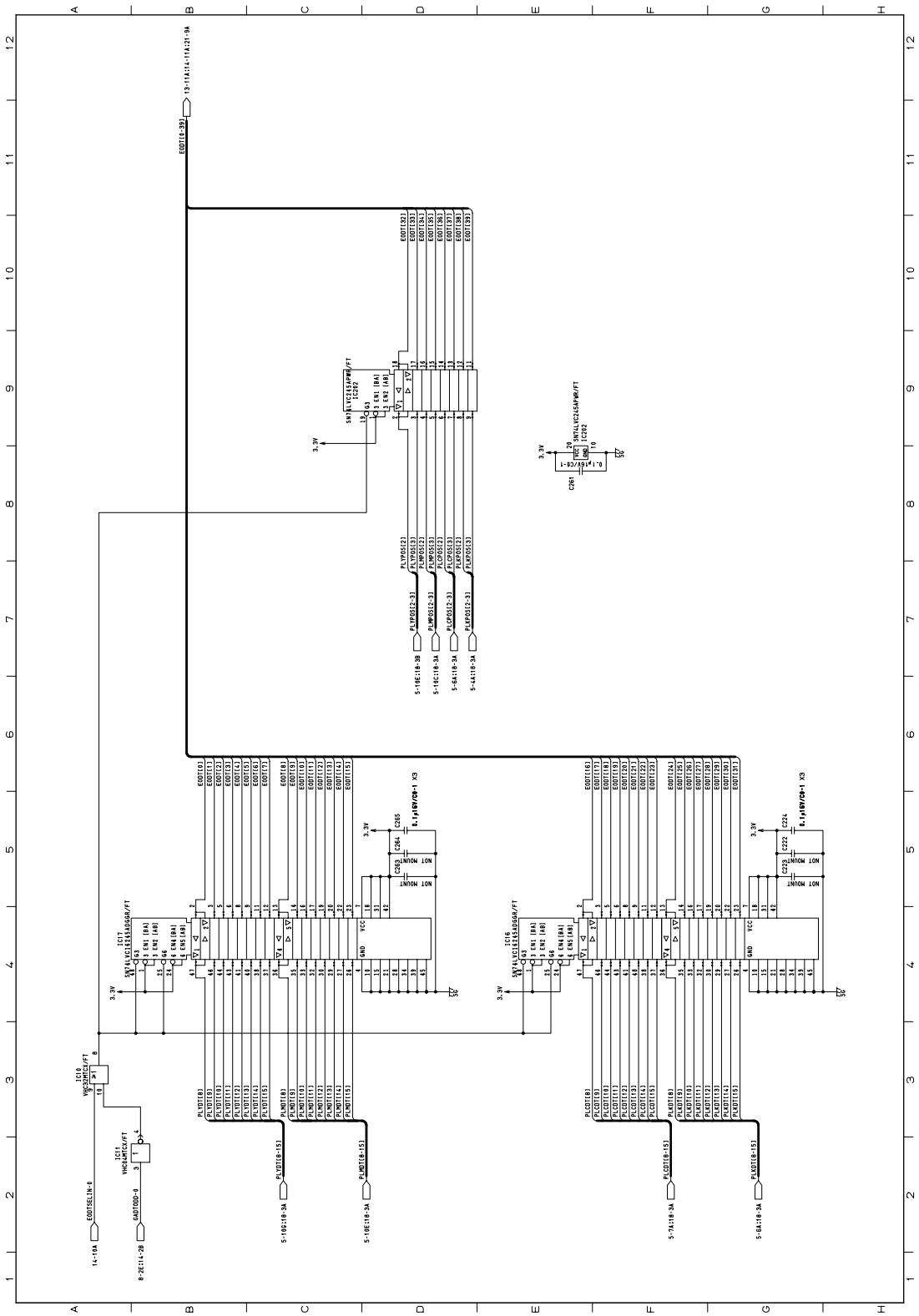

Fig. 3-91

3.5 Scanning section circuit (SLG board)

SLG board 1/18

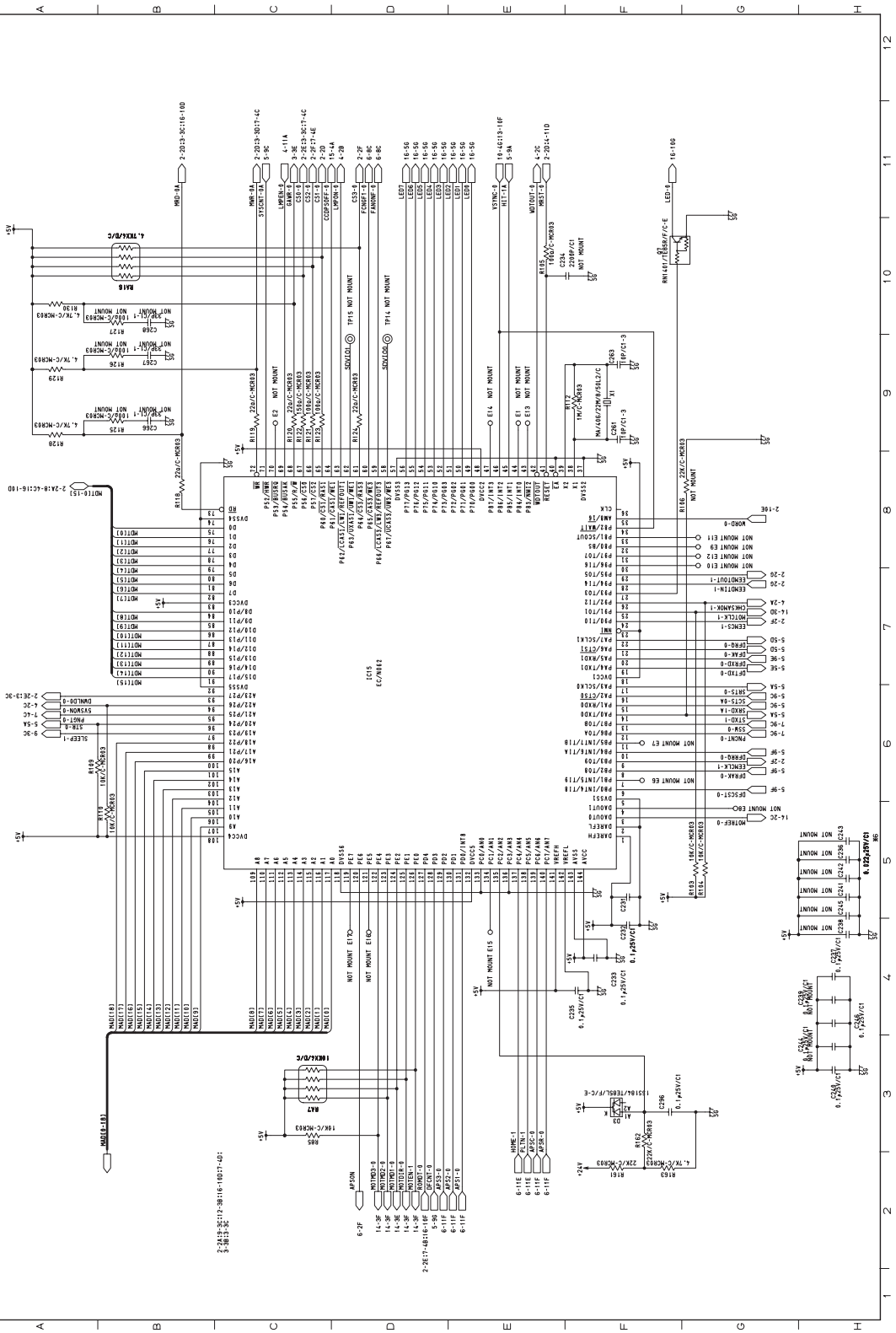

Fig. 3-92

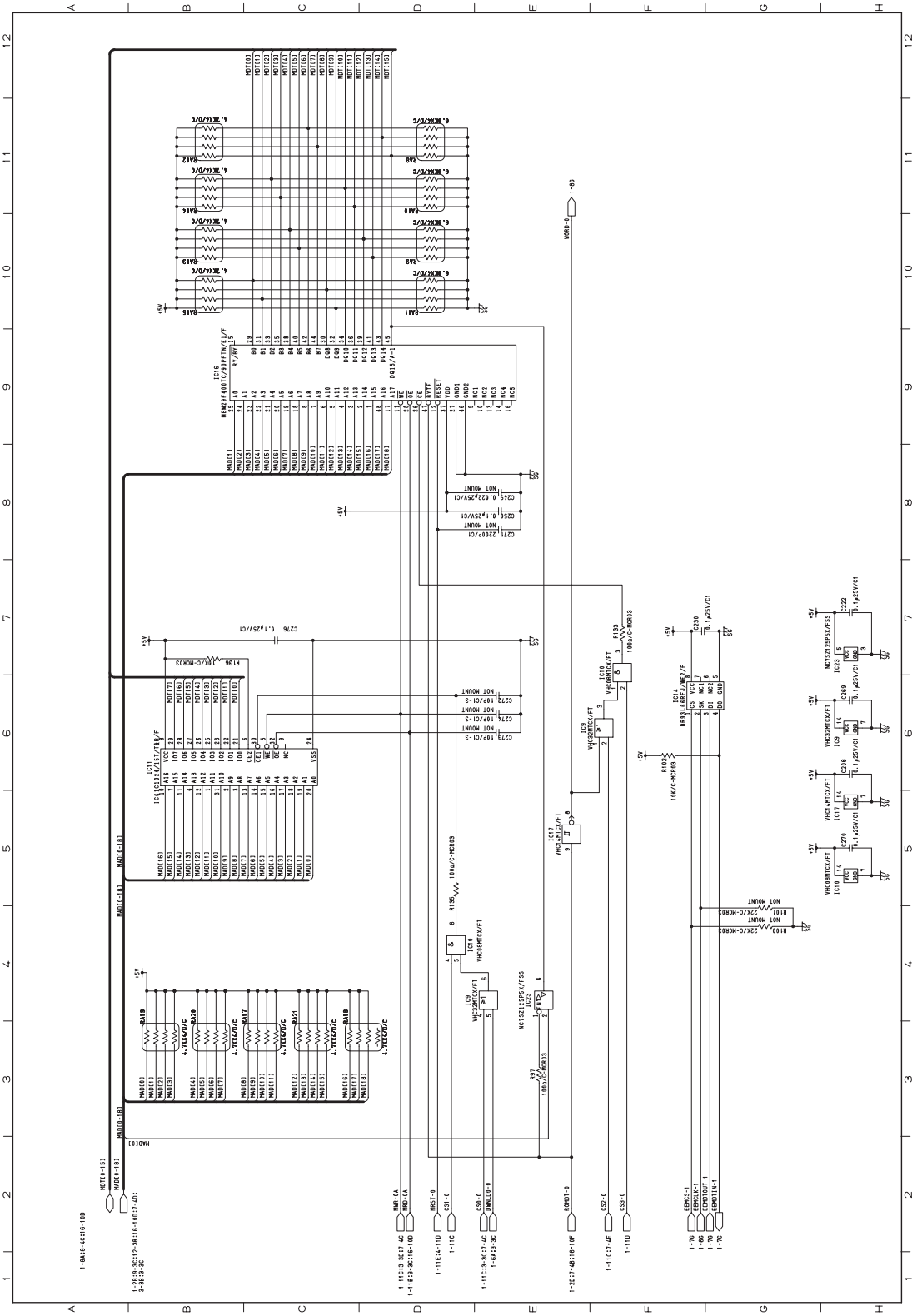

Fig. 3-93

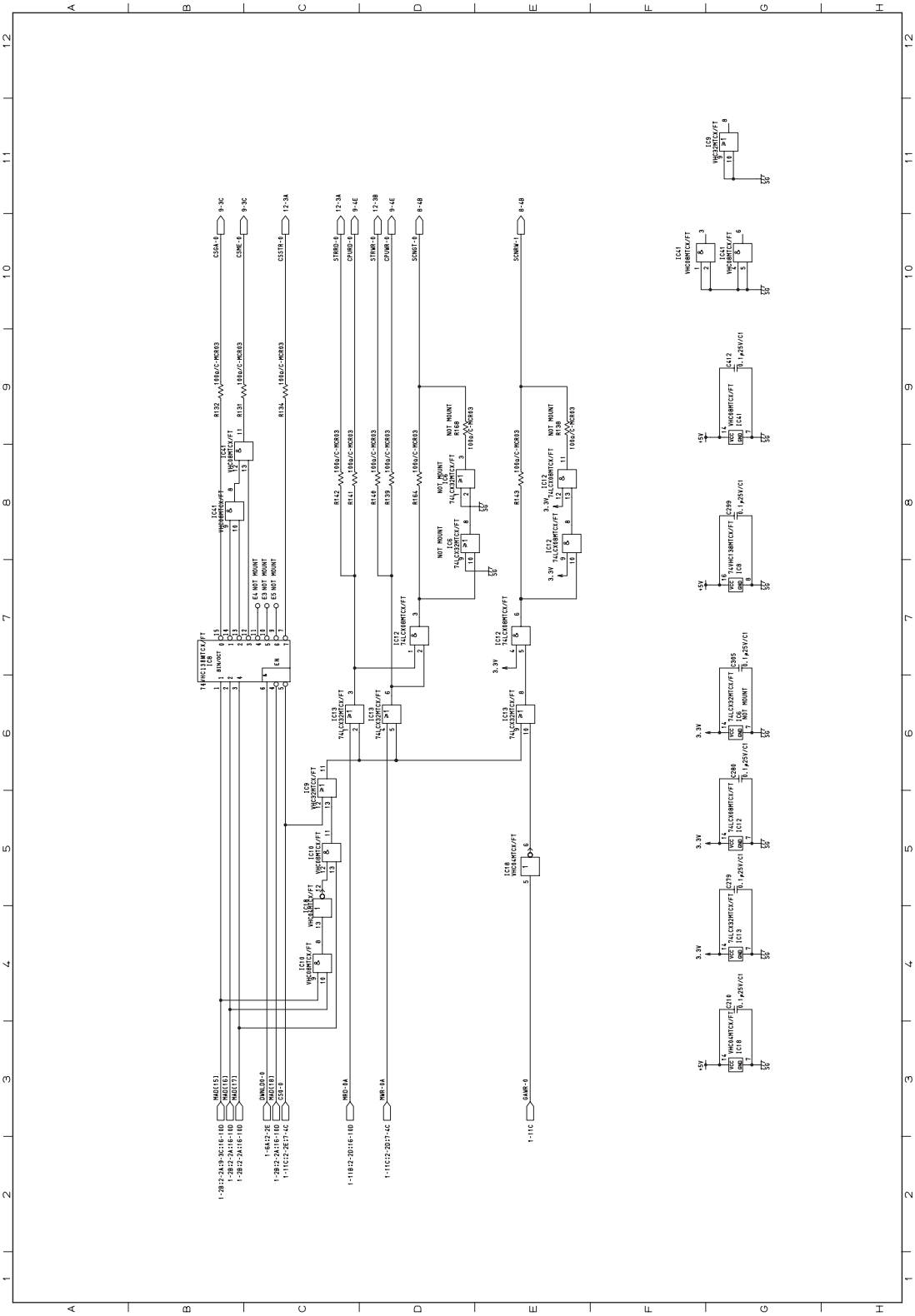

Fig. 3-94

SLG board 4/18

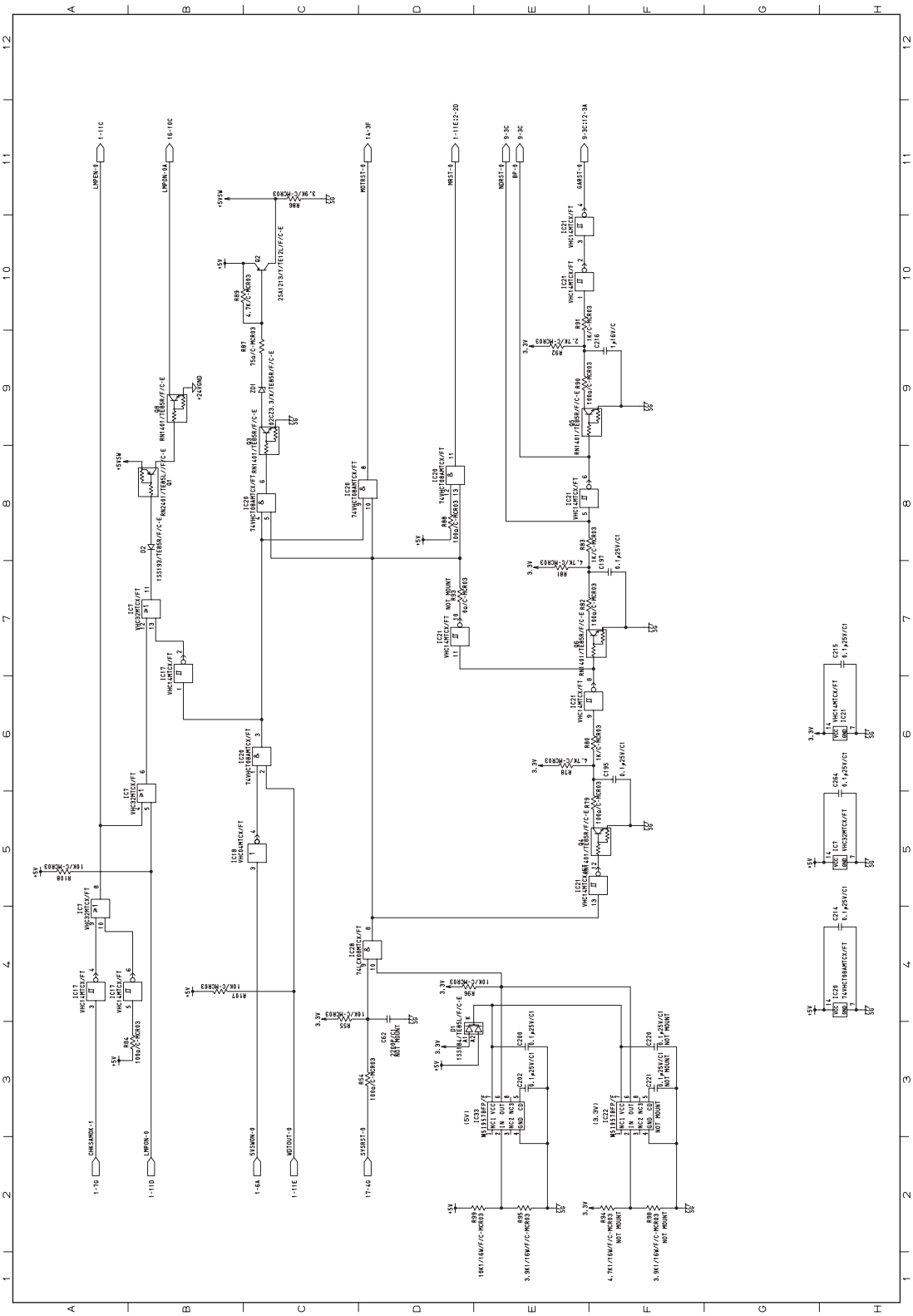

Fig. 3-95

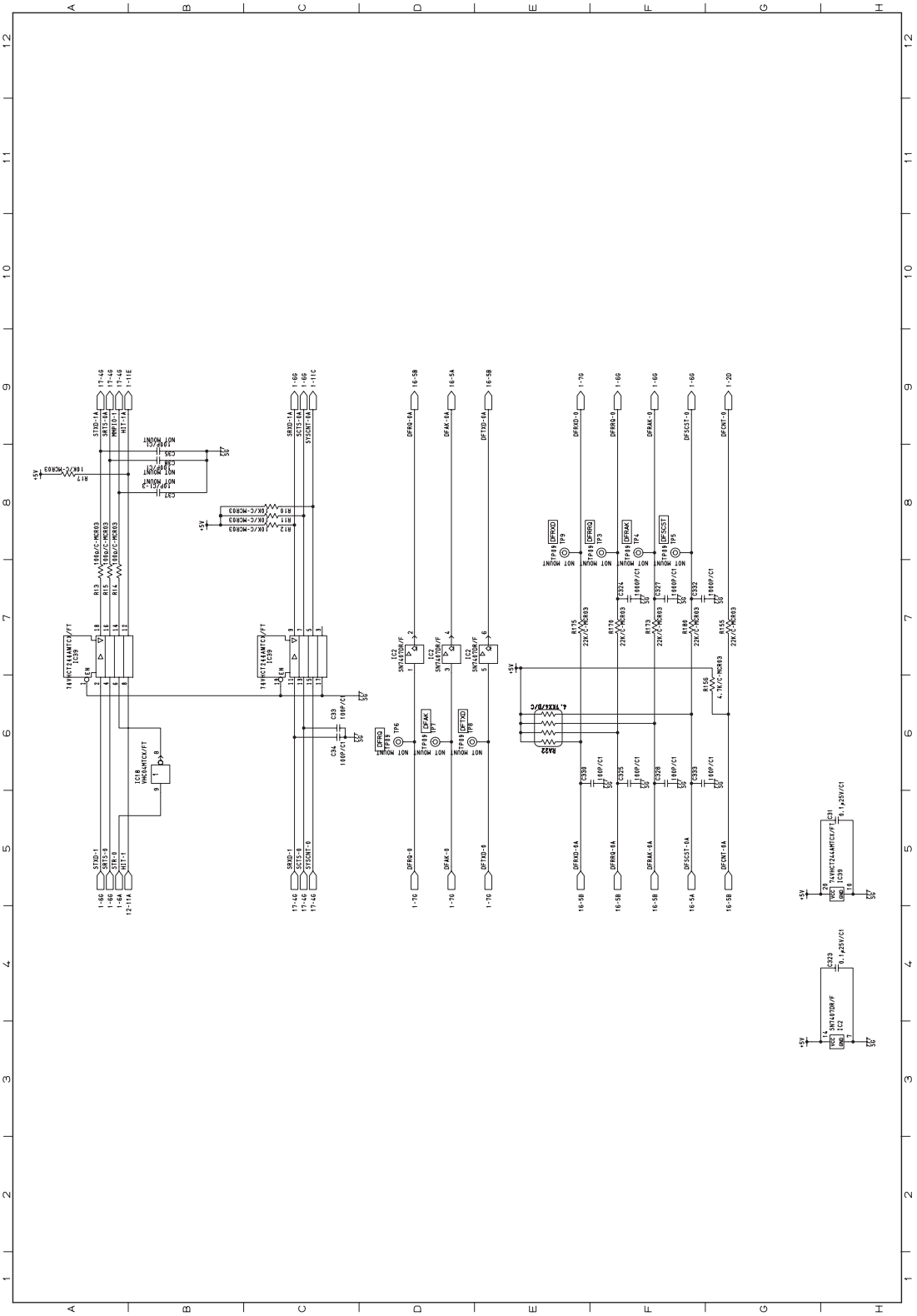

Fig. 3-96

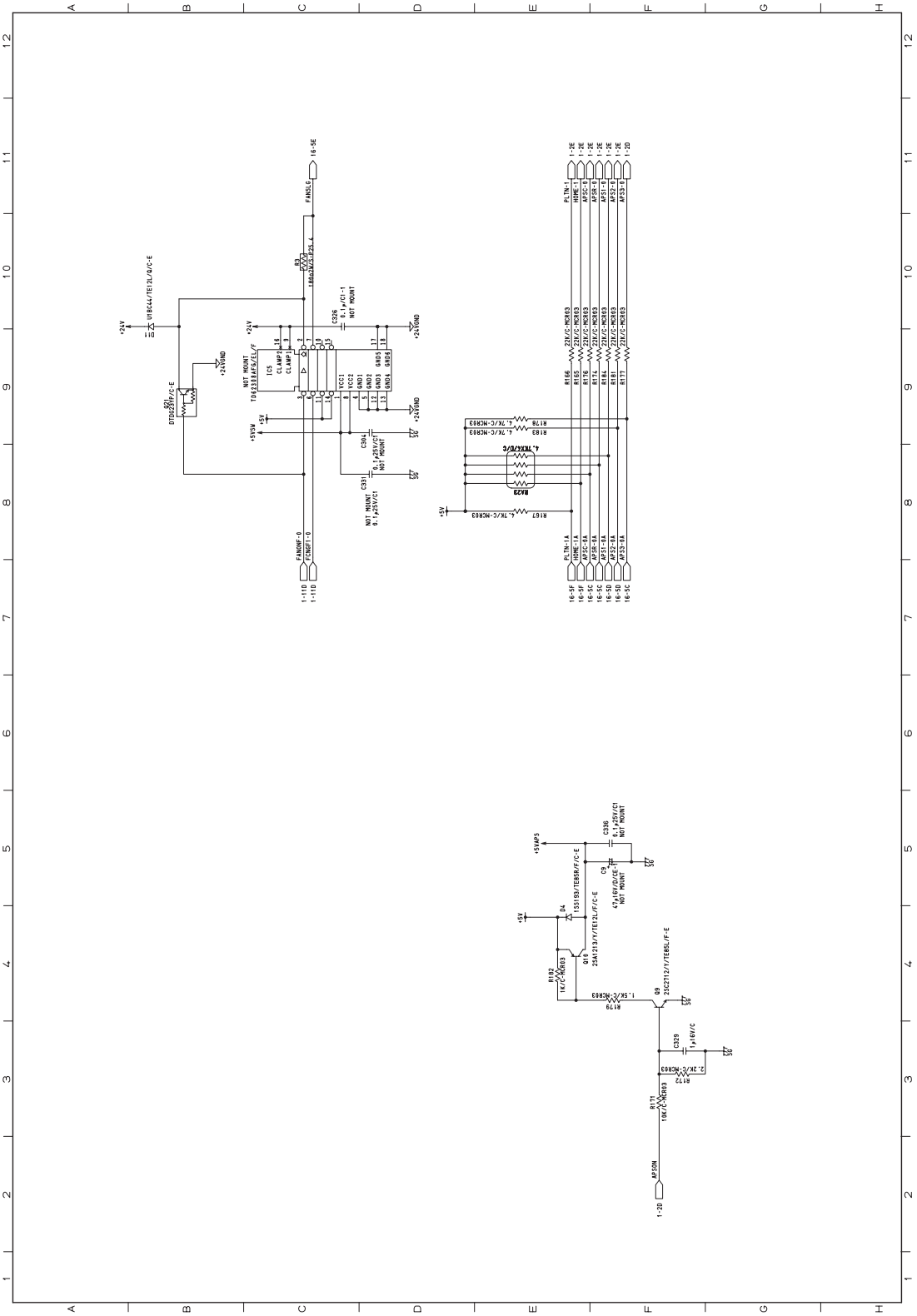

Fig. 3-97

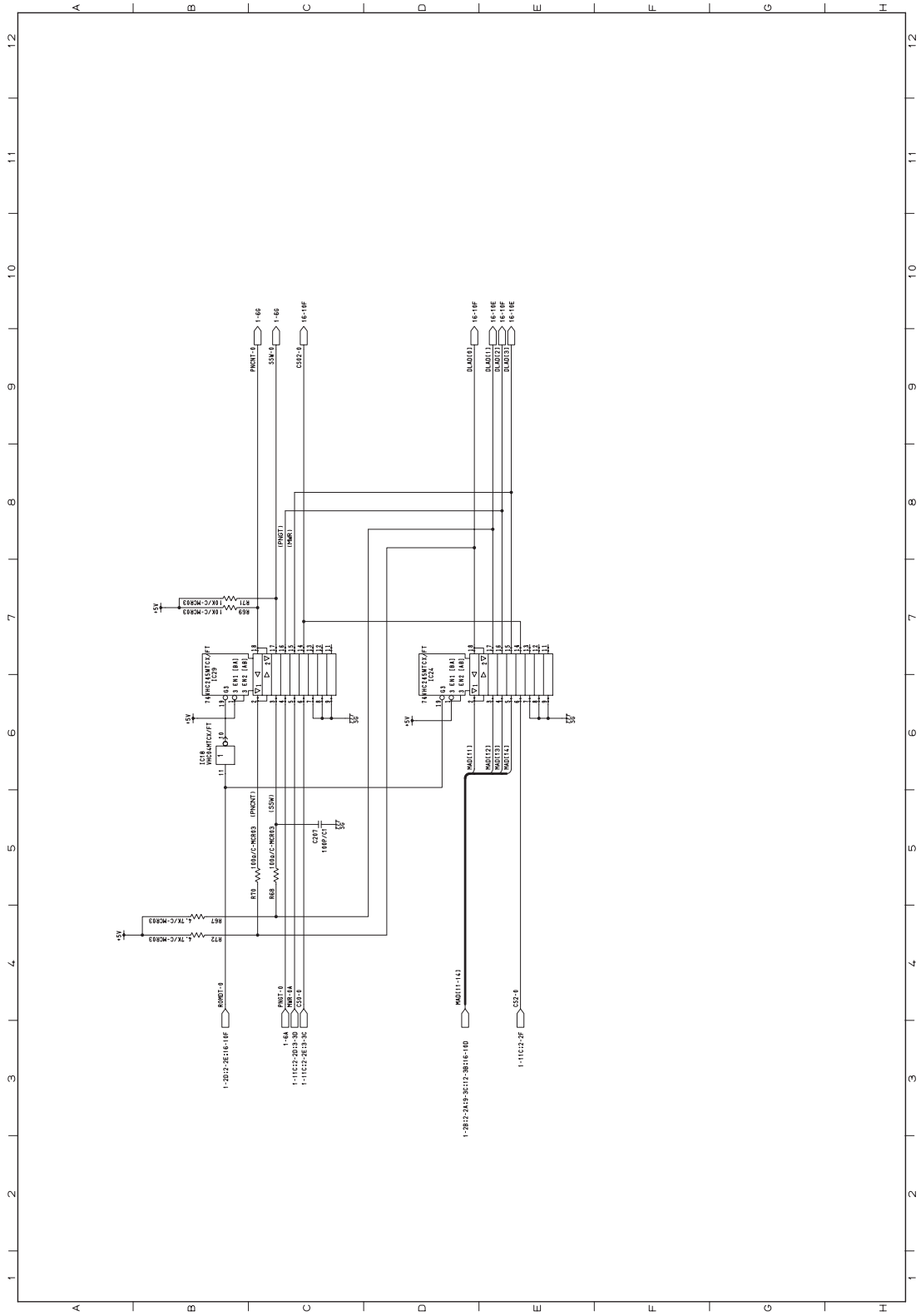

Fig. 3-98

SLG board 8/18

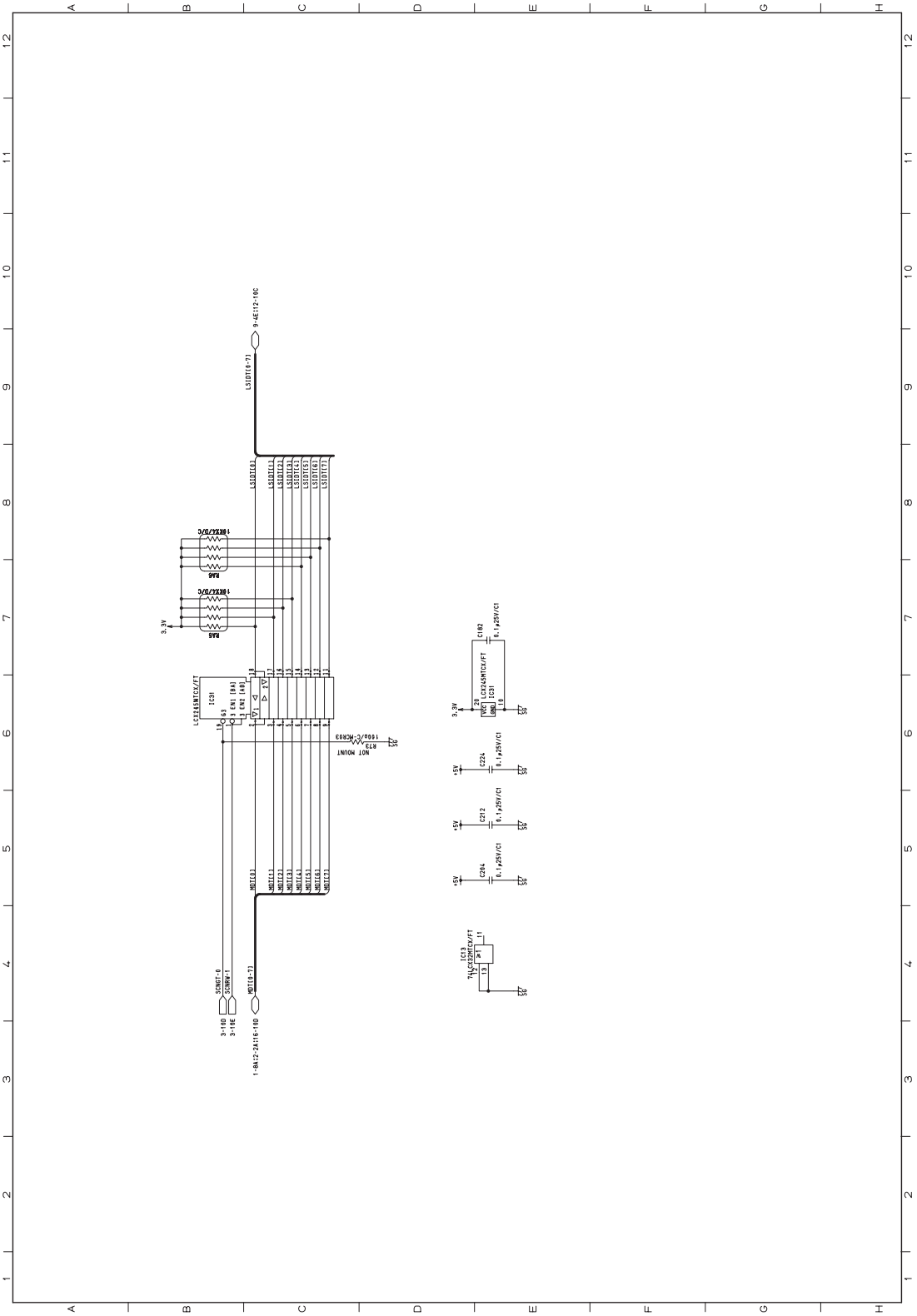

Fig. 3-99

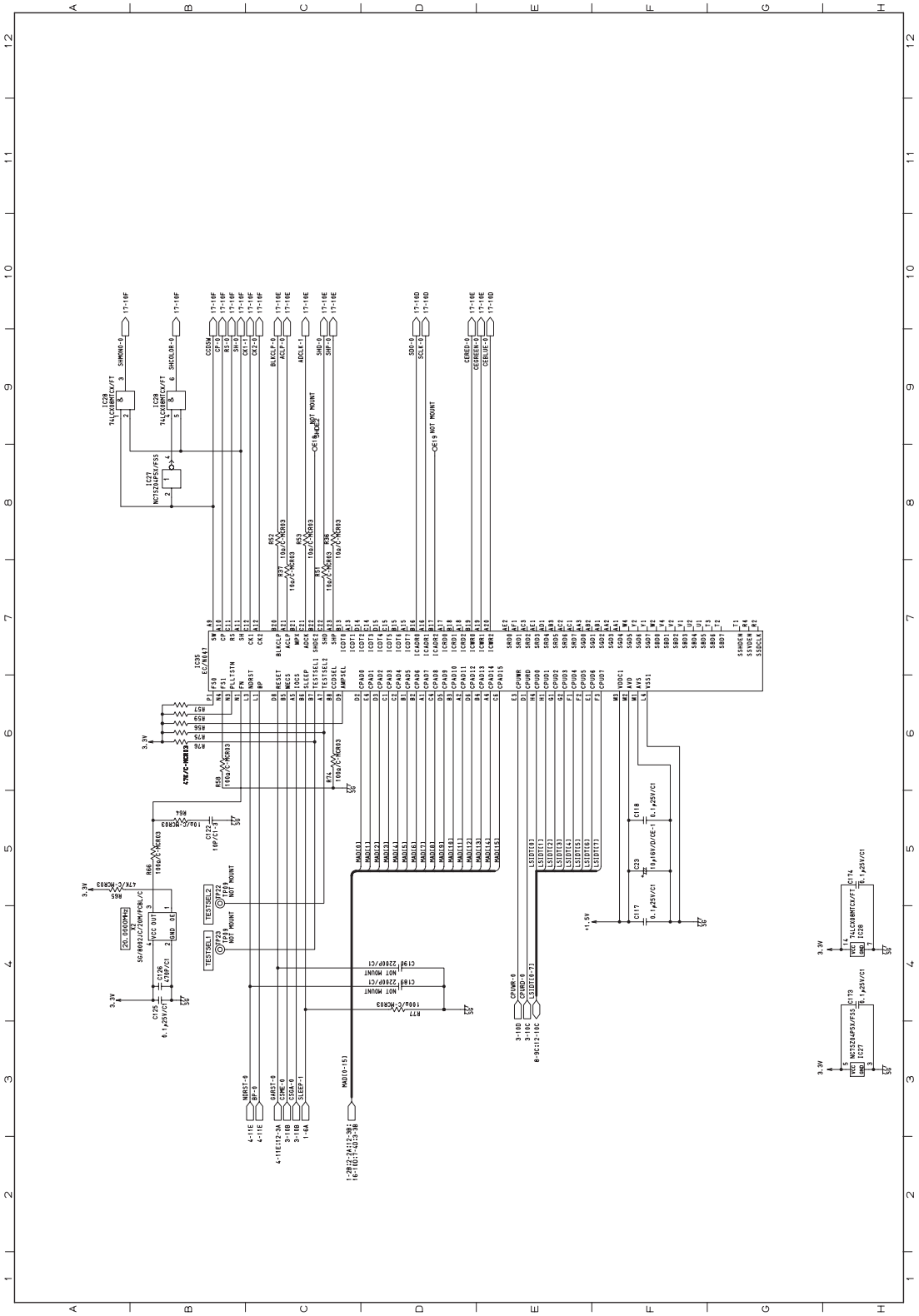

Fig. 3-100

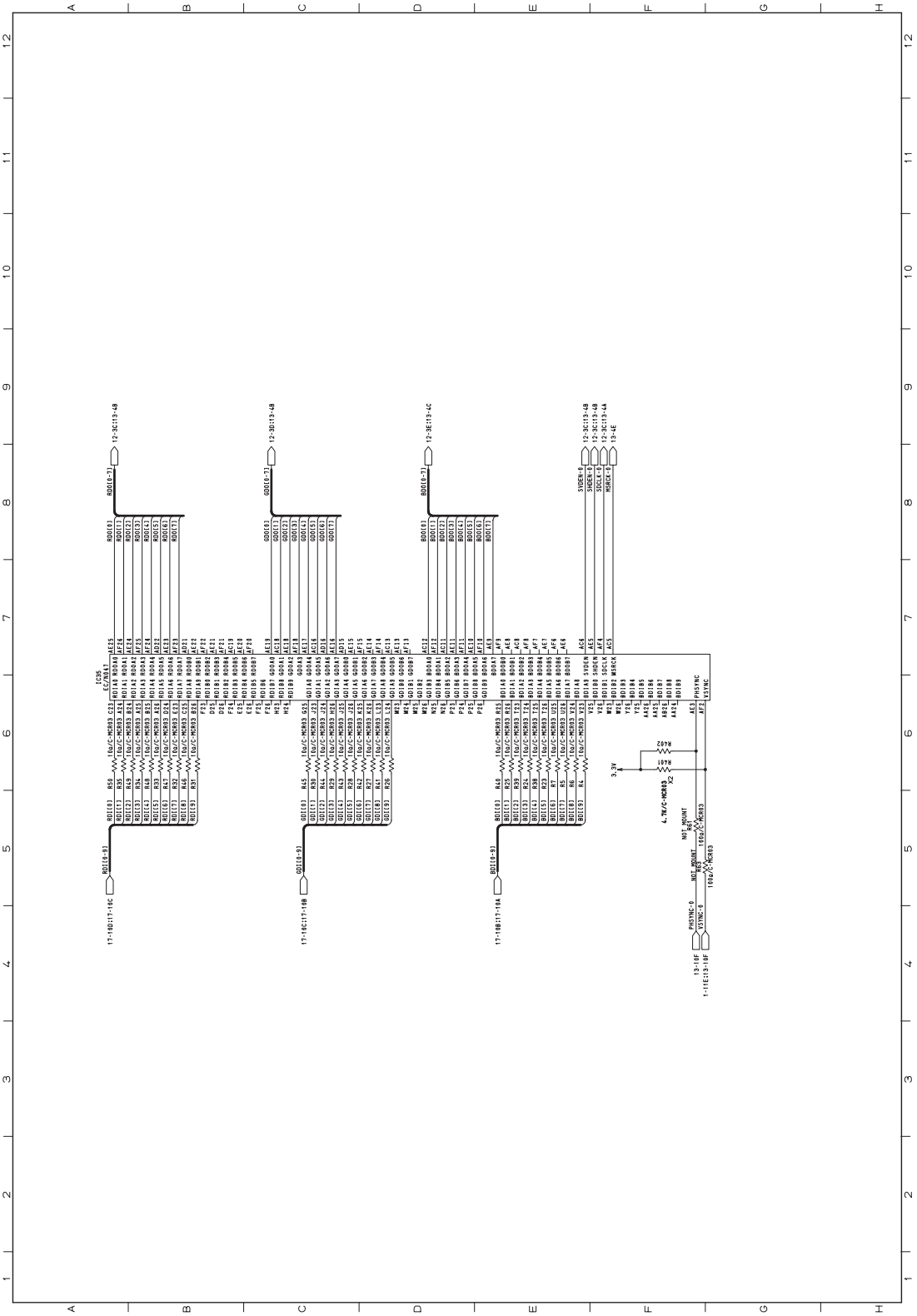

Fig. 3-101

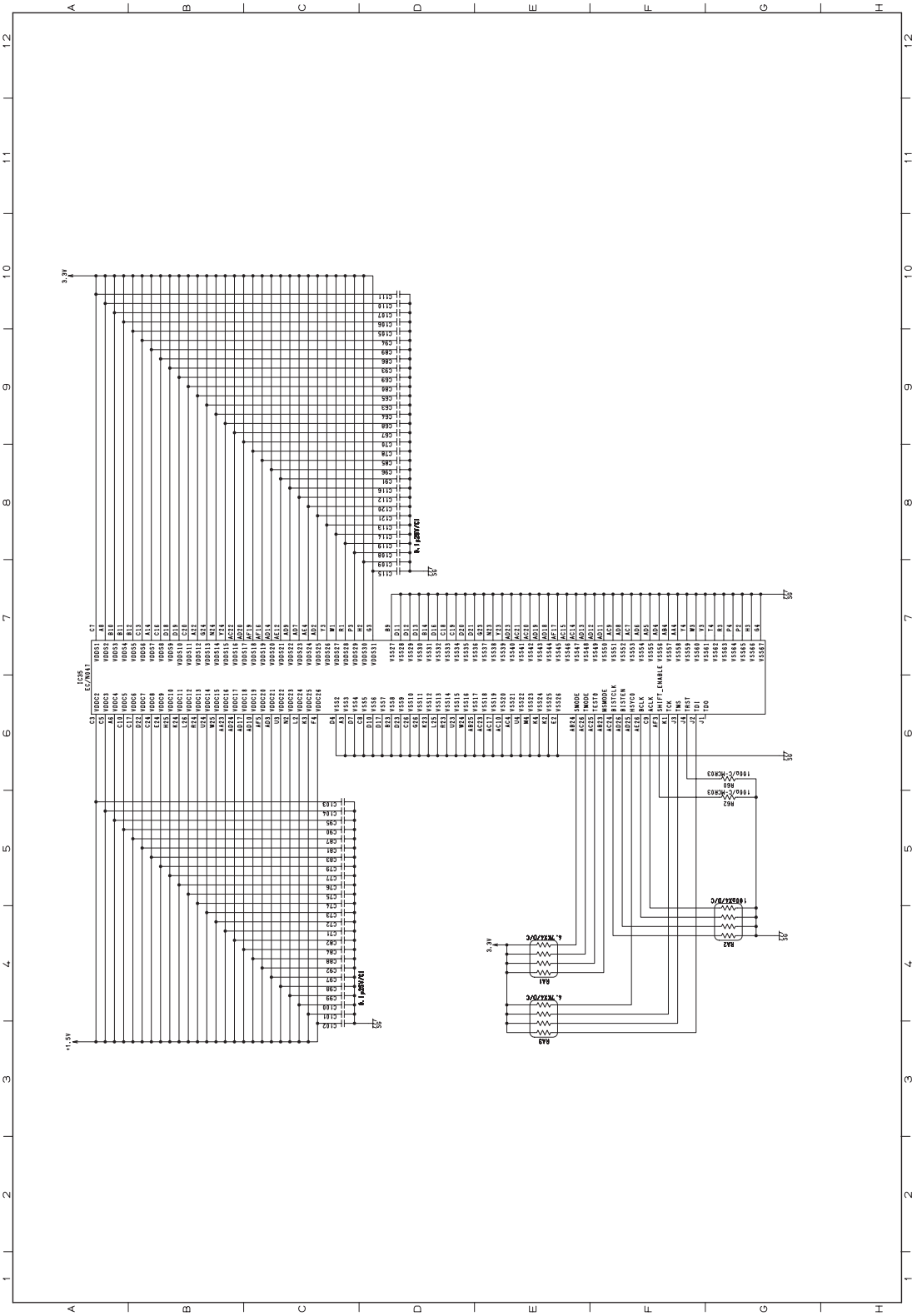

Fig. 3-102

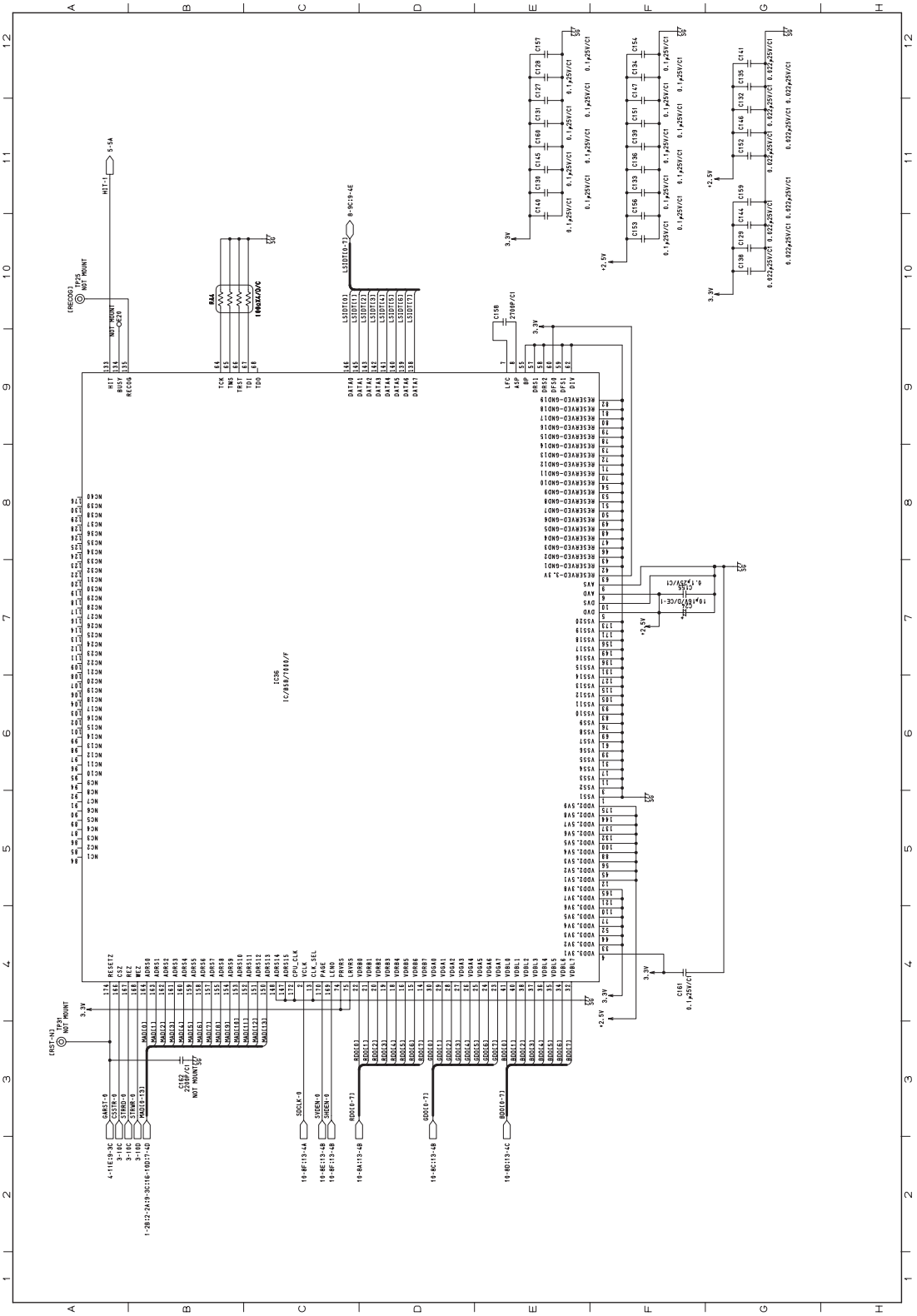

Fig. 3-103

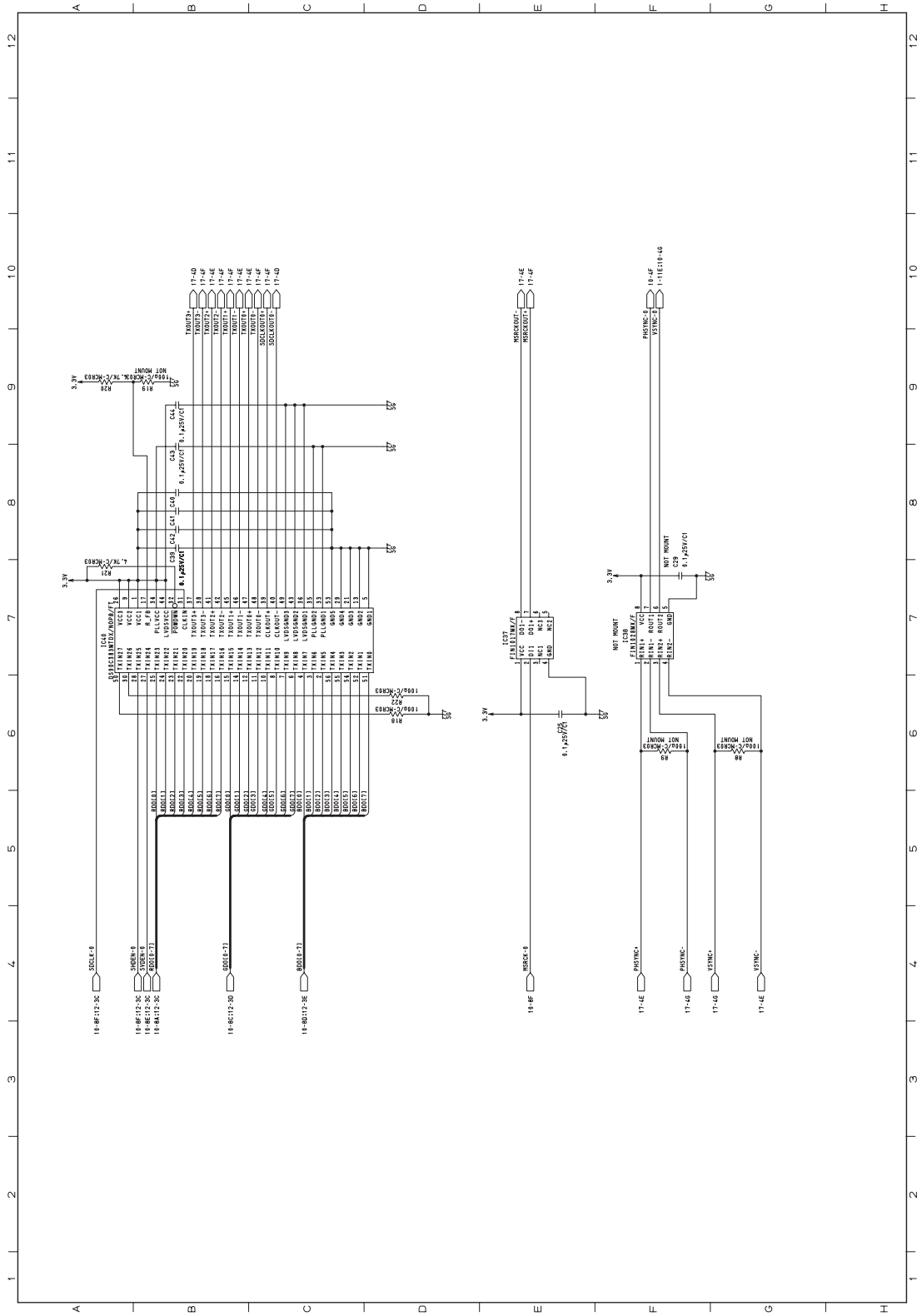

Fig. 3-104

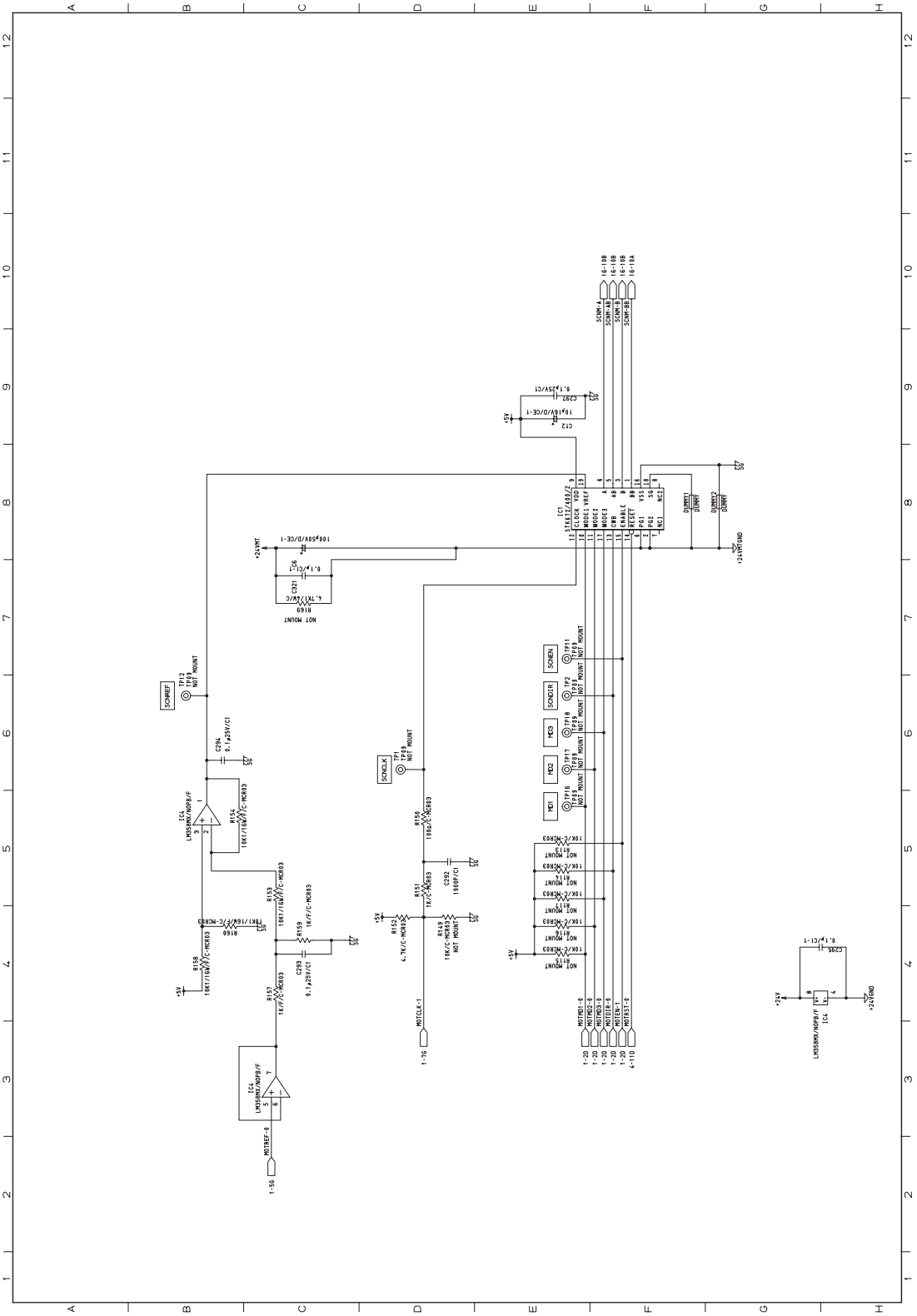

Fig. 3-105

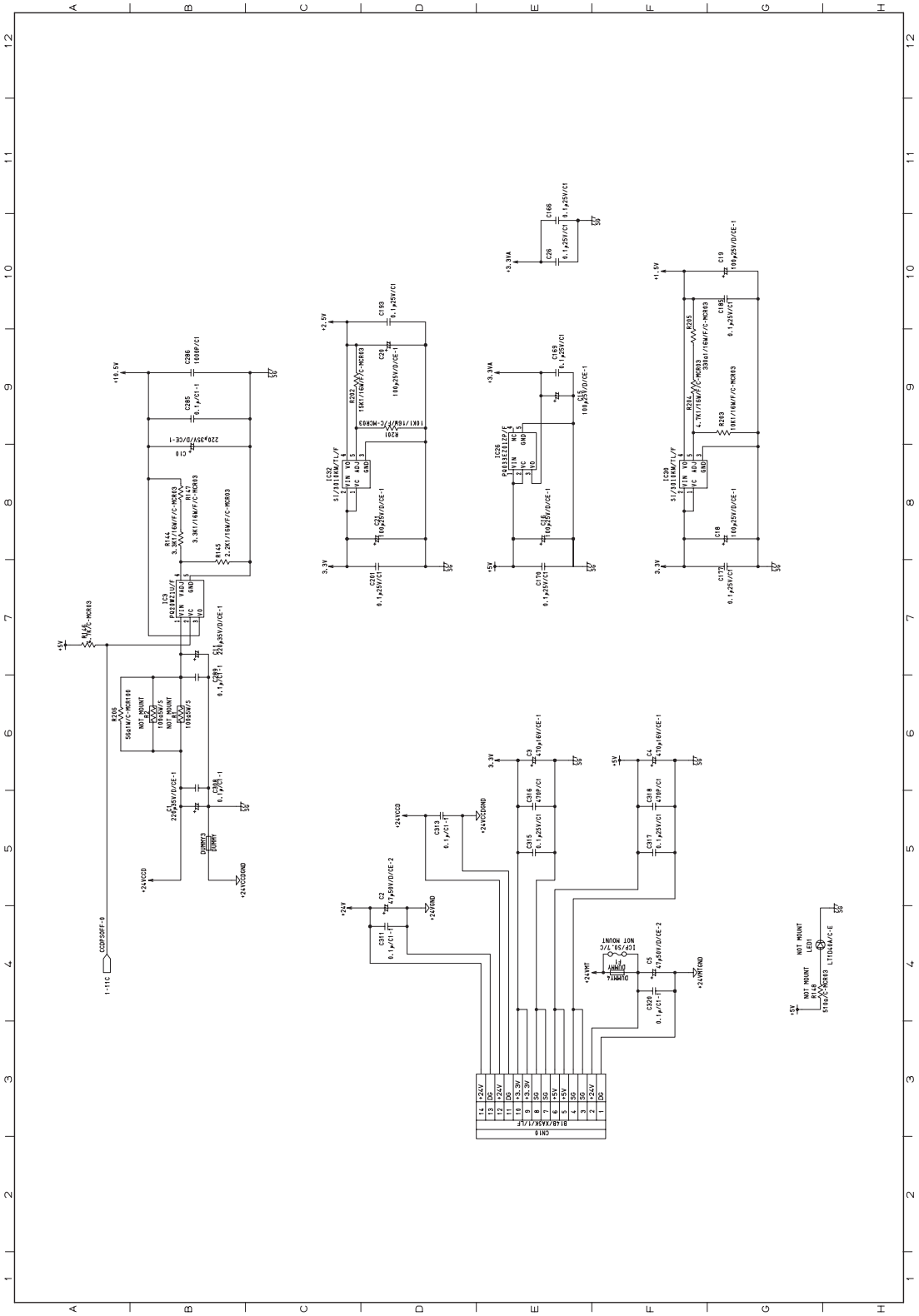

Fig. 3-106

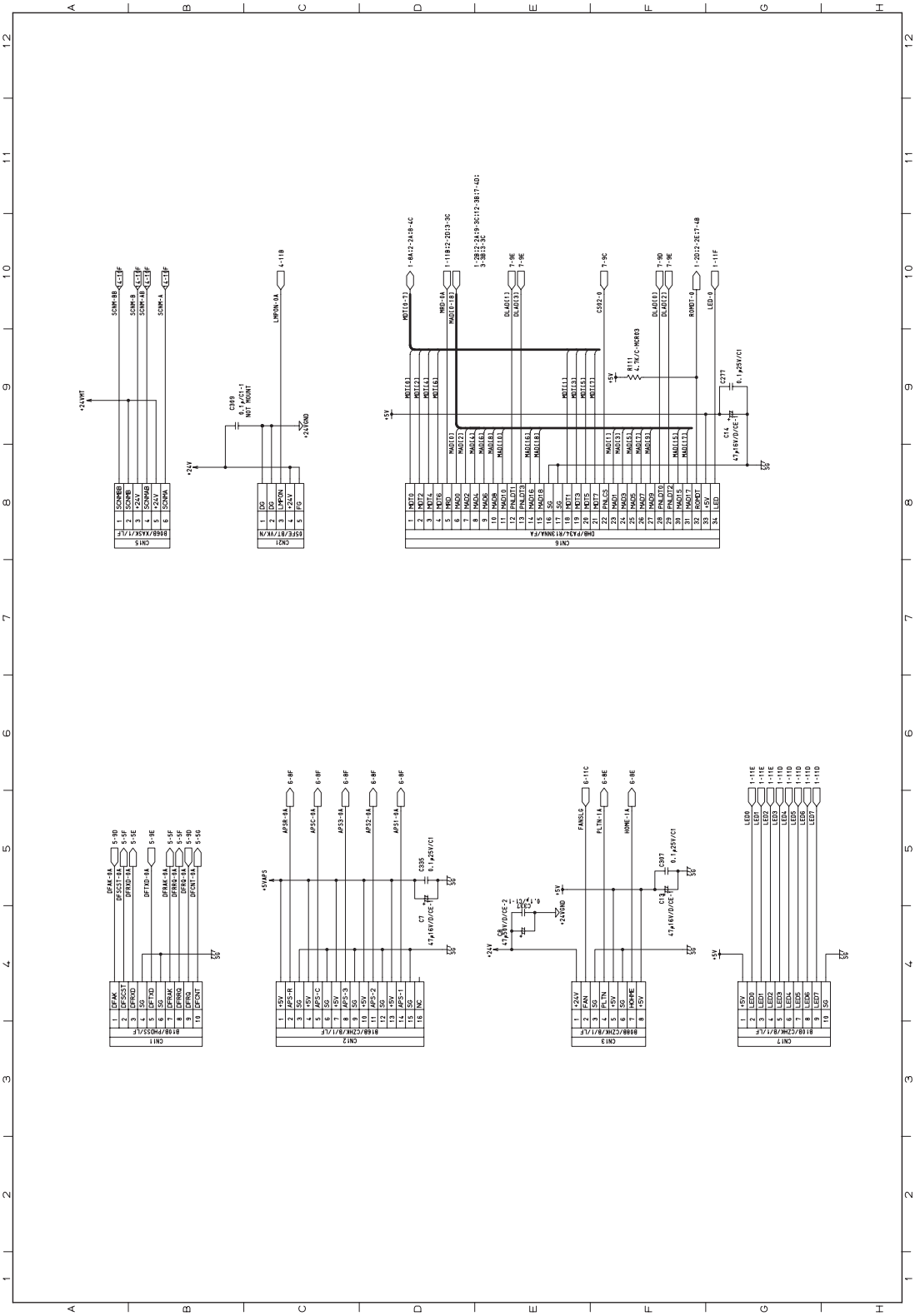

Fig. 3-107

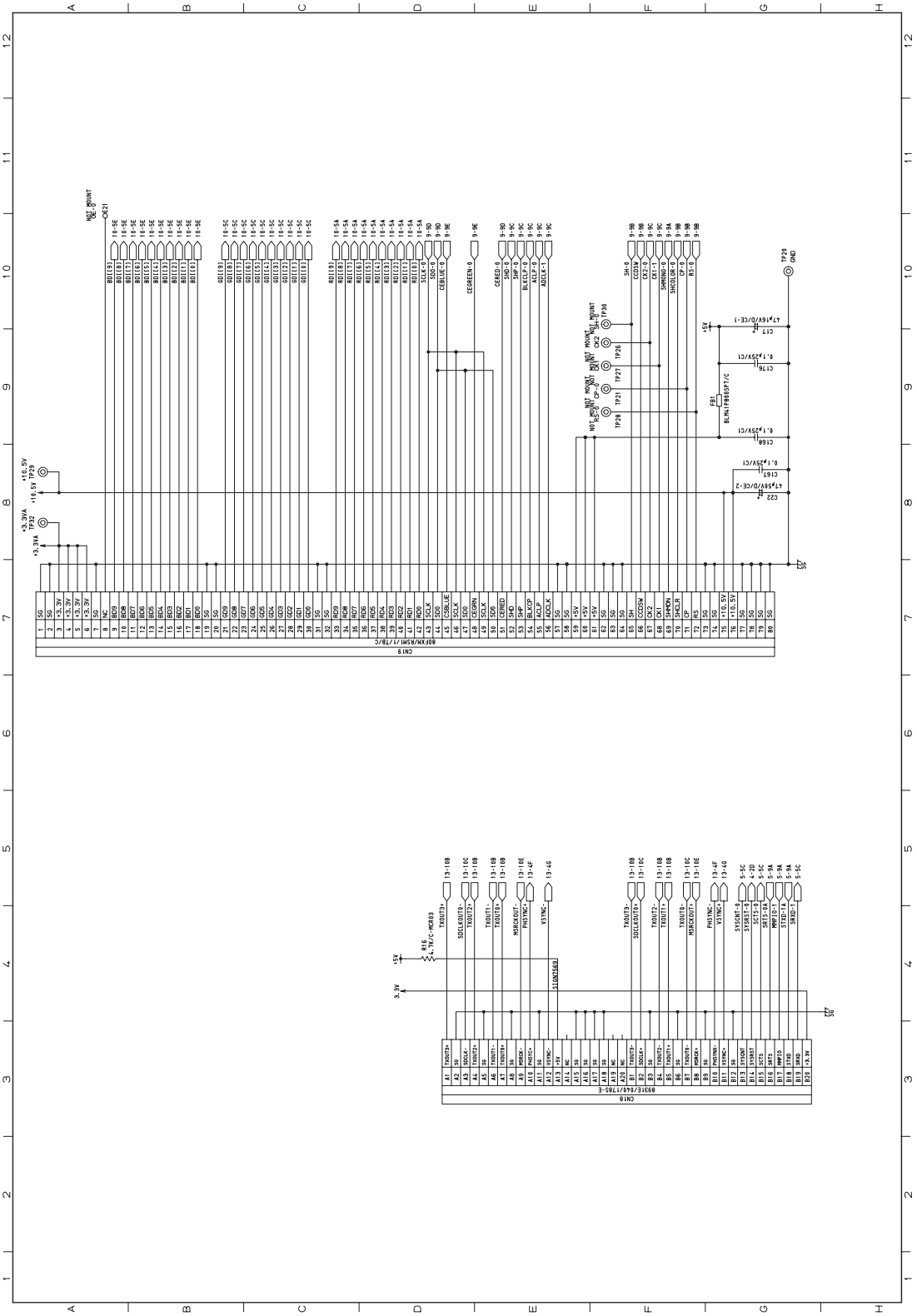

Fig. 3-108

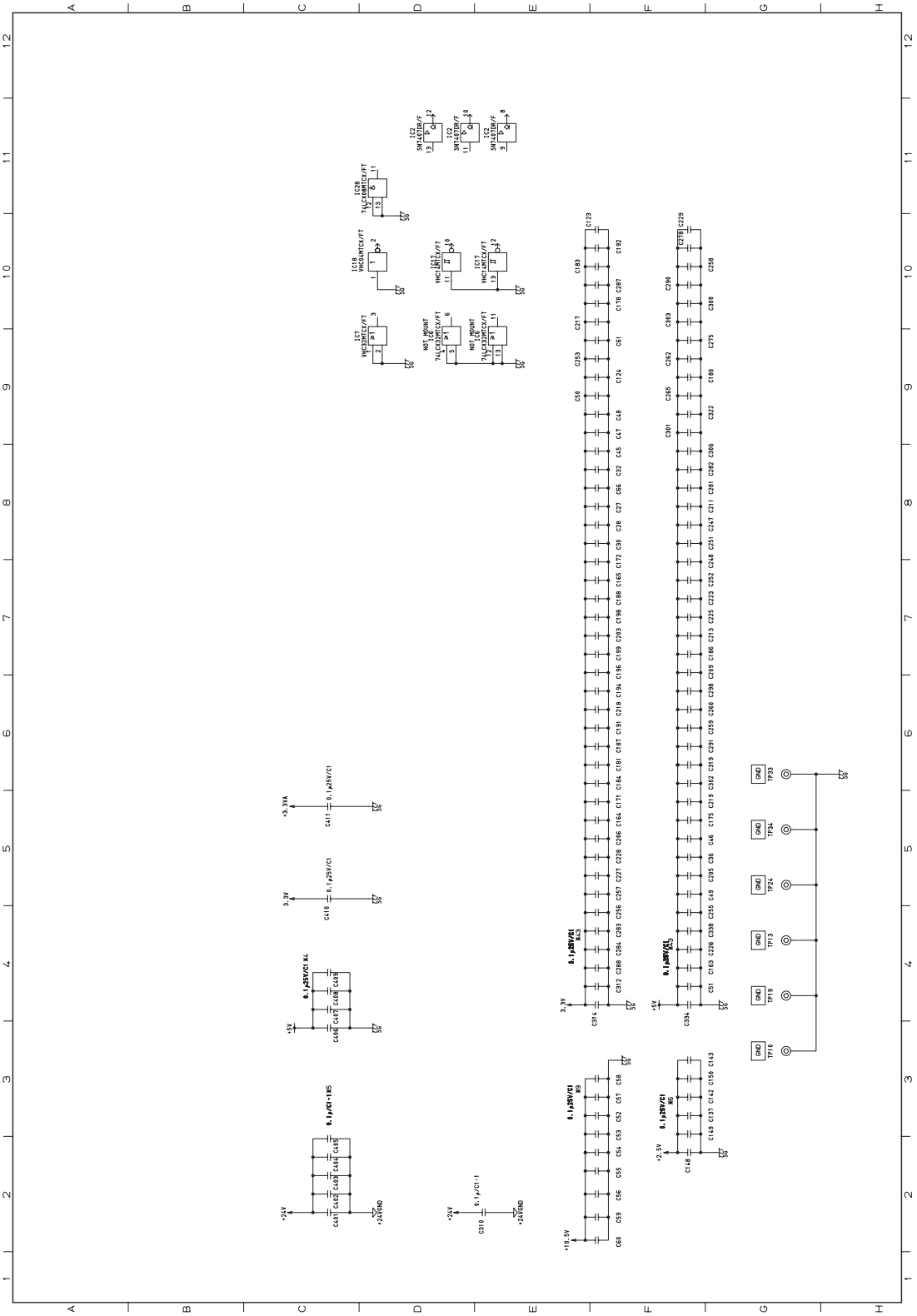

Fig. 3-109

3.6 CCD driving circuit (CCD board)

CCD board 1/5

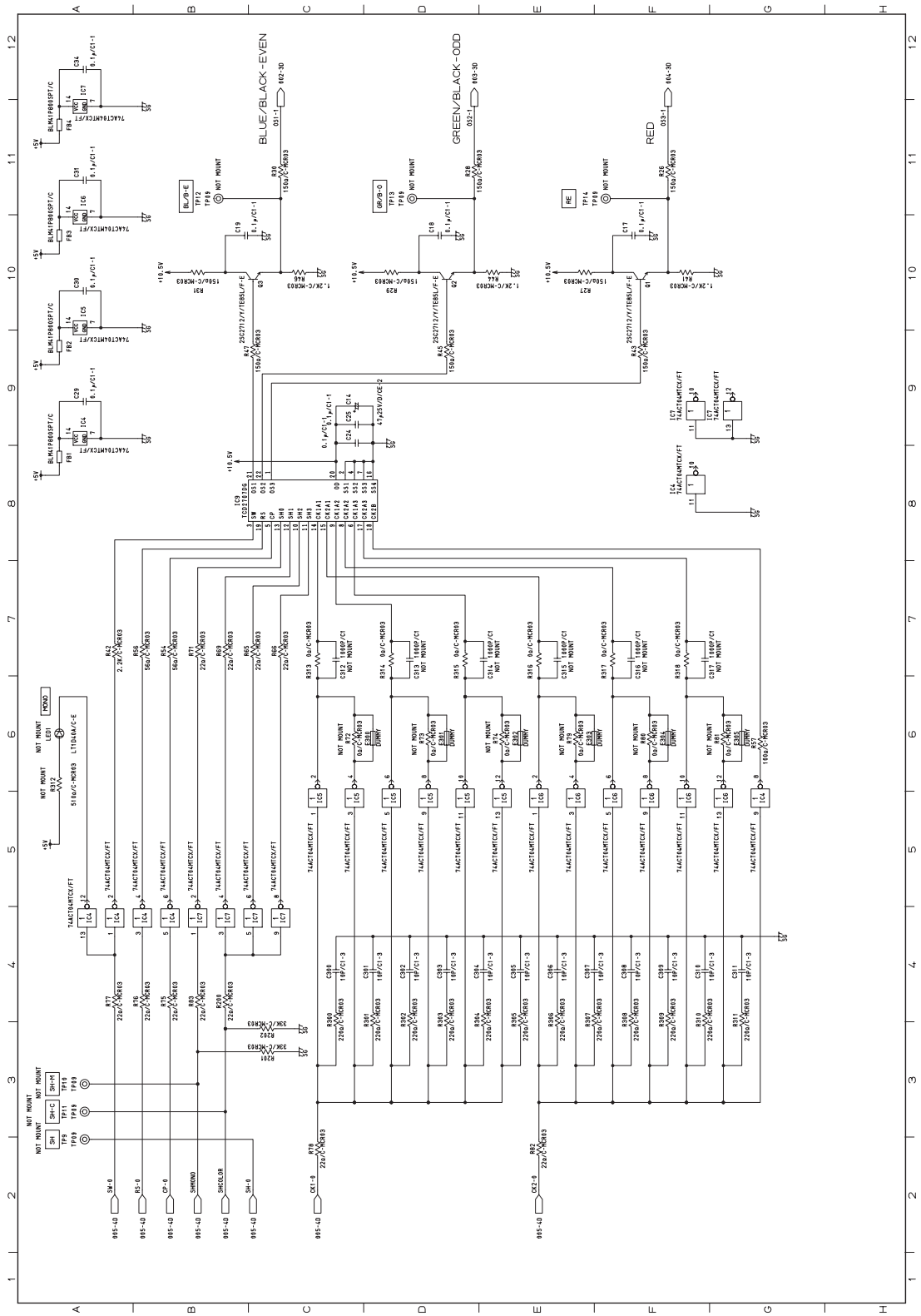

Fig. 3-110

CCD board 2/5

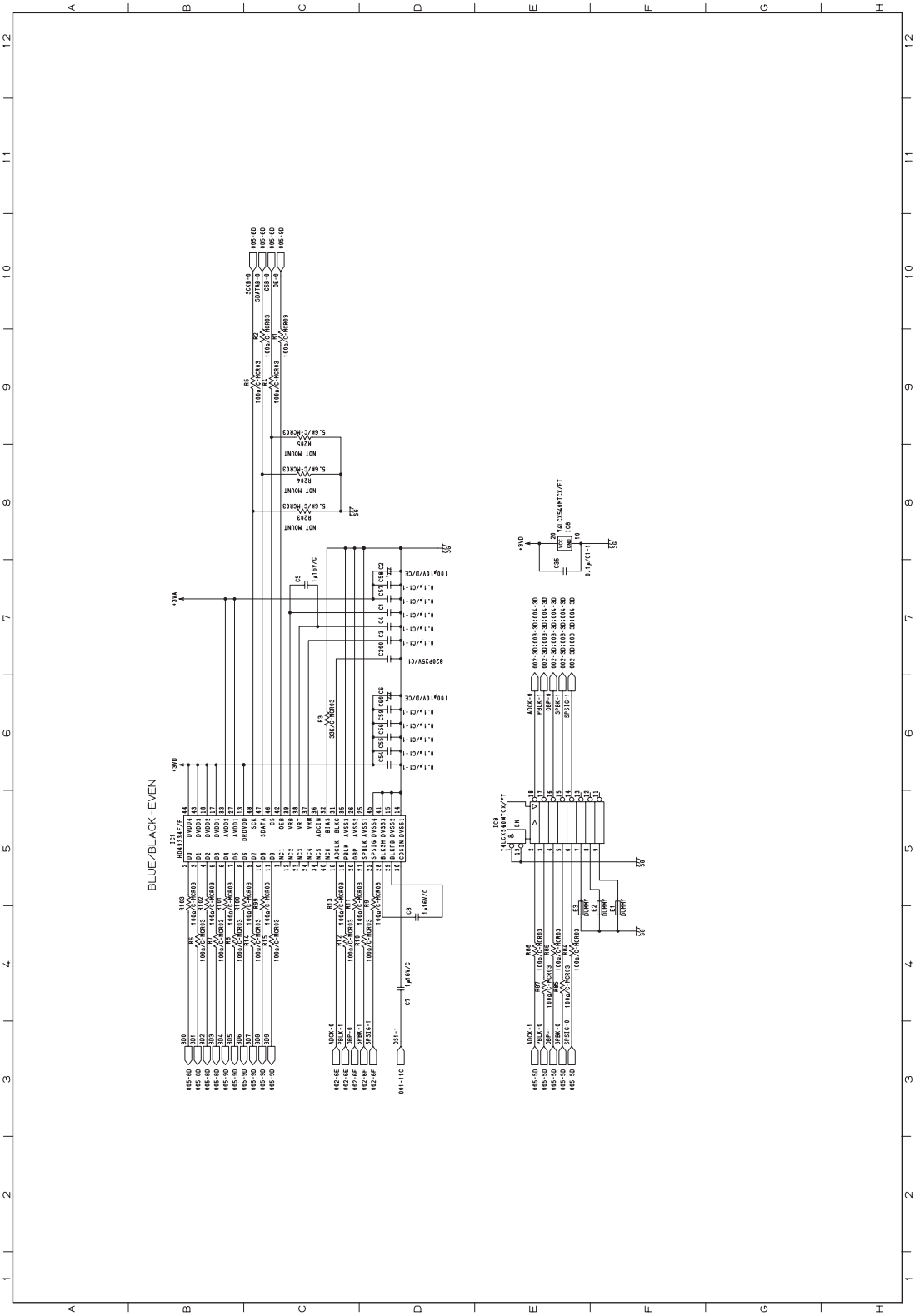

Fig. 3-111

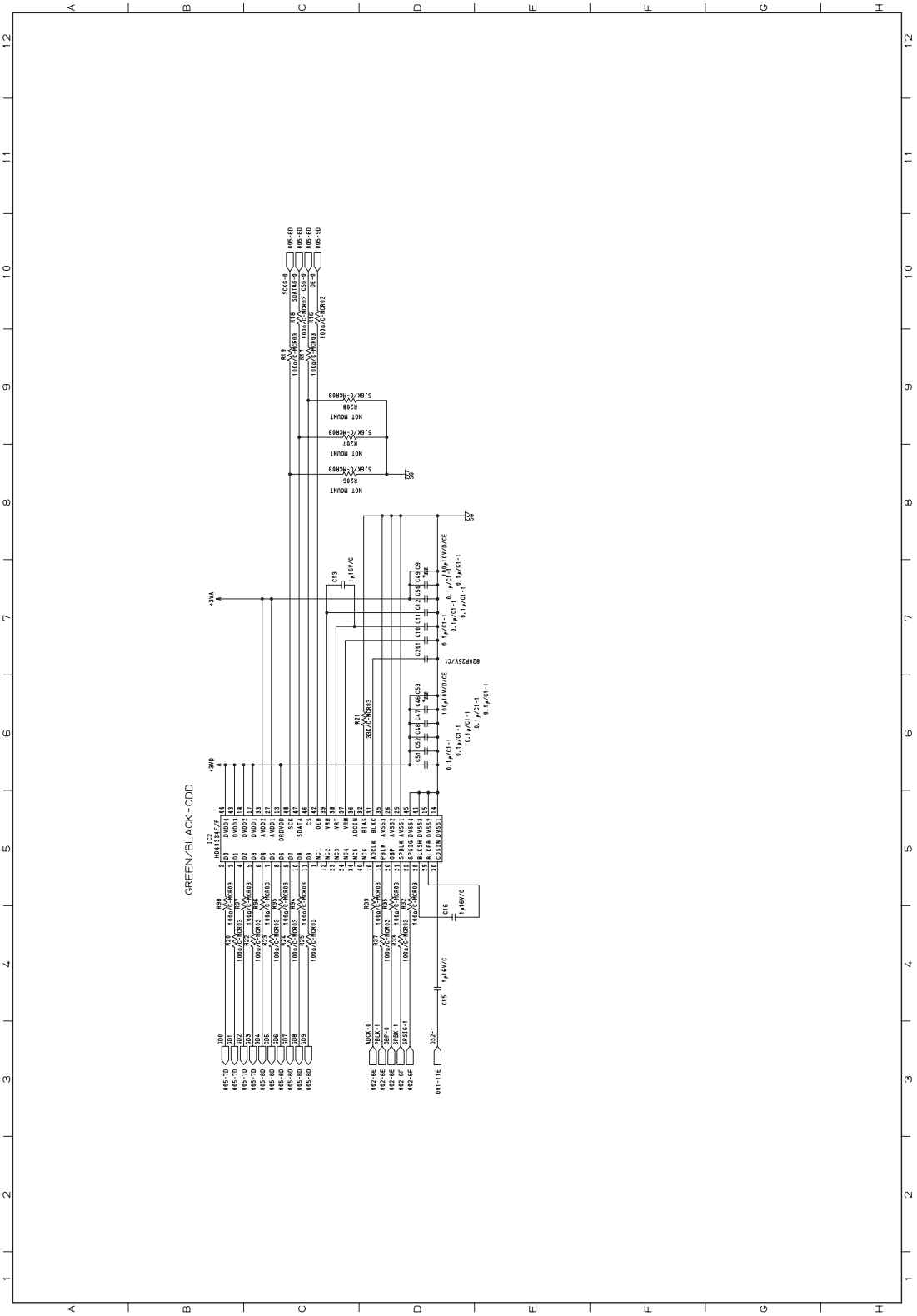

Fig. 3-112

CCD board 4/5

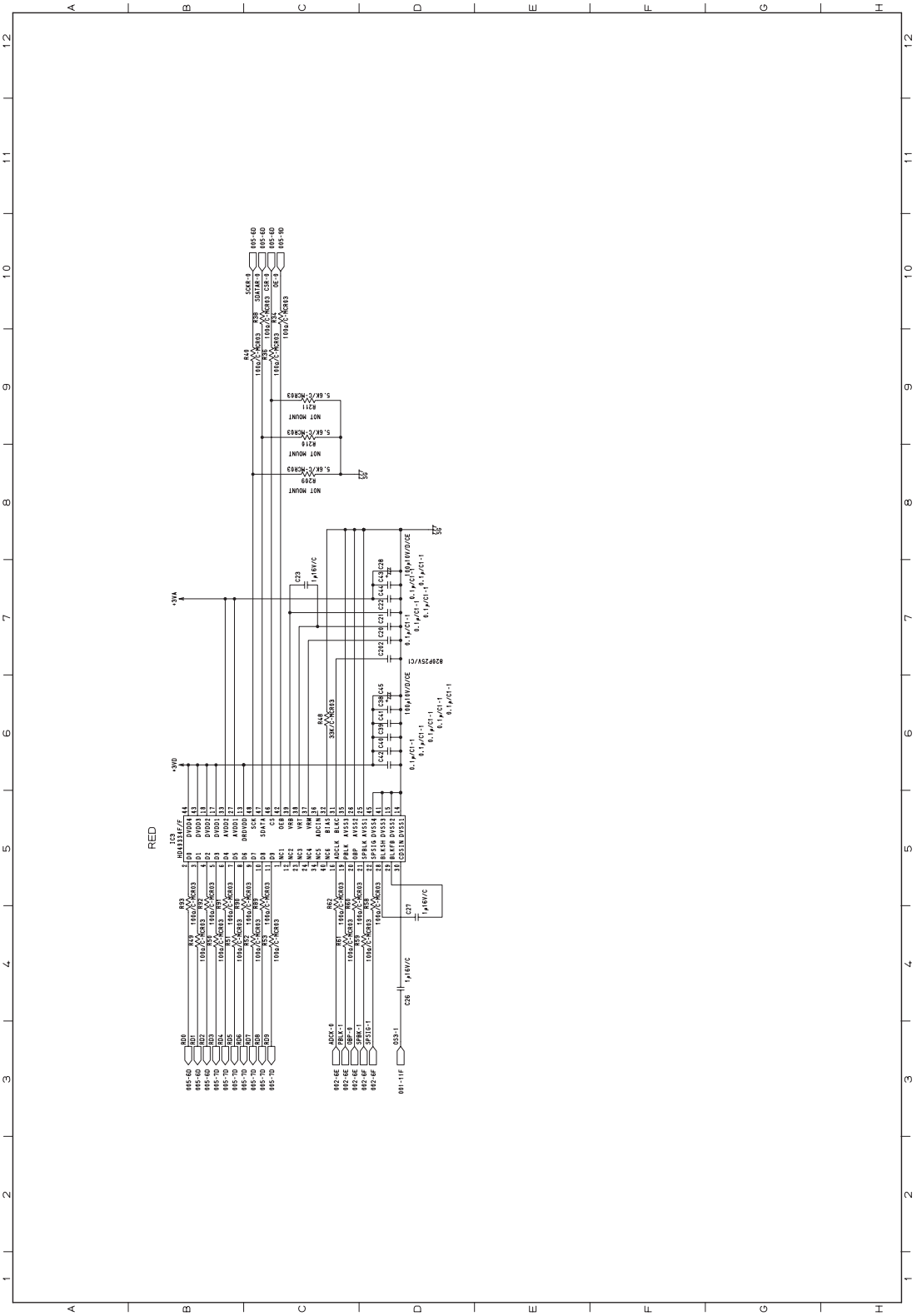

Fig. 3-113

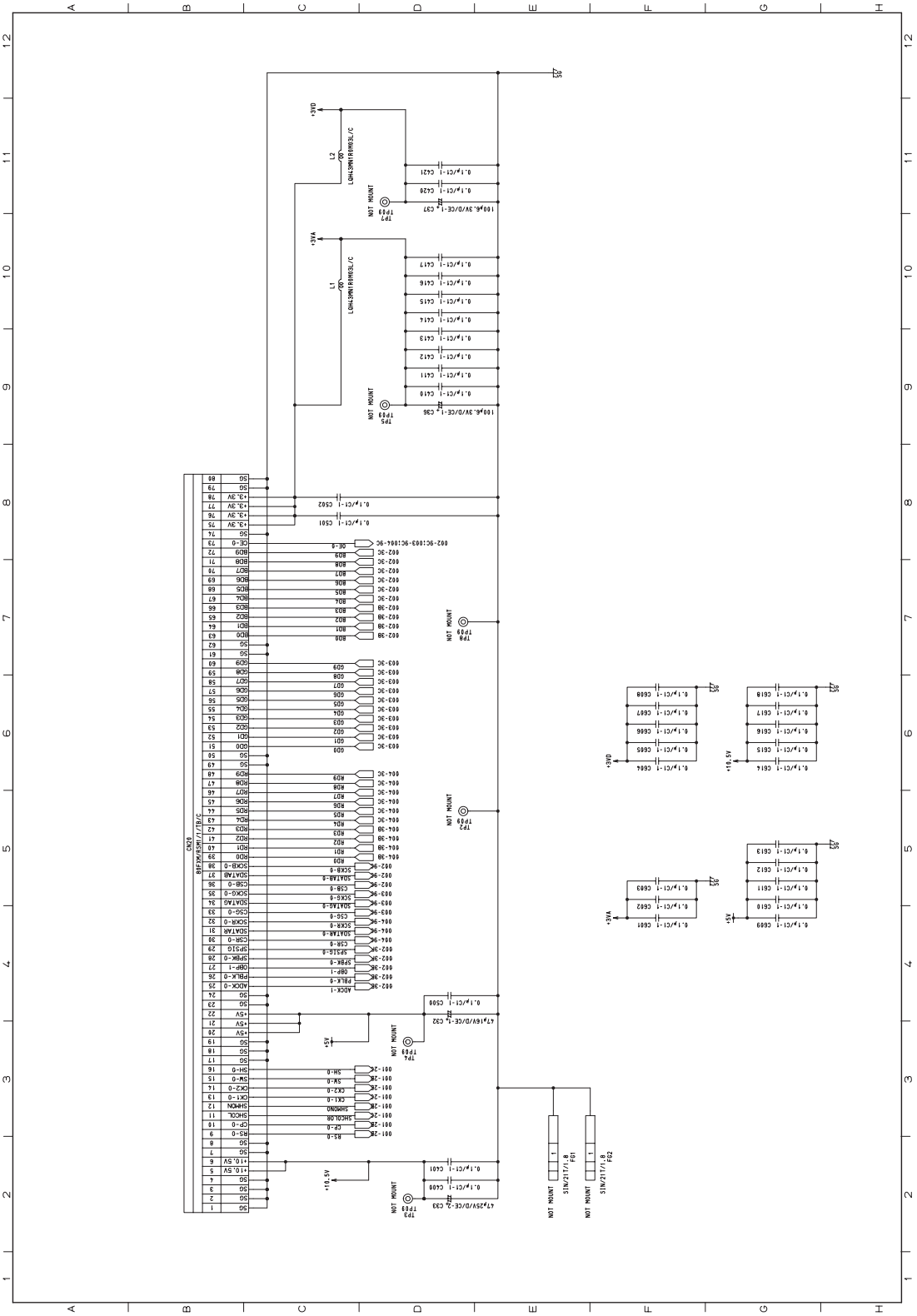

Fig. 3-114

3.7 ADU driving circuit (ADU board)

ADU board 1/2

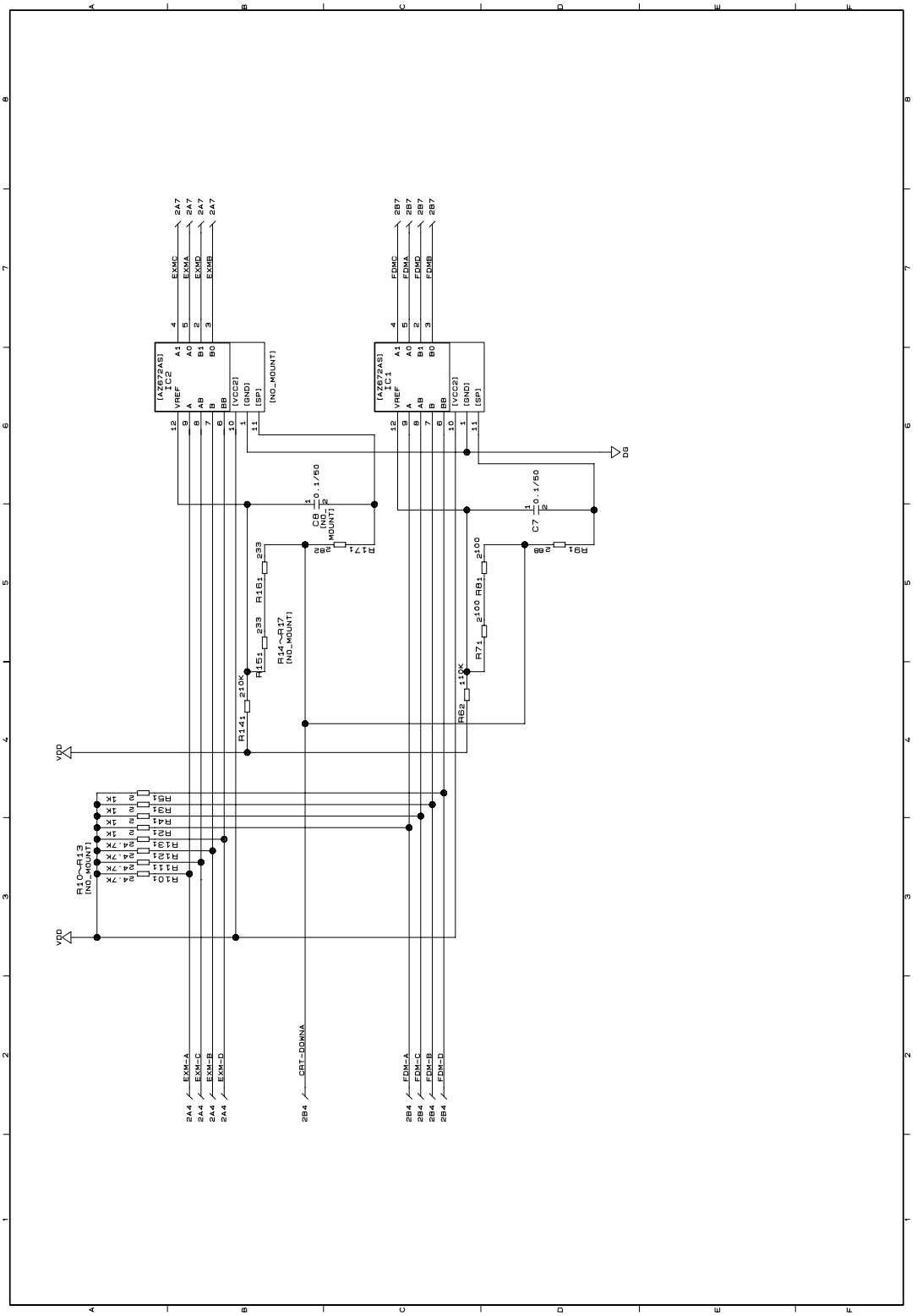

Fig. 3-115

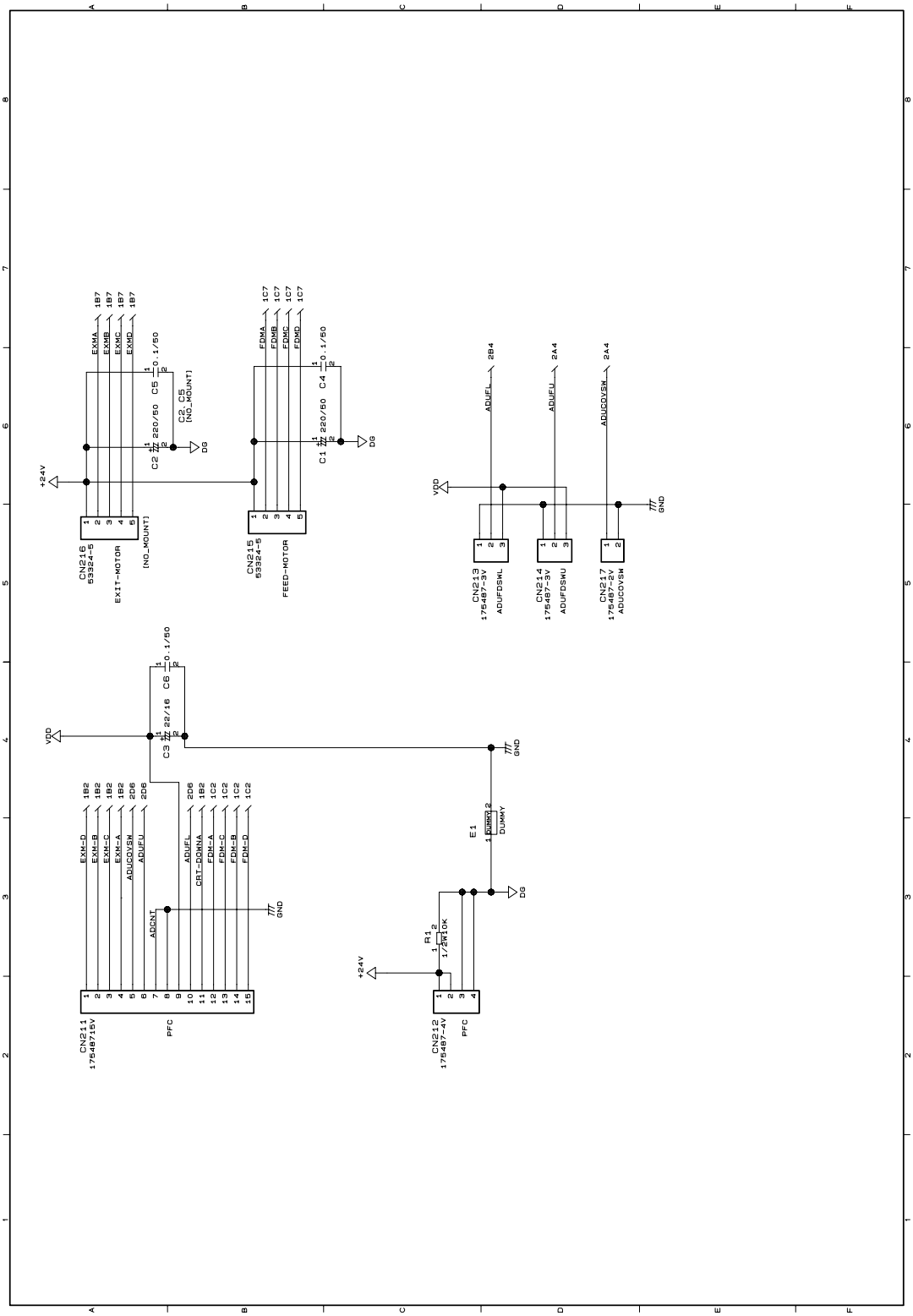

Fig. 3-116

3.8 Display circuit (DSP board)

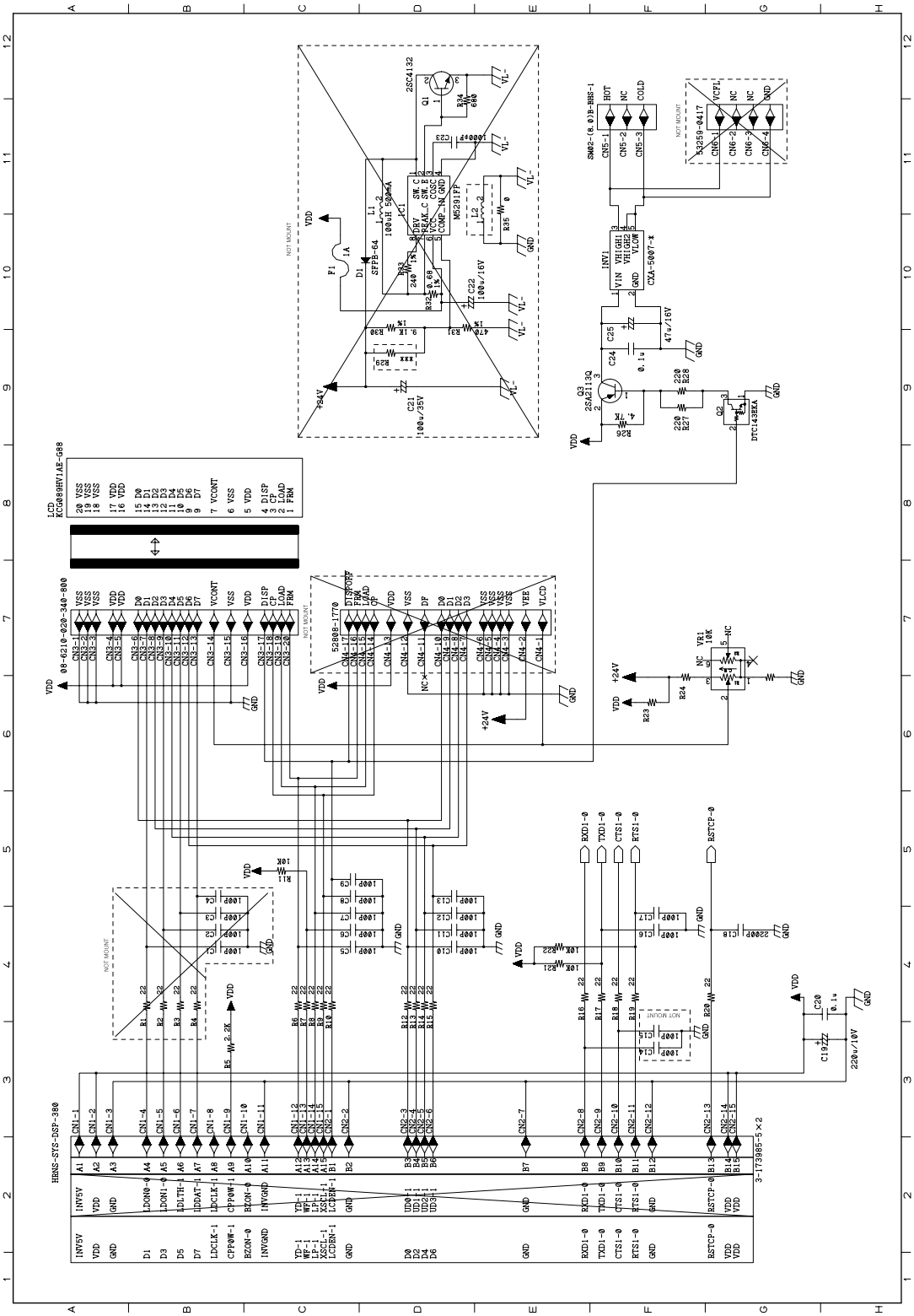

Fig. 3-117

3.9 Key control circuit (KEY board)

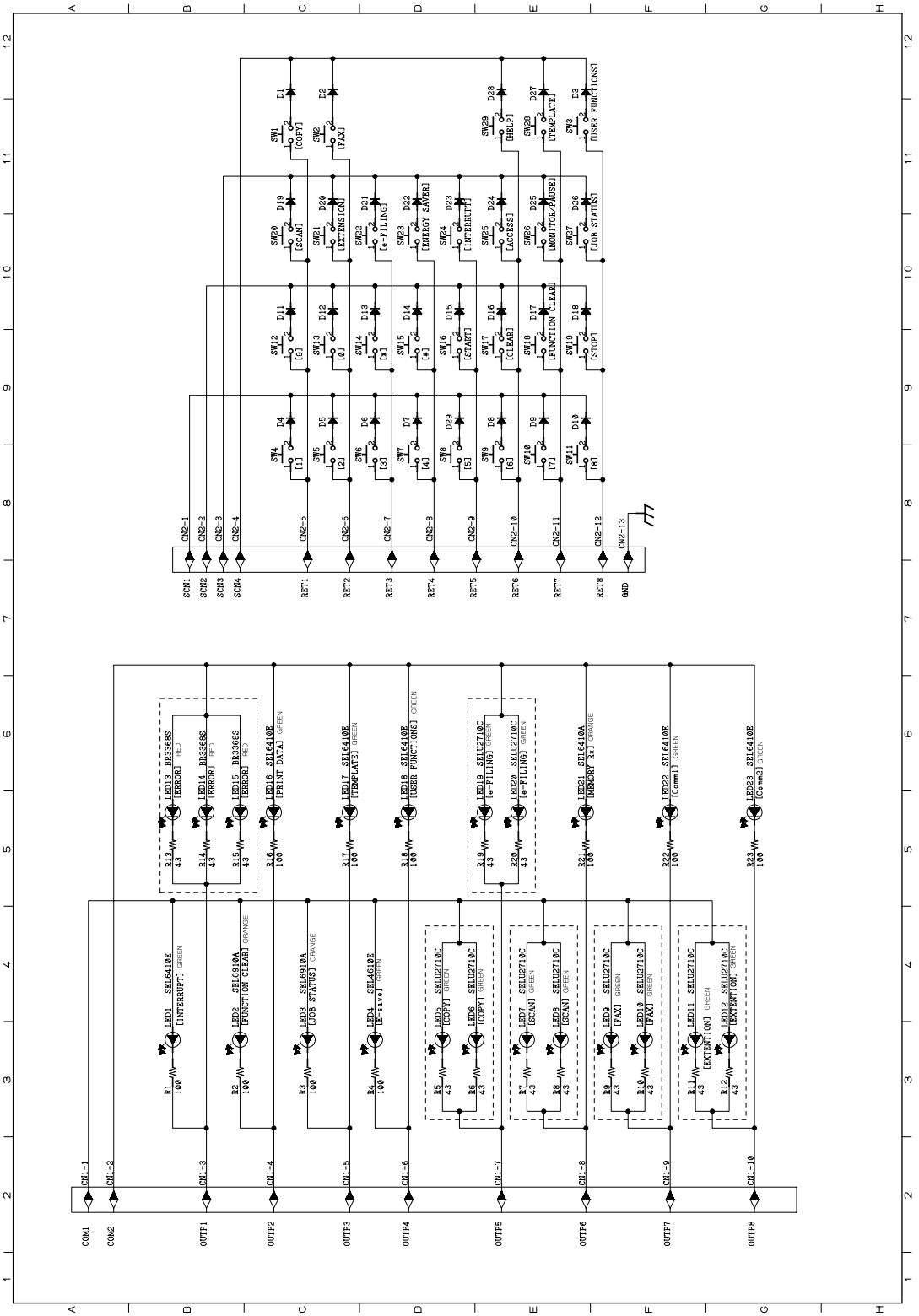

Fig. 3-118

3.10 Filter circuit (FIL board)

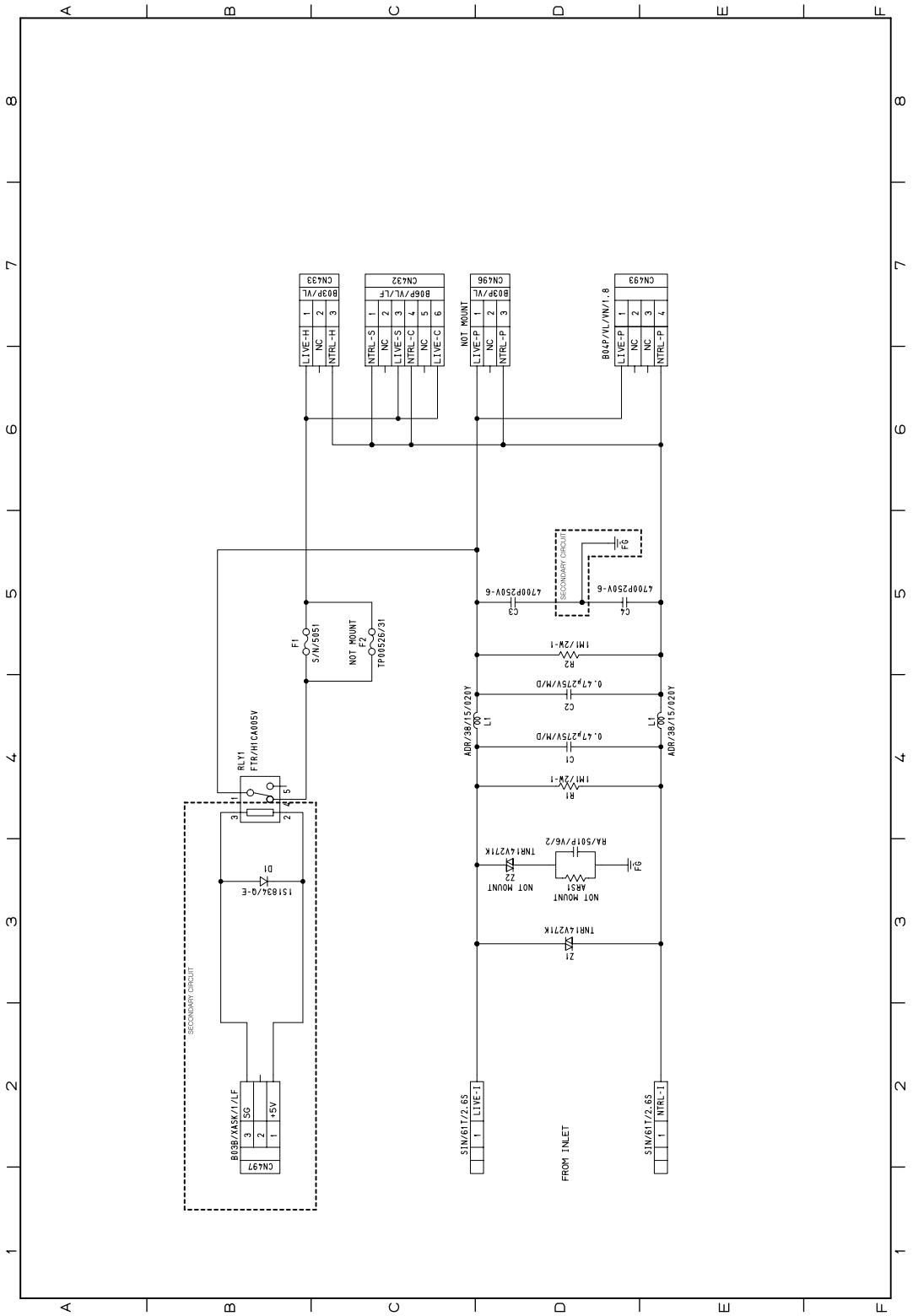

Fig. 3-119

3.11 Facsimile circuit (FAX board: GD-1210)

FAX board 1/14

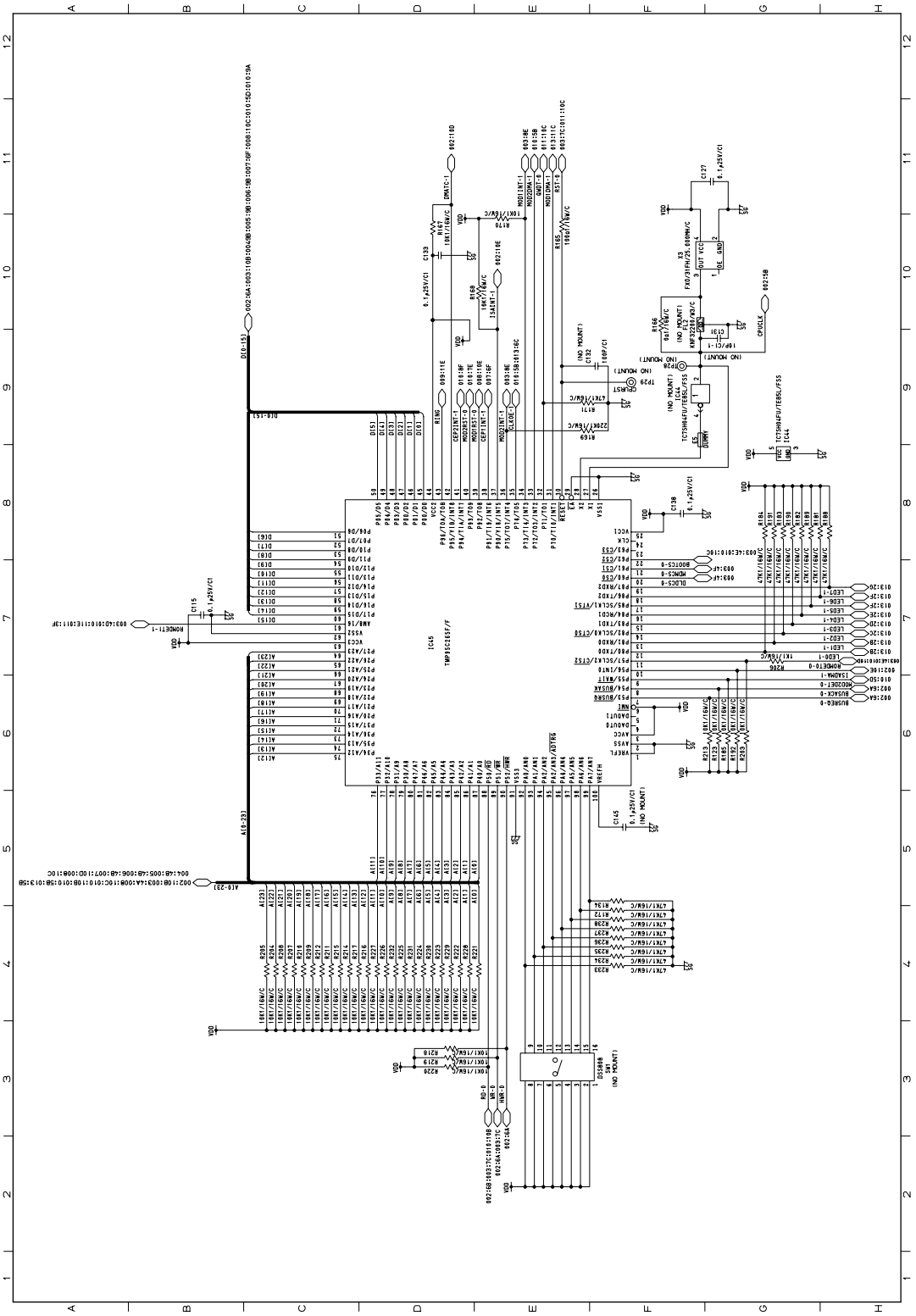

Fig. 3-120

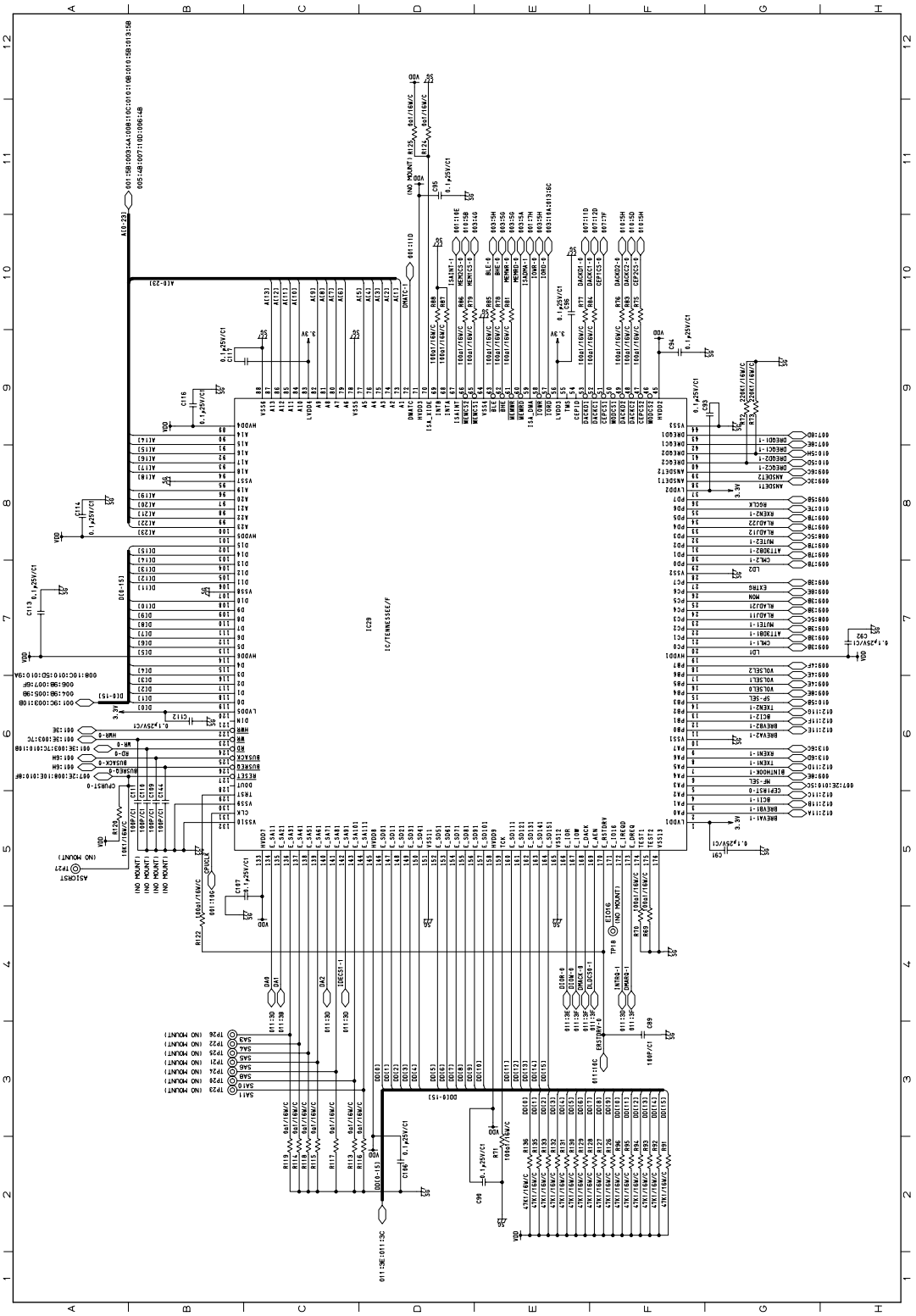

Fig. 3-121

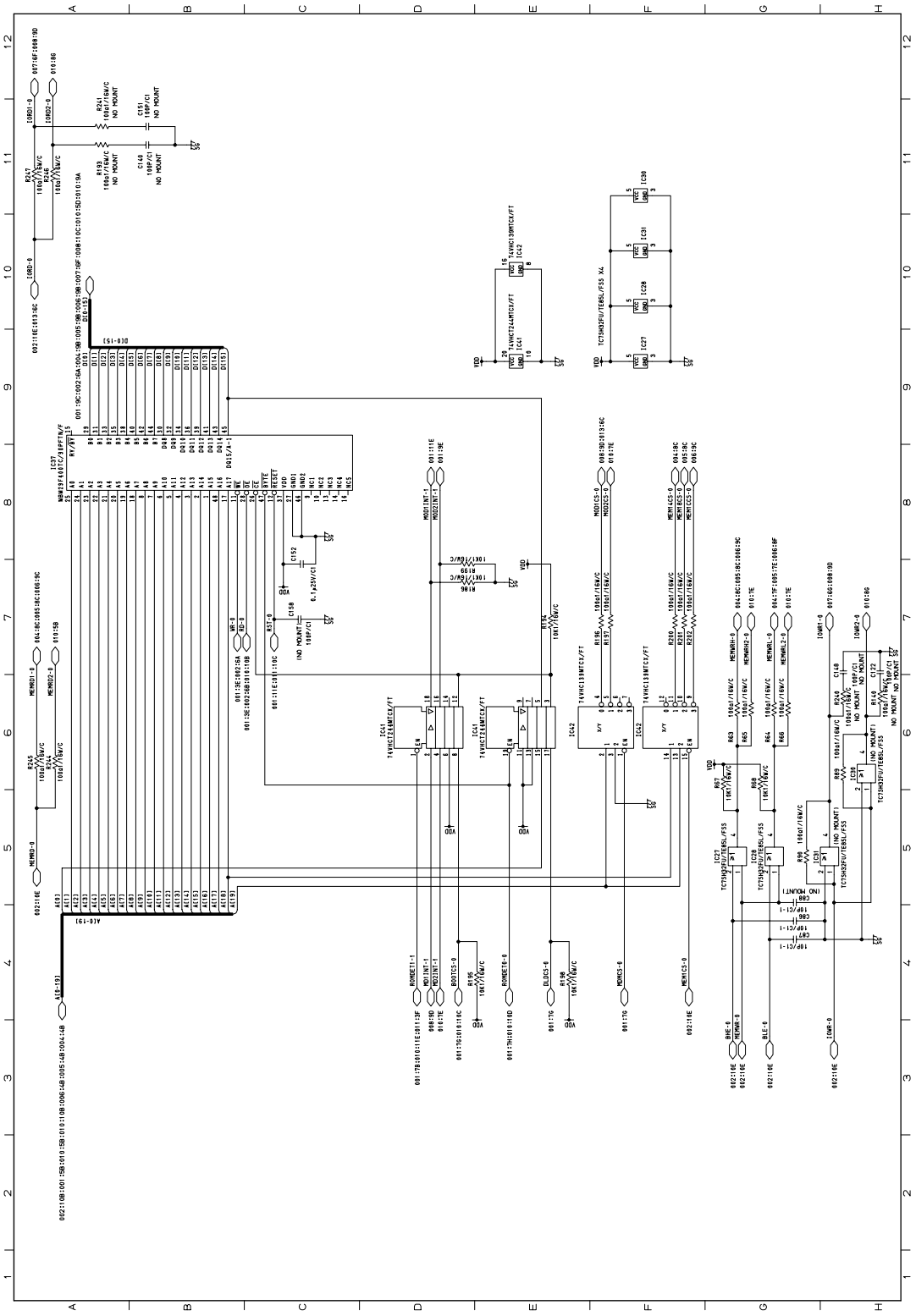

Fig. 3-122

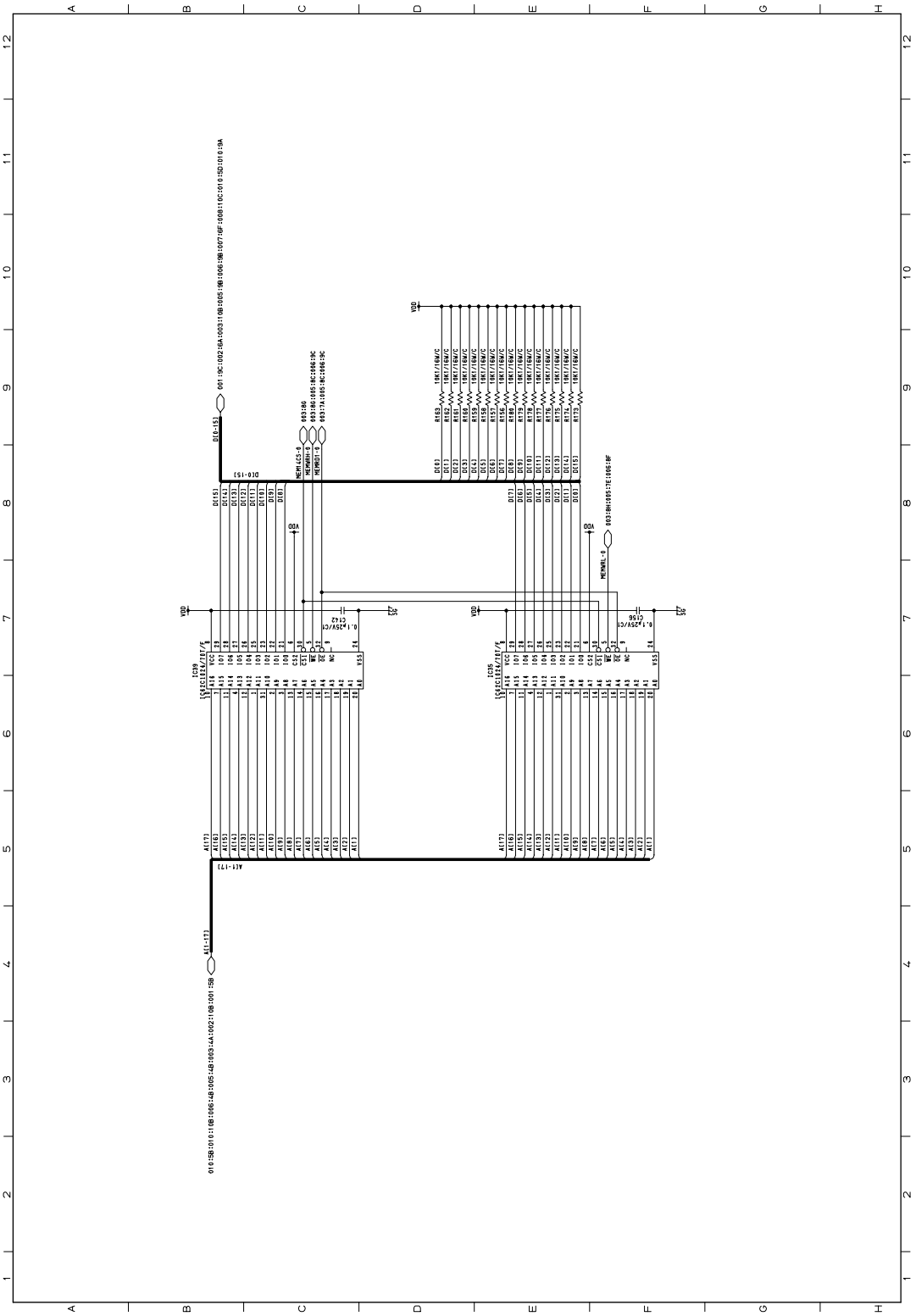

Fig. 3-123

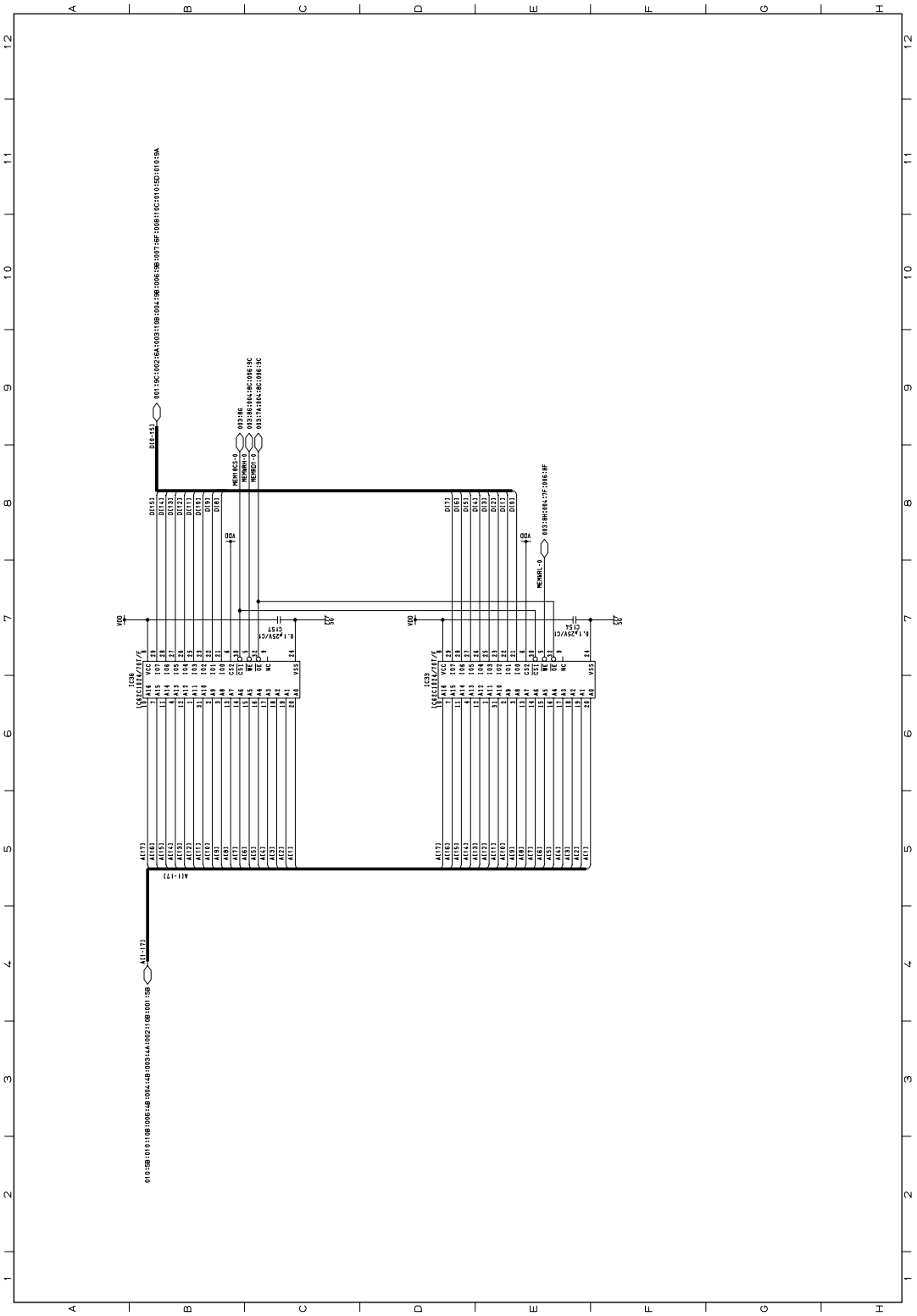

Fig. 3-124

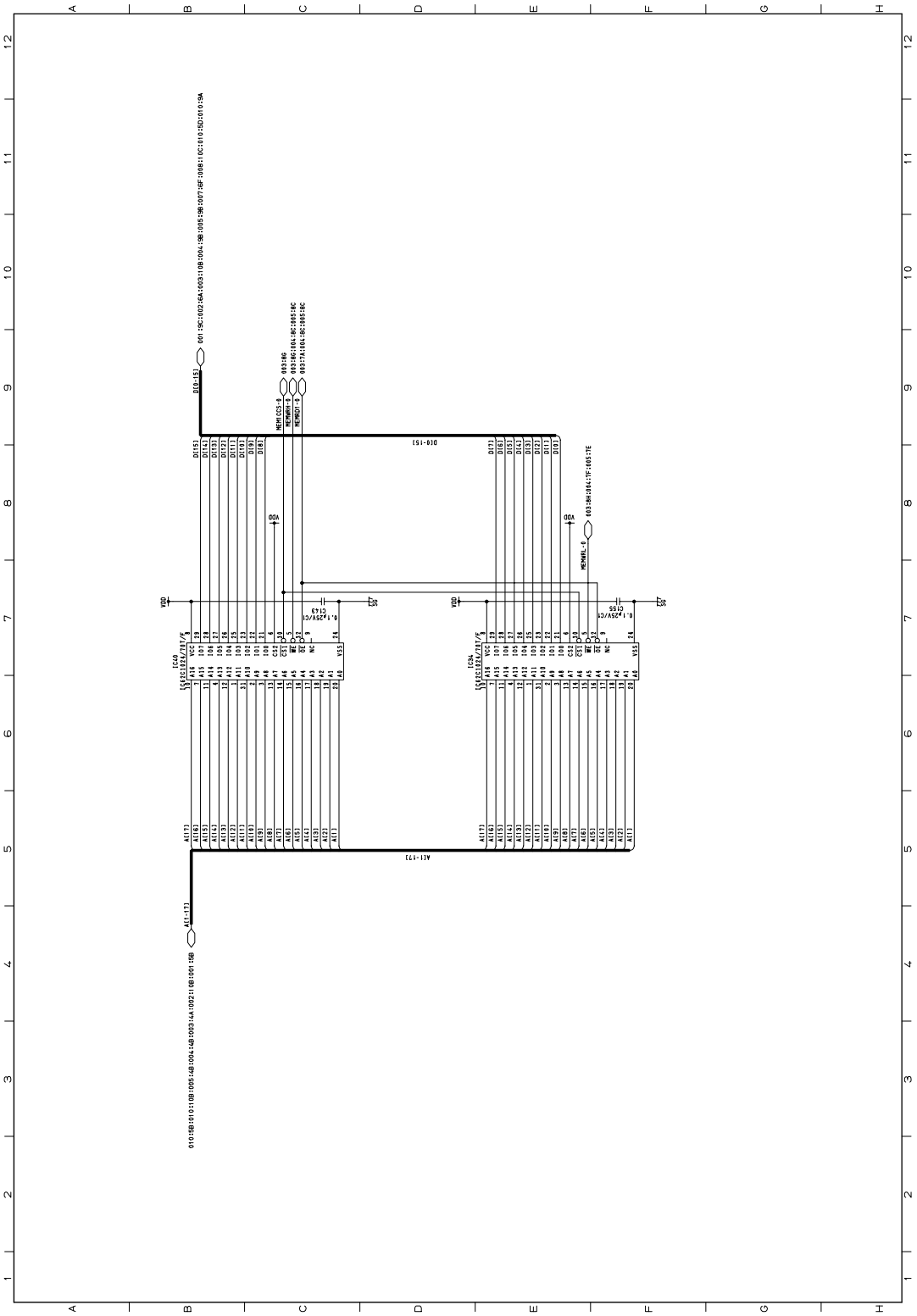

Fig. 3-125

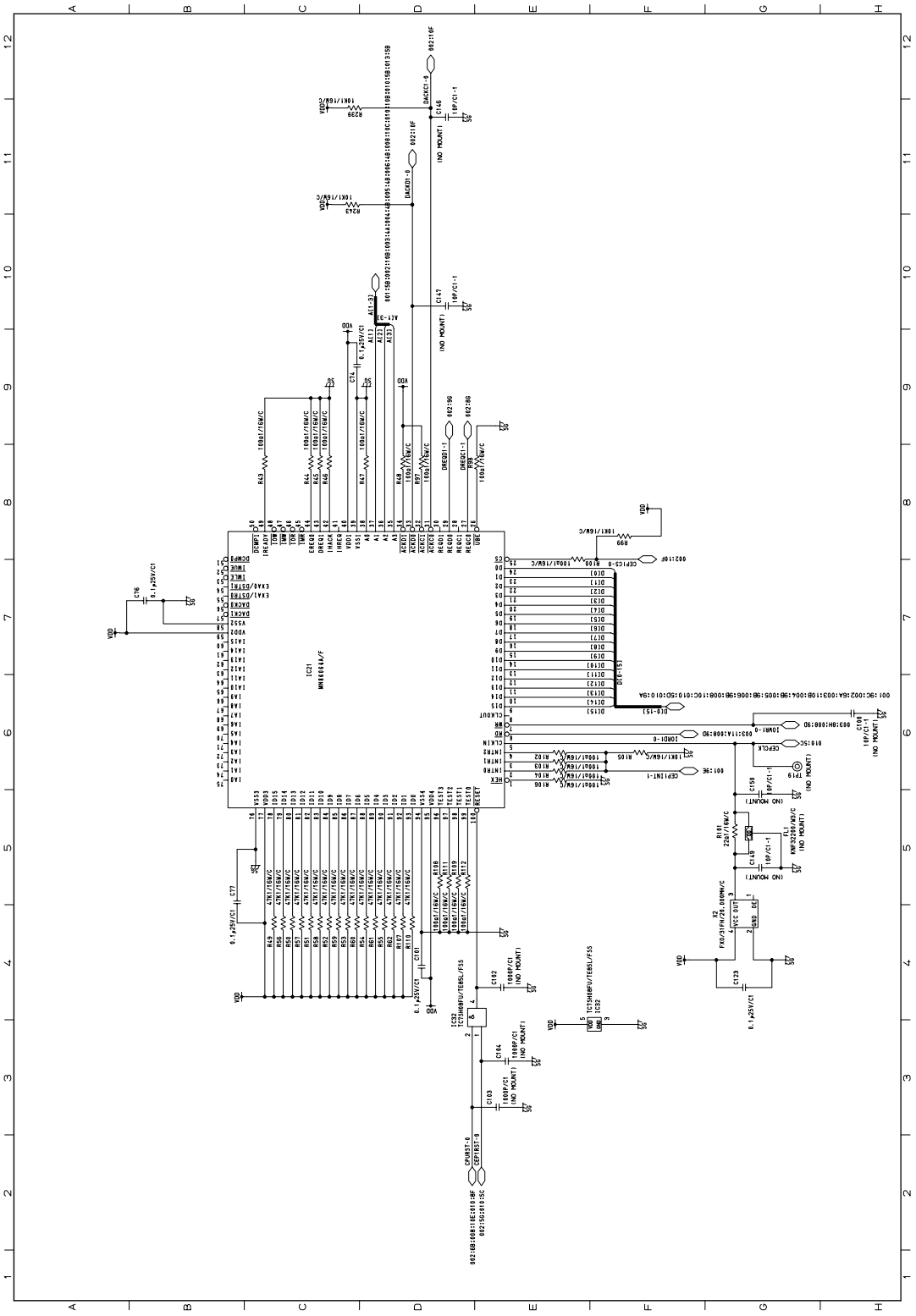

Fig. 3-126

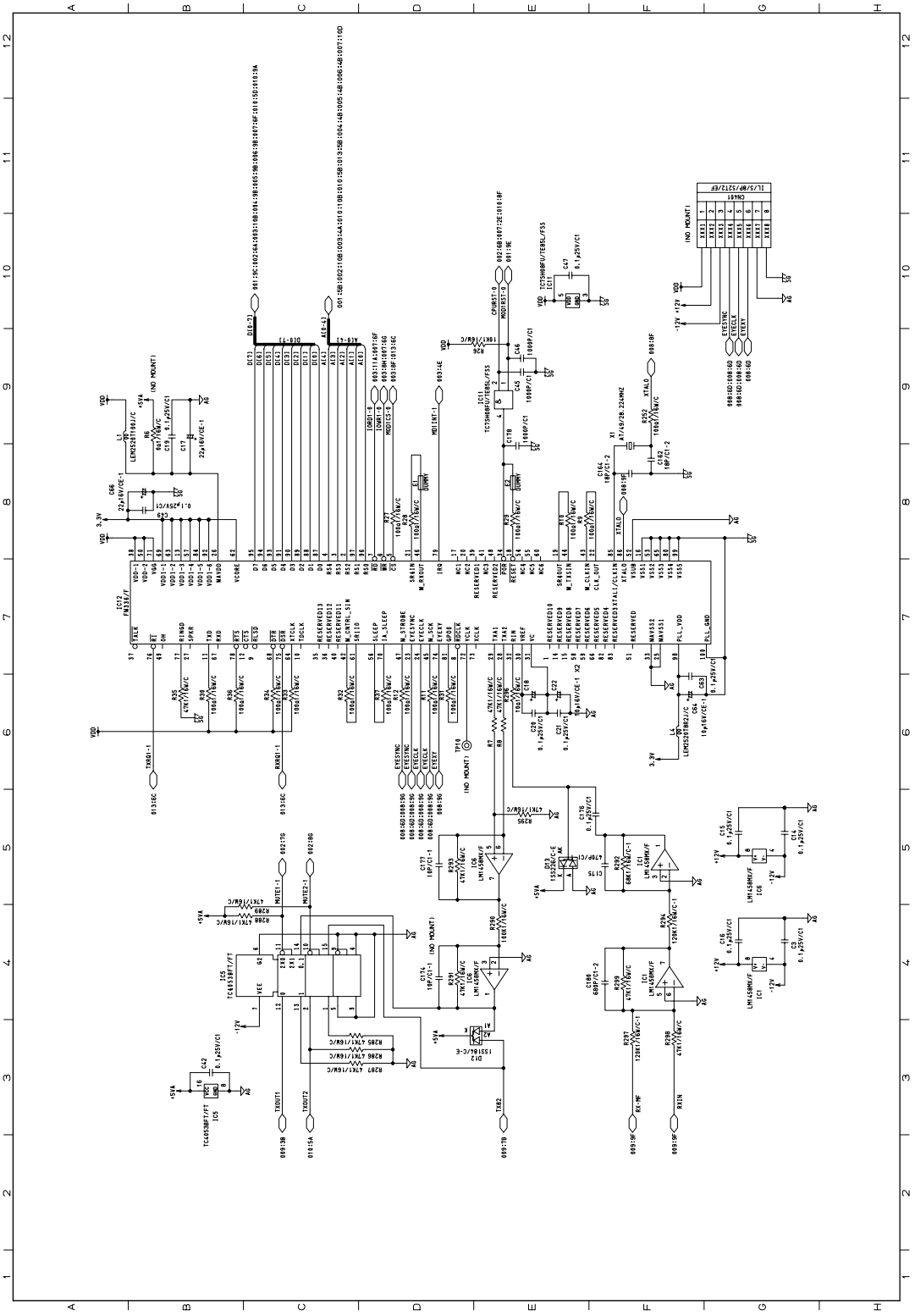

Fig. 3-127

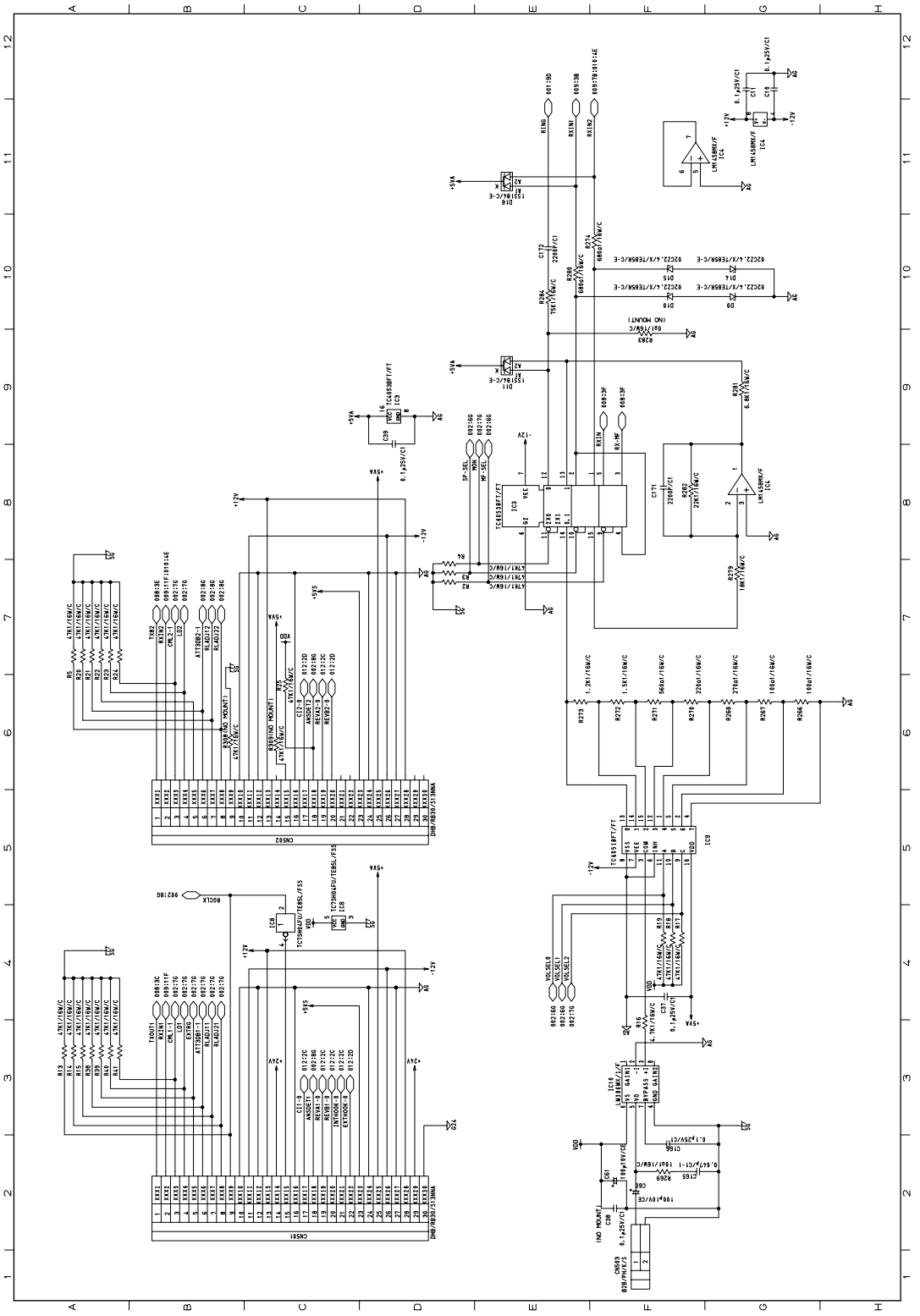

Fig. 3-128

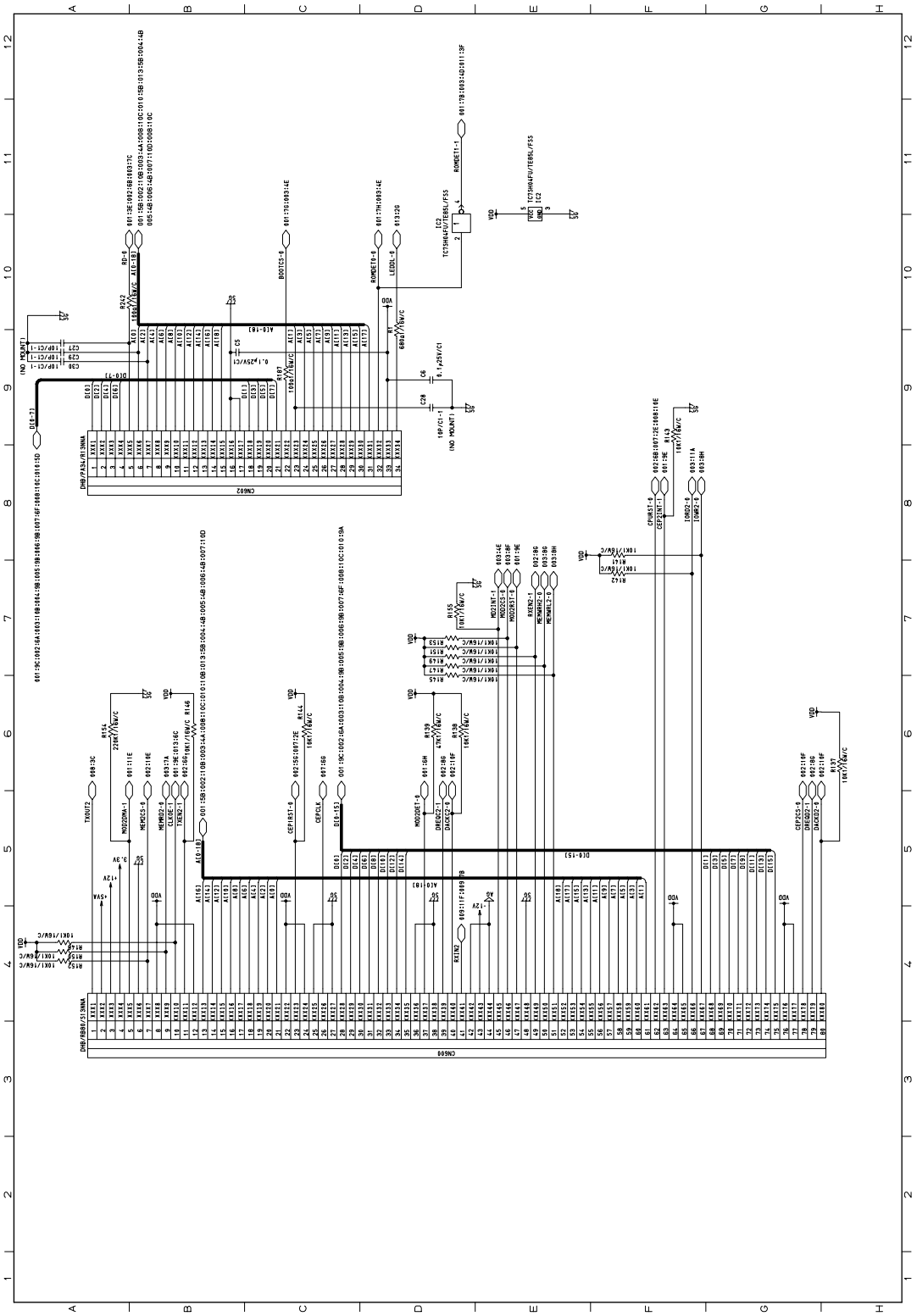

Fig. 3-129

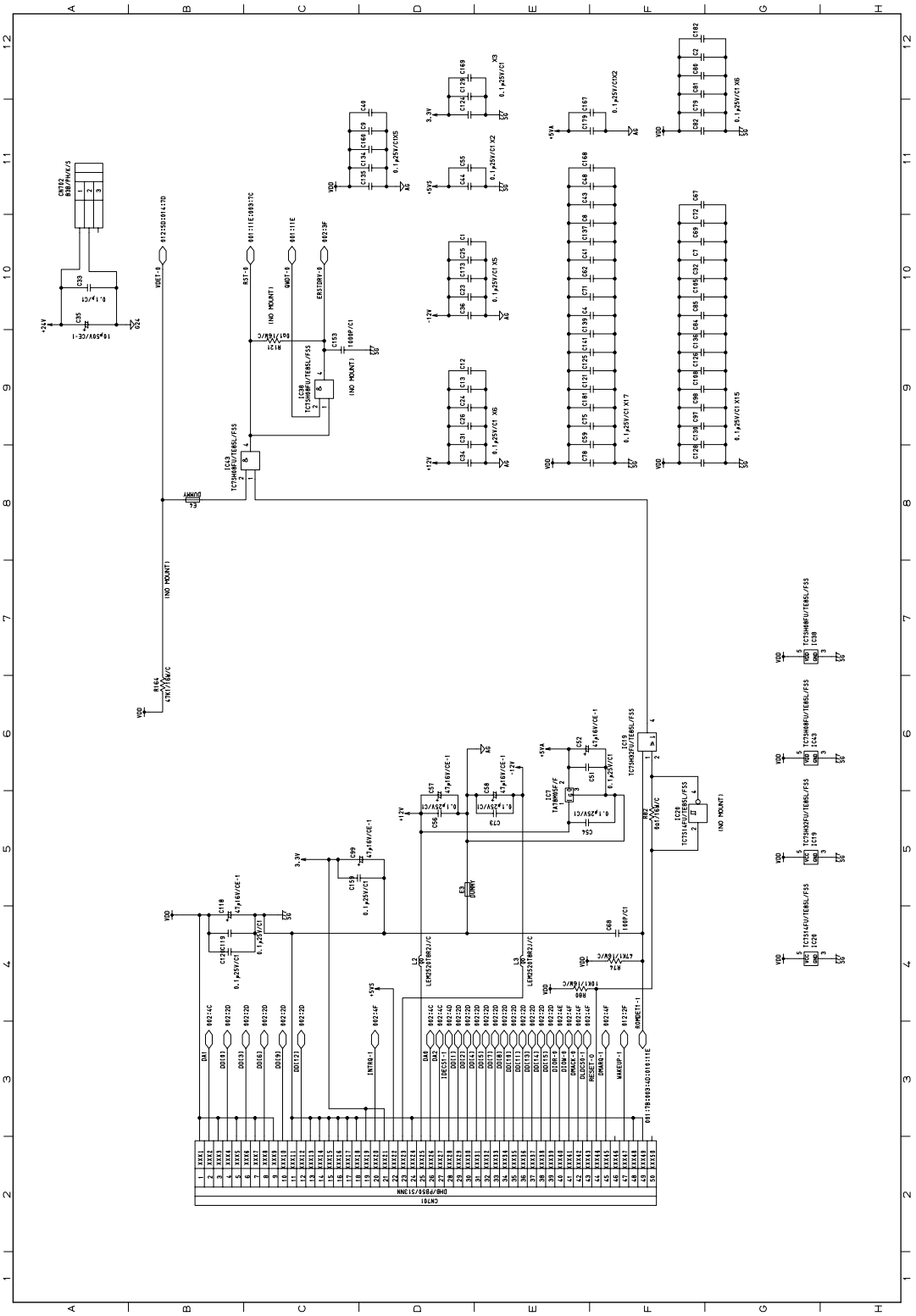

Fig. 3-130

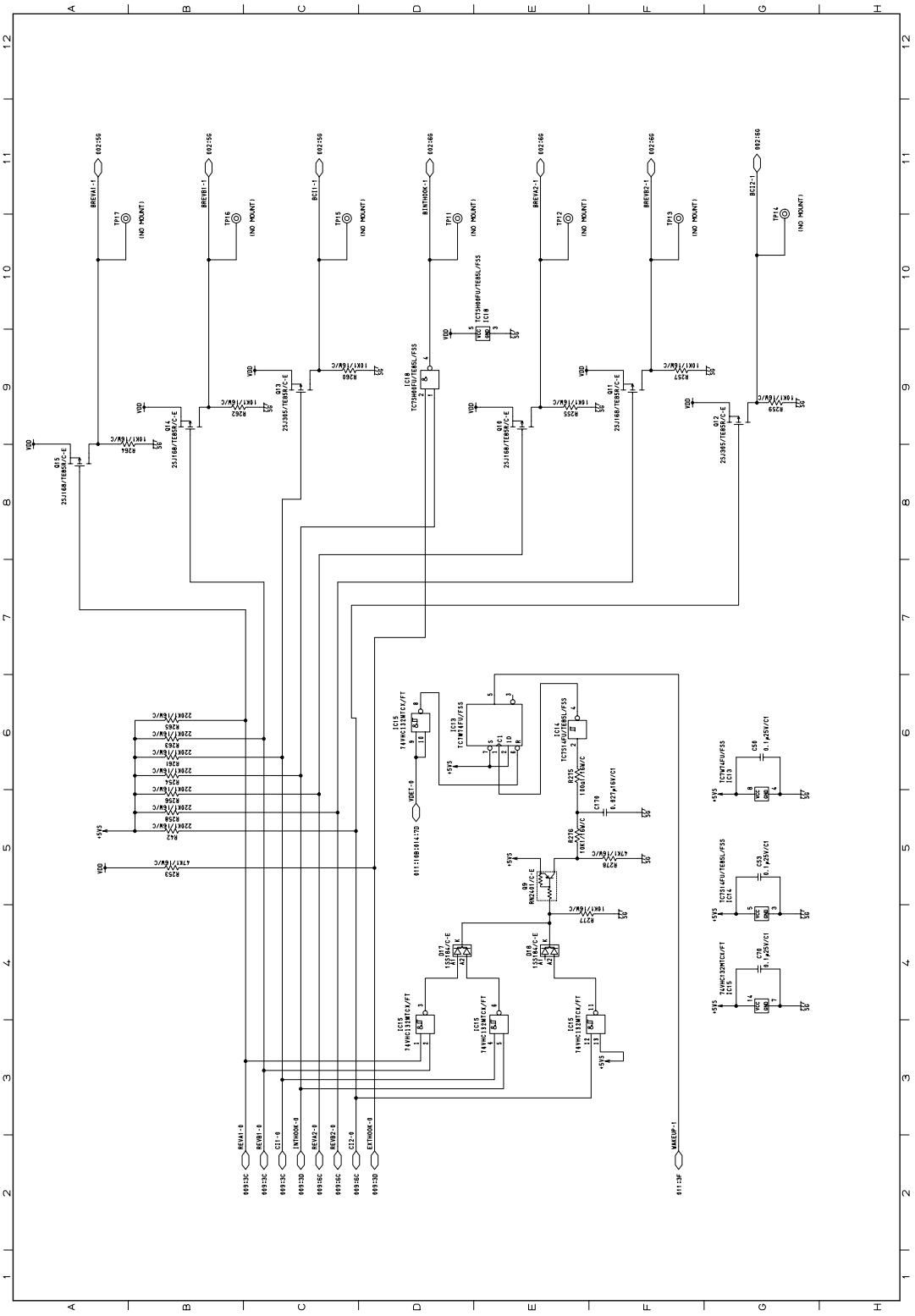

Fig. 3-131

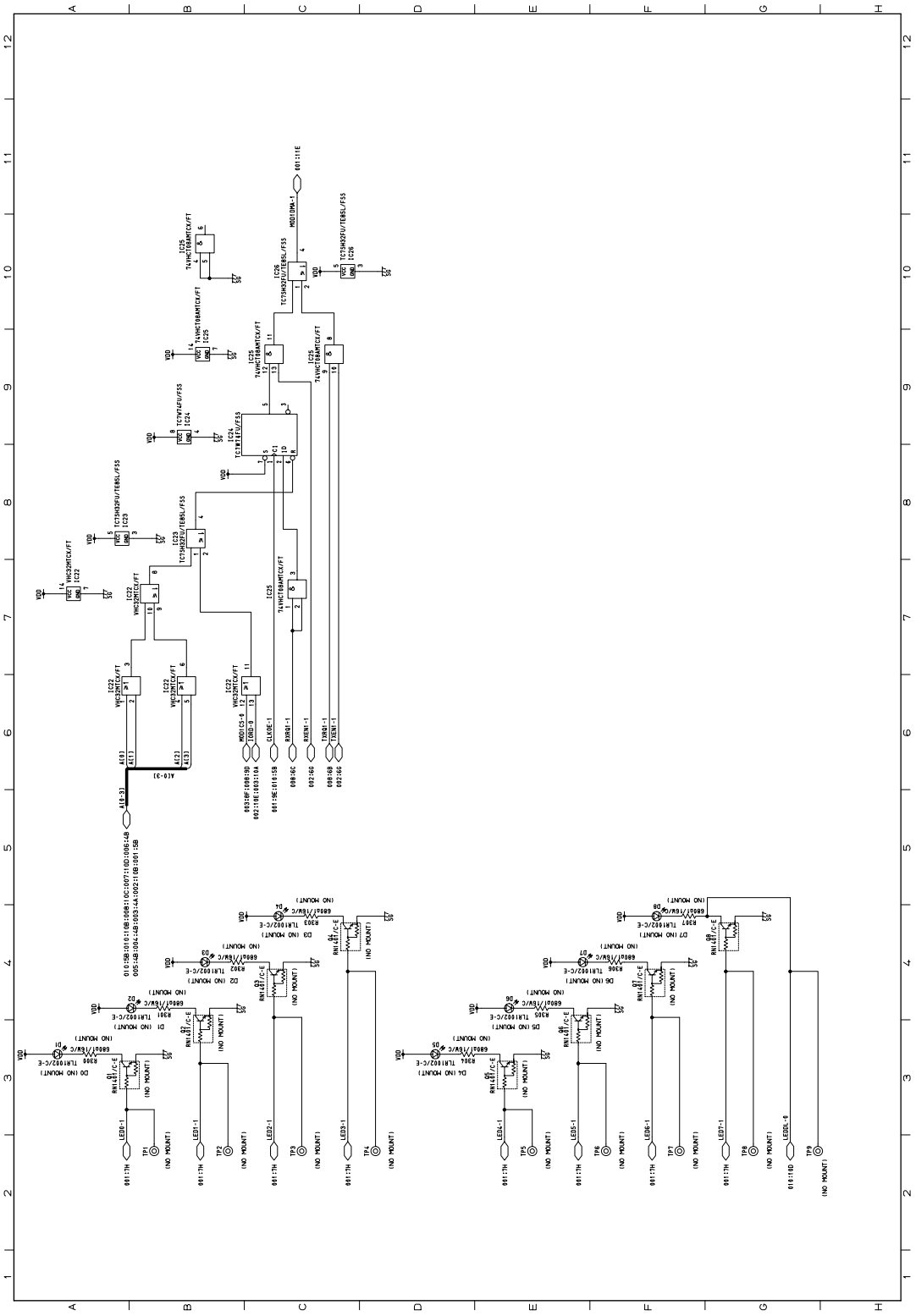

Fig. 3-132

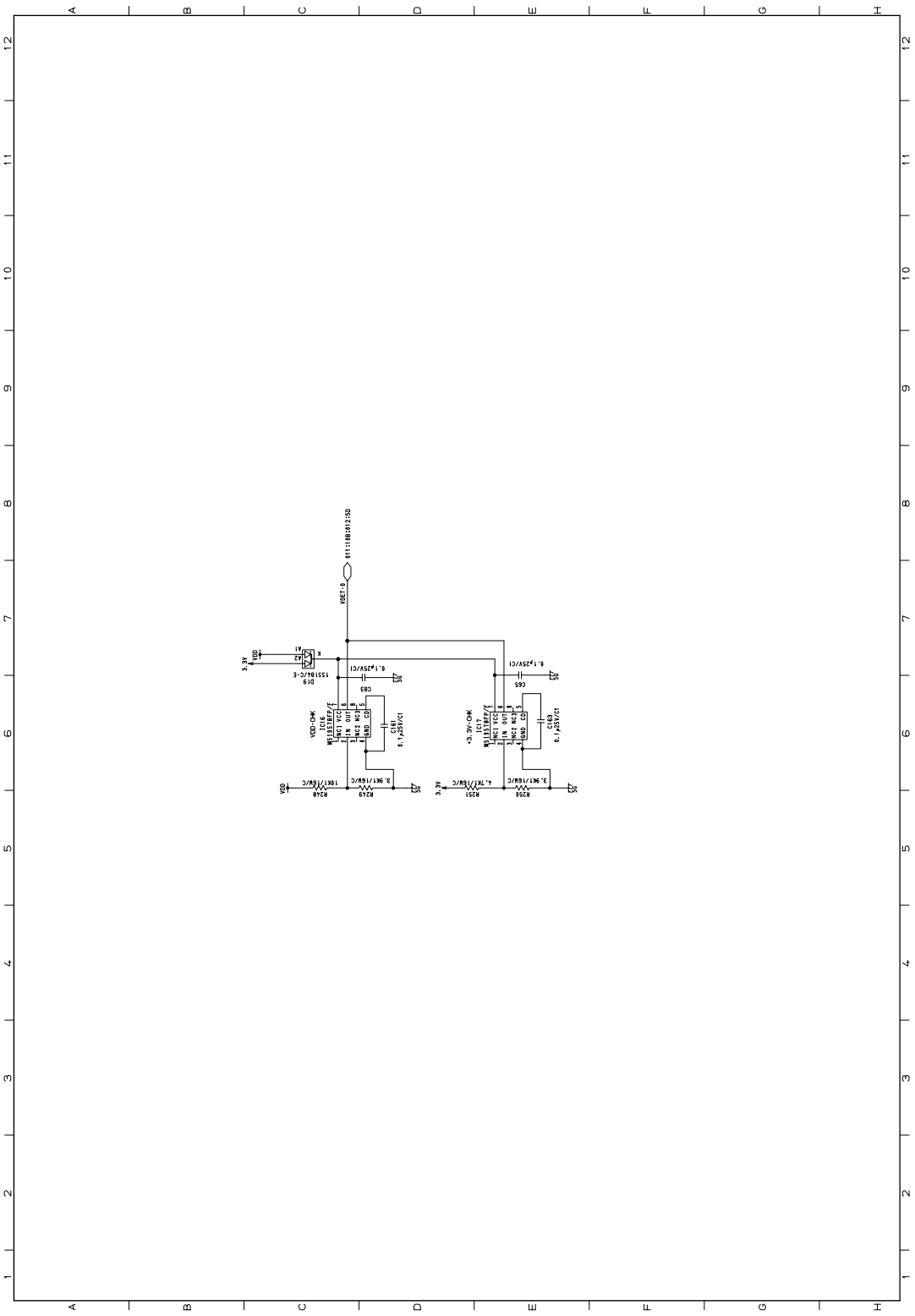

Fig. 3-133

3.12 Facsimile power supply circuit (FAX PWR board: GD-1210)

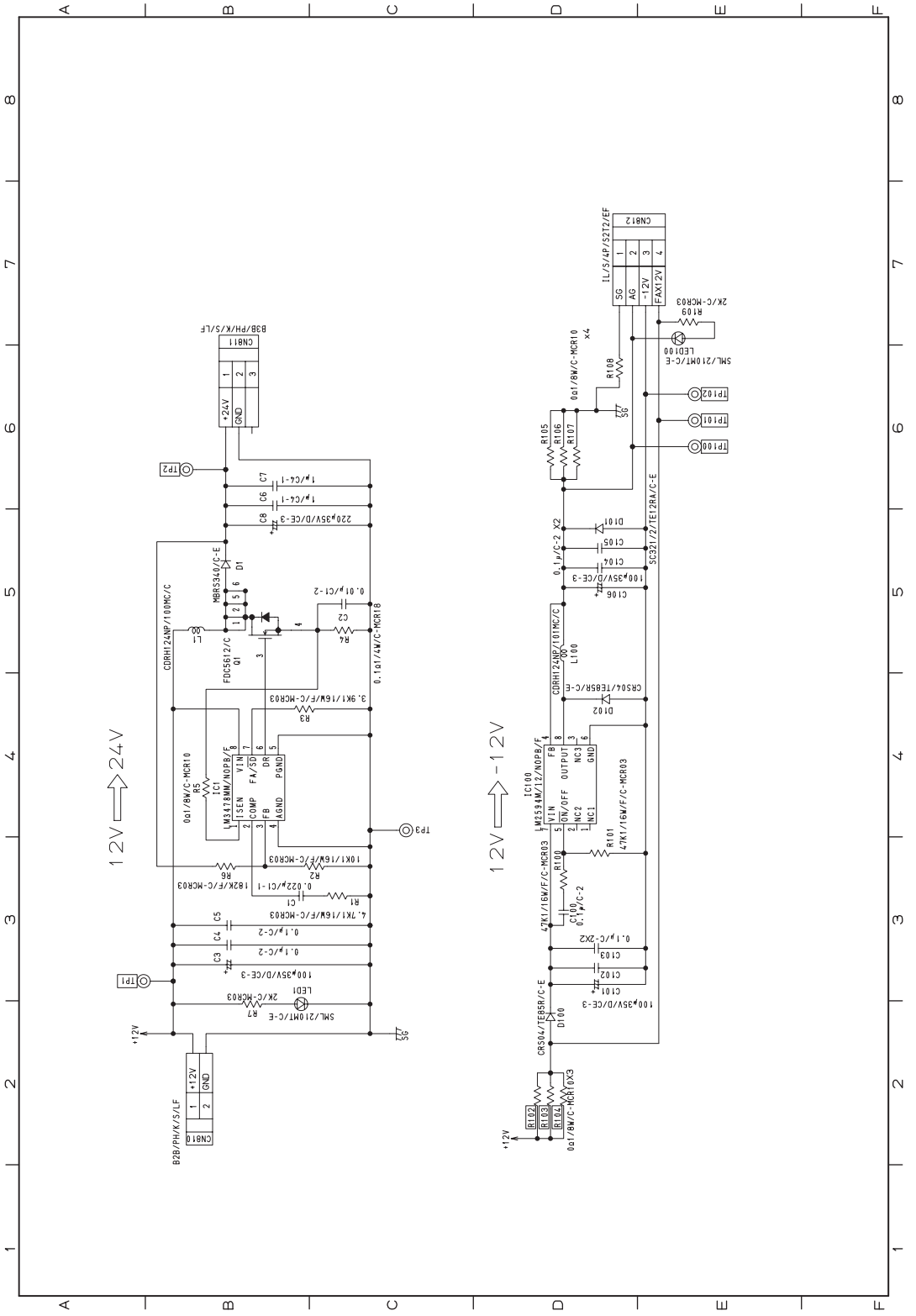

Fig. 3-134

3.13 Modem circuit (MDM board: GD-1160)

MDM board 1/4

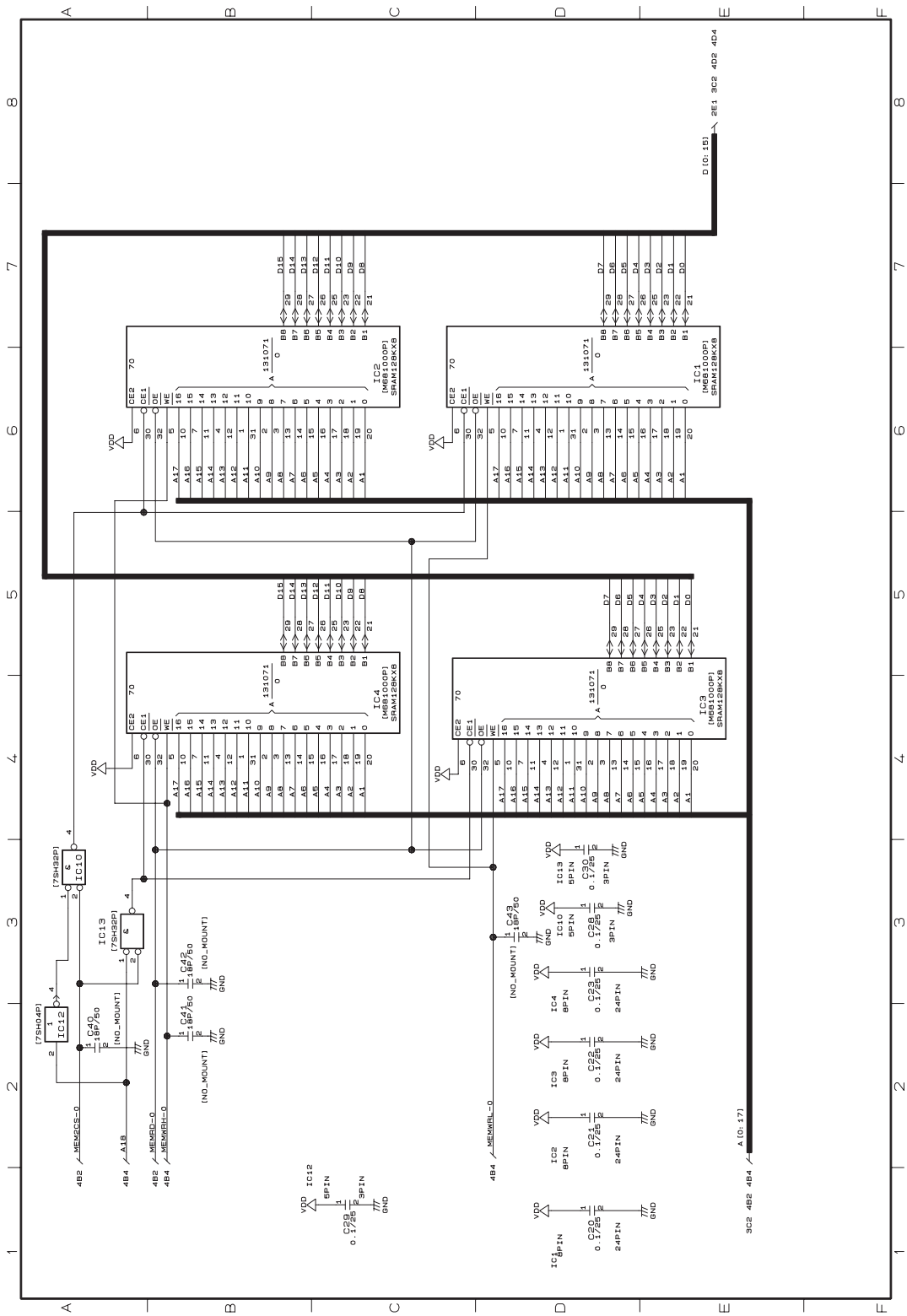

Fig. 3-135

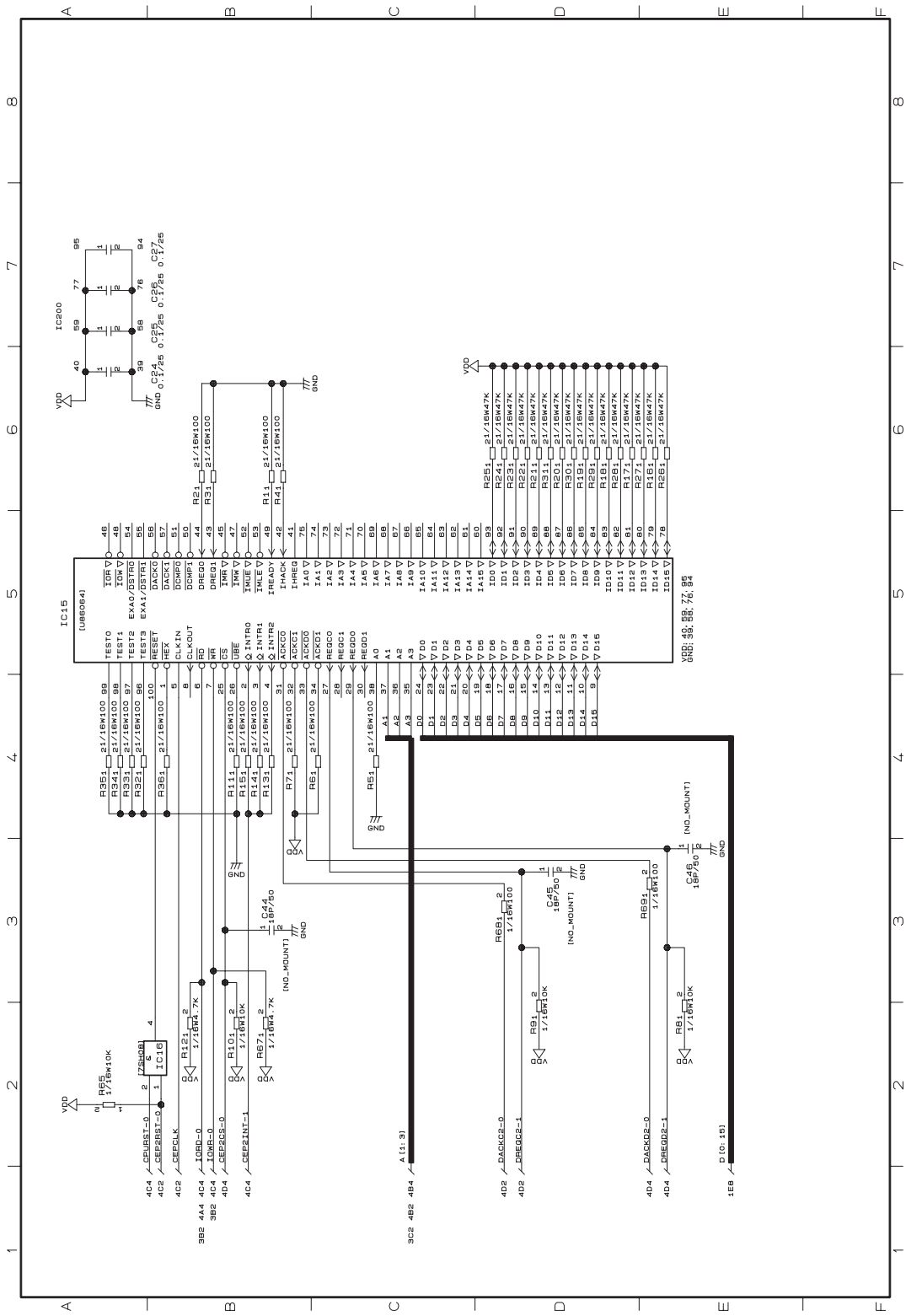

Fig. 3-136

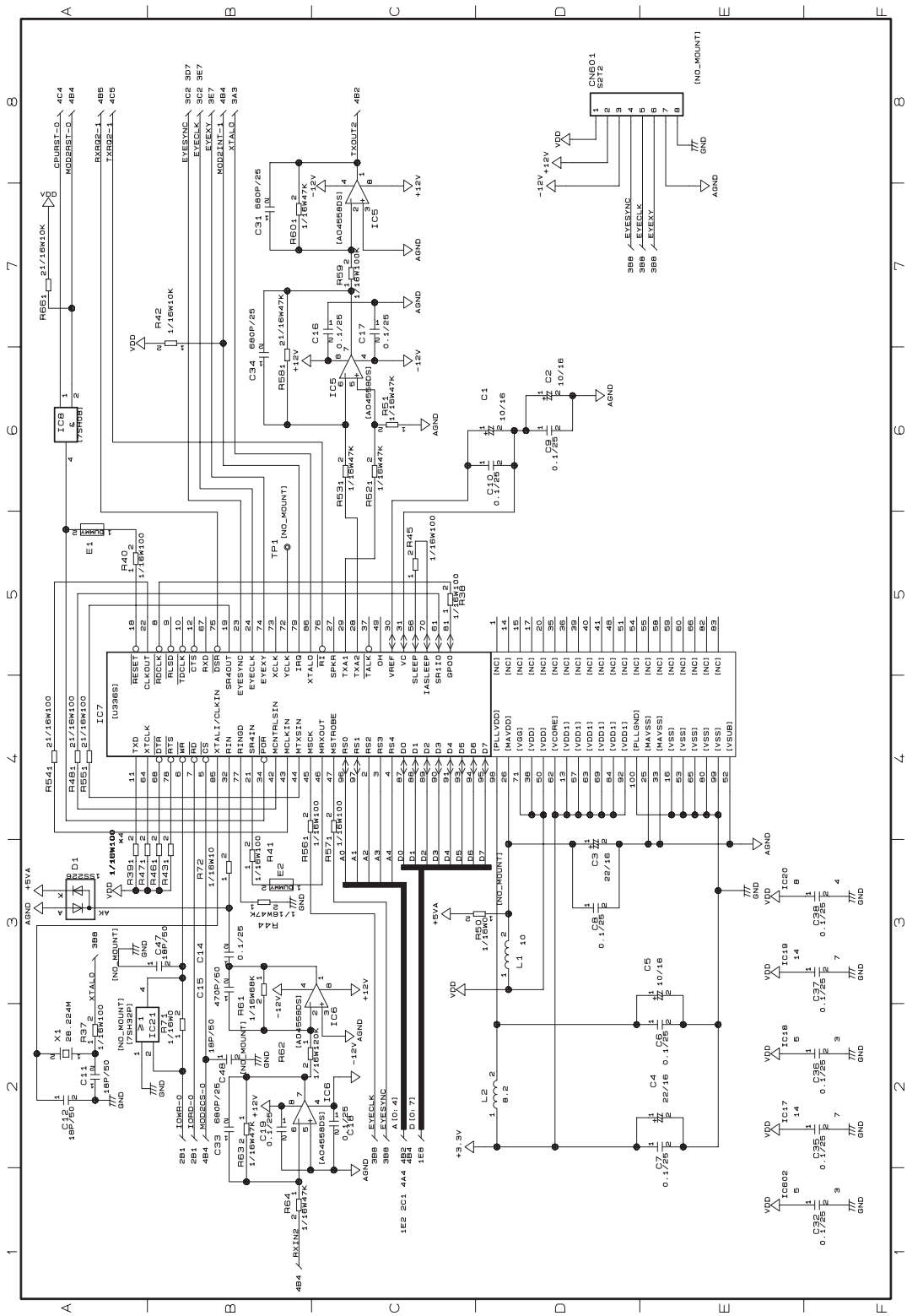

Fig. 3-137

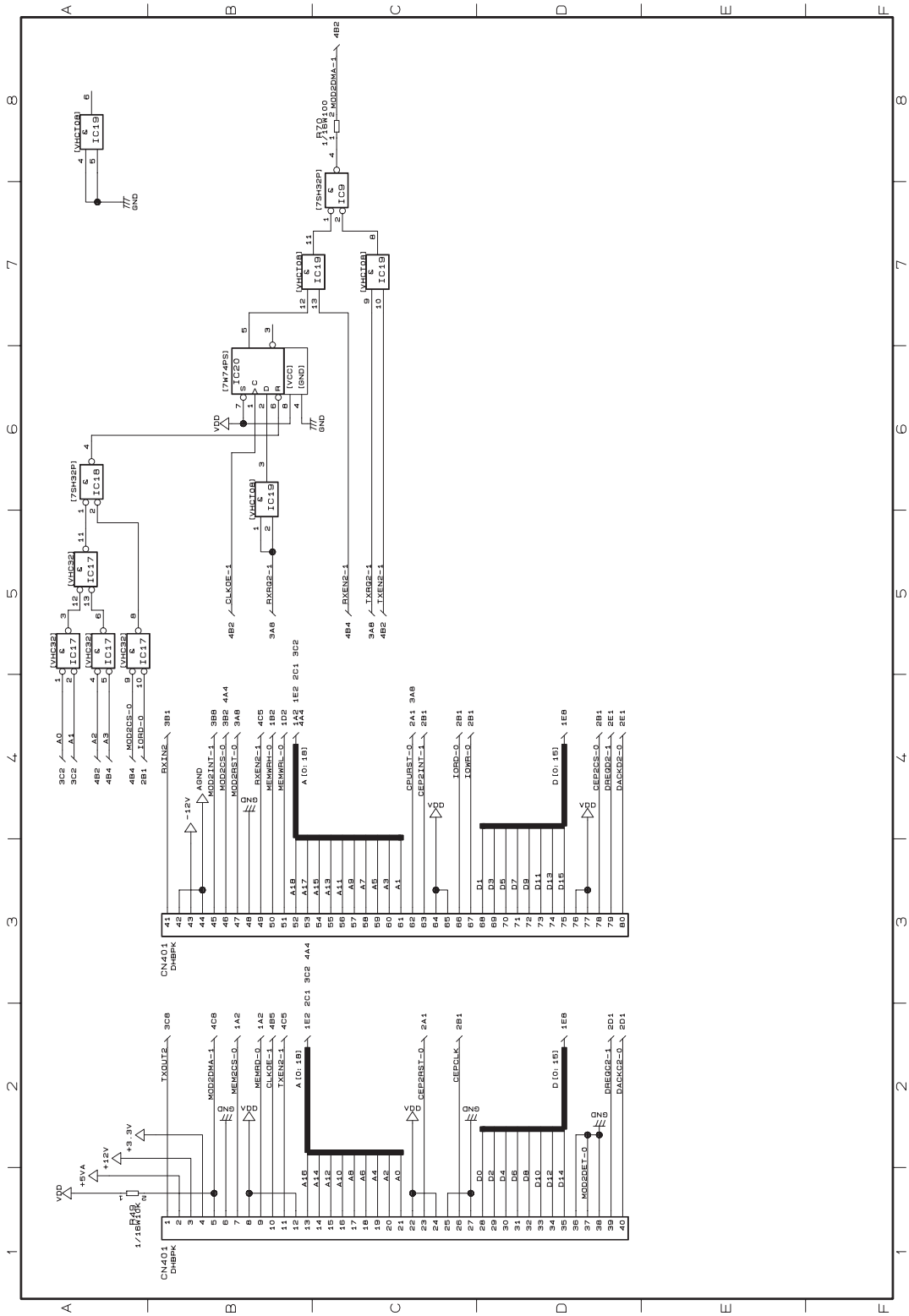

Fig. 3-138

3.14 Telephone line network control circuit (NCU board: GD-1210NA/TW / GD-1160NA/TW)

NCU board 1/2

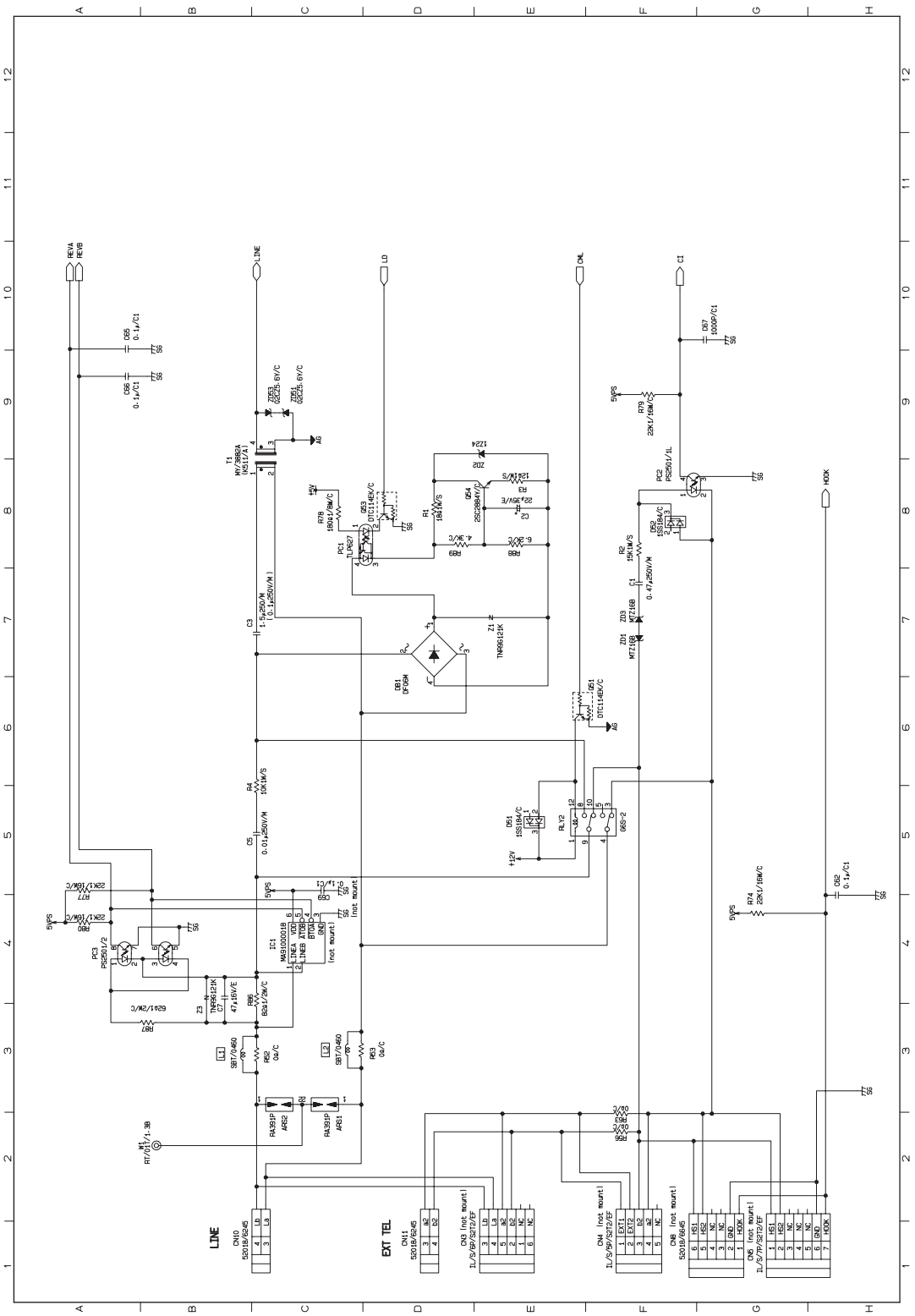

Fig. 3-139

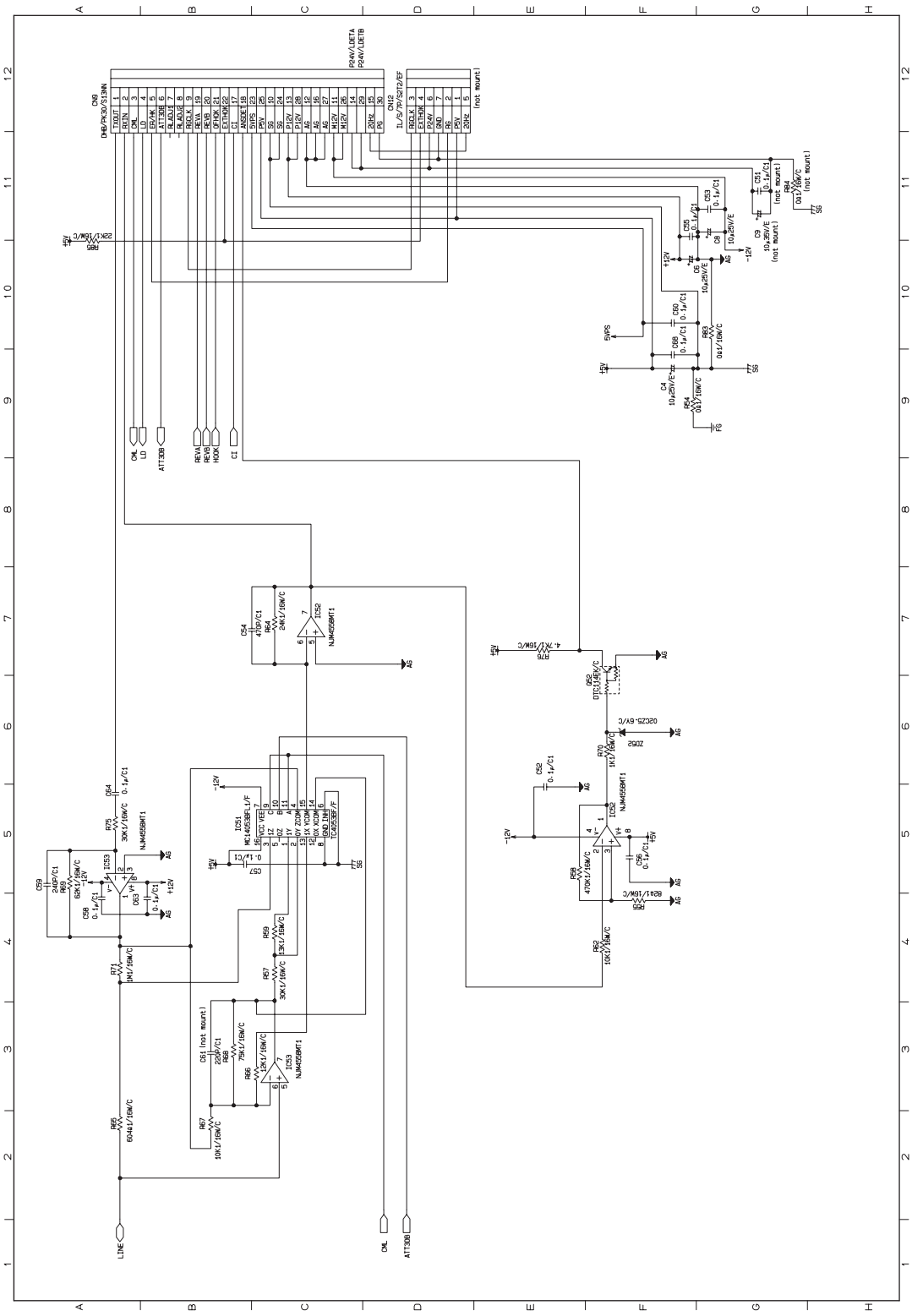

Fig. 3-140

3.15 Telephone line network control circuit (NCU board: GD-1210EU/AU/AS/C/KR / GD-1160EU-N/C)

NCU board 1/2

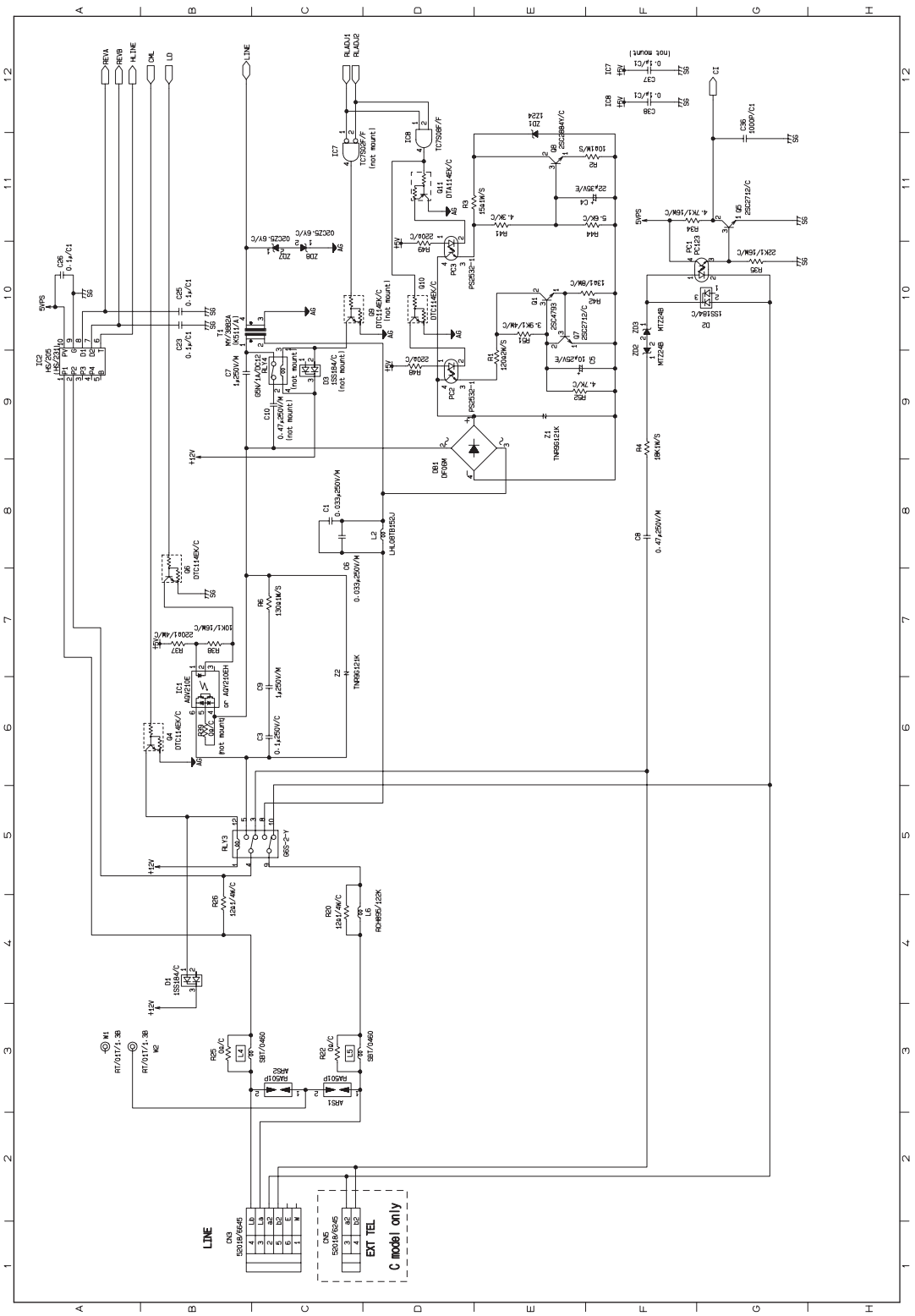

Fig. 3-141

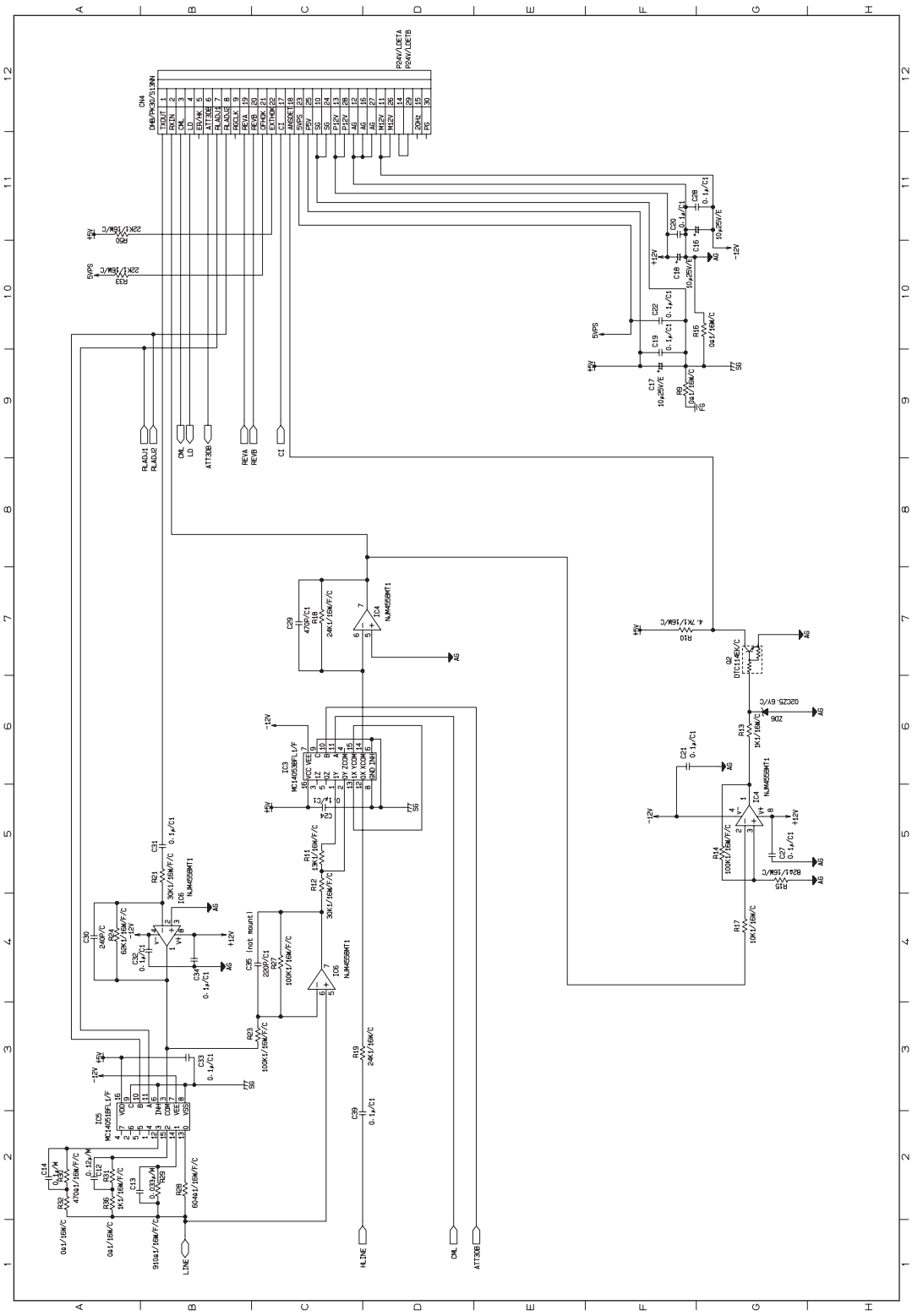

Fig. 3-142

TOSHIBA

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2-17-2, HIGASHIGOTANDA, SHINAGAWA-KU, TOKYO, 141-8664, JAPAN