BSI Service Note BSI Note

TOSHIBA TEC CORPORATION

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| BSI No.: | G09G058 |
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| Subject: | Circuit Diagram Information Release: e-STUDIO205L/255/305/355/455 |

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|---|---|
| Model: | e-STUDIO205L, e-STUDIO255, e-STUDIO305, e-STUDIO355, e-STUDIO455 |

| Category | Field Application | UNIT |
|---|---|---|
| C02 Other | F01 Others | U32 Service Document |

FactoryApplication: - Parts Availability in Tokyo:

CONTENT

"PC BOARD REPAIR MANUAL" for e-STUDIO205L/255/305/355/455 will not be issued; however, the circuit diagram information is released in this BSI instead.
Refer to the attached file for details.

## Attached File

1. Data File Name G09G058E.pdf
   Remark: Circuit Diagram

 - G09G058E.pdf

SLG CPU PORT LIST (IC10)

| Port | Bit | Signal | I/O | Function | Description | After reset | Initial (Firmware setting) | Remarks |
|---|---|---|---|---|---|---|---|---|
| Port 1 | 0 \| 7 | MDT8 \| MDT15 | I/O \| I/O | D8 \| D15 | Data bus: D8-D15 | - \| - | - \| - | |
| Port 6 | 0 | MAD16 | OUT | A16 | Address bus: A16 | 0 | 0 | |
| | 1 | MAD17 | OUT | A17 | Address bus: A17 | 0 | 0 | |
| | 2 | MAD18 | OUT | A18 | Address bus: A18 | 0 | 0 | |
| | 3 | NC | OUT | P63 | (Not used) | 1 | 1 | |
| | 4 | NC | OUT | P64 | (Not used) | 0 | 0 | |
| | 5 | NC | OUT | P65 | (Not used) | 1 | 1 | |
| | 6 | LMPON-0 | OUT | P66 | Exposure lamp ON | 1 | 1 | 0: Exposure lamp ON |
| | 7 | Spare | OUT | P67 | (Not used) E4 | 0 | 0 | |
| Port 7 | 1 | MWR-0A | OUT | WR | WRITE | 0 | 0 | |
| | 2 | NC | OUT | P72 | (Not used) | 0 | 0 | |
| | 3 | PNLWR | OUT | R/W | Scanner/control panel LEDs | 1 | 1 | 1: CPU -> SPN (output) |
| | 4 | Spare | OUT | P74 | (Not used) | 0 | 0 | |
| | 5 | Spare | OUT | P75 | (Not used) | 1 | 1 | |
| | 6 | STR-0 | OUT | P76 | STR judgment -- NG | 1 | 1 | 0: NG |
| | 7 | NC | OUT | P77 | (Not used: Reserved for WAIT) | 0 | 0 | |
| Port 8 | 0 | CS0-0 | OUT | CS0 | Decoding for ASIC, STR, control panel | 1 | 1 | |
| | 1 | CS1-0 | OUT | CS1 | Chip select signal for data RAM | 1 | 1 | |
| | 2 | CS2-0 | OUT | CS2 | FROM chip select signal for programming | 0 | 0 | |
| | 3 | CS3-0 | OUT | CS3 | FROM chip select signal for downloading | 1 | 1 | |
| | 4 | NC | OUT | CS4 | (Not used: Reserved for CS4) | 1 | 0 | |
| | 5 | WDTOUT-0 | OUT | WDTOUT | Watchdog timer - Timeout | 1 | 1 | 1: CPU - Normal 0: CPU - Runaway |
| | 6 | Spare | OUT | P86 | (Not used) E3 | 1 | 0 | |
| | 7 | SLEEP-1 | OUT | P87 | ASIC SLEEP setting | 0 | 0 | 1: ASIC PLL stop |
| Port 9 | 0 | DWNLD-0 | OUT | P90 | ROM download ON | 1 | 1 | 0: ROM download |
| | 1 | NC | OUT | P91 | (Not used) | 1 | 0 | |
| | 2 | LED-0 | OUT | P92 | LED ON at downloading | 0 | 0 | 1: LED ON |
| | 3 | FCNGF1-0 | OUT | P93 | Fan rotation - high speed (spare) | 1 | 1 | 01: High speed |
| | 4 | NC | OUT | P94 | (Not used) | 1 | 1 | 10: Low speed 11: Stopped |
| | 5 | APSON-1 | OUT | P95 | APS power ON | 0 | 1 | 1: APS power ON |
| | 6 | NC | OUT | P96 | (Not used) | 0 | 0 | |
| Port A | 0 | SRXD-1A | IN | RXD0 | SYS serial interface data input | 0 | - | |
| | 1 | STXD-1 | OUT | TXD0 | SYS serial interface data output | 0 | 0 | |
| | 2 | SCTS-0A | IN | CTS0 | SYS serial interface data - Scanner ready for receiving | 0 | - | 0: Ready for receiving |
| | 3 | DFRXD-0 | IN | RXD1 | DF serial interface data input | 0 | - | |
| | 4 | DFTXD-0 | OUT | TXD1 | DF serial interface data output | 0 | 0 | |
| | 5 | SRTS-0 | OUT | PA5 | SYS serial interface data - Scanner ready for sending | 1 | 1 | 0: Ready for sending |
| Port C | 0 | MOTMD1-0 | OUT | PC0 | Data 1 for motor | 0 | 0 | |
| | 1 | MOTMD2-0 | OUT | PC1 | Data 2 for motor | 0 | 0 | |
| | 2 | MOTMD3-0 | OUT | PC2 | Data 3 for motor | 0 | 0 | |
| | 3 | MOTDIR-0 | OUT | PC3 | Motor rotation (normal/reverse) | 0 | 0 | 0: Normal rotation 1: Reverse rotation |
| | 4 | MOTEN-0 | OUT | PC4 | Motor holding OFF | 0 | 1 | 0: Holding OFF (current shutoff) |
| | 5 | NC | OUT | PC5 | (Not used) | 0 | 0 | |
| Port D | 0 | SYSCNT-0A | IN | PD0 | For checking SYS board installation | 0 | - | 0: SYS board installed |
| | 1 | NC | OUT | PD1 | (Not used) | 0 | 0 | |
| | 2 | DFCNT-0 | IN | PD2 | DF connection | 0 | - | 0: DF installed |
| | 3 | DFAK-0 | OUT | PD3 | DF serial interface - Acknowledge to DF | 1 | 1 | 0: ACK |
| | 4 | DFRQ-0 | OUT | PD4 | DF serial interface - Send request to DF | 1 | 1 | Request signal (SLG -> DF) |
| | 5 | DFRAK-0 | IN | PD5 | DF serial interface - Acknowledge to SLG | 0 | - | 0: ACK |
| Port F | 0 | SG | OUT | PF0 | Pulldown | 0 | 0 | |
| | 1 | MOTCLK-1 | OUT | TA1OUT | Scan motor reference clock | 0 | 1 | |
| | 2 | HIT-1 | IN | INT1 | Hit from STR (interruption) | 0 | - | Rising edge |
| | 3 | EEMCS-1 | OUT | PF3 | EEPROM chip select | 0 | 0 | |
| | 4 | DFSCST-0 | IN | PF4 | DF scanning start | 1 | - | 1->0: DF scanning start (falling edge) |
| | 5 | EEMDTOUT-1 | OUT | PF5 | EEPROM data output | 0 | 0 | |
| | 6 | EEMDTIN-1 | IN | PF6 | EEPROM data input | 0 | - | |
| Port J | 0 | NC | OUT | PJ0 | (Not used) | 0 | 0 | |
| | 1 | NC | OUT | PJ1 | (Not used) | 0 | 0 | |
| | 2 | NC | OUT | PJ2 | (Not used) | 0 | 0 | |
| | 3 | NC | OUT | PJ3 | (Not used) | 0 | 0 | |
| | 4 | EEMCLK-1 | OUT | PJ4 | EEPROM clock input | 1 | 1 | |
| | 5 | NC | OUT | PJ5 | (Not used) | 0 | 0 | |
| | 6 | NC | OUT | PJ6 | (Not used) | 0 | 0 | |
| | 7 | NC | OUT | PJ7 | (Not used) | 0 | 0 | |
| Port K | 0 | SG | IN | PK0 | SG connection | 0 | - | |
| | 1 | SG | IN | PK1 | SG connection | 0 | - | |
| | 2 | DFRRQ-0 | IN | INT6 | DF serial interface - Send request to SLG | 0 | - | Request signal (DF -> SLG) |
| | 3 | SG | IN | PK3 | SG connection | 0 | - | |
| | 4 | SG | IN | PK4 | SG connection | 0 | - | |
| | 5 | SG | IN | PK5 | SG connection | 0 | - | |
| | 6 | FANON-0 | IN | PK6 | Fan connection check signal (spare) | 0 | - | |
| | 7 | NC | IN | PK7 | (Not used: Reserved for NTB) | 0 | - | |
| Port L | 0 | DBG0 | OUT | PL0 | | 0 | - | |
| | 1 | DBG1 | OUT | PL1 | | 0 | - | |
| | 2 | DBG2 | OUT | PL2 | For debugging | 0 | - | |
| | 3 | DBG3 | OUT | PL3 | | 0 | - | |
| | 4 | DBG4 | OUT | PL4 | | 0 | - | |
| | 5 | DBG5 | OUT | PL5 | | 0 | - | |
| | 6 | DBG6 | OUT | PL6 | | 0 | - | |
| | 7 | DBG7 | OUT | PL7 | | 0 | - | |
| Port M | 0 | HOME-1 | IN | PM0 | Home position sensor input | 0 | - | 1: Carriage home position |
| | 1 | 24VCHK | IN | AN1 | +24V voltage check | 0 | - | Threshold - 200/255 or above |
| | 2 | PLTN-1 | IN | PM2 | Platen cover SW input | 0 | - | 0: Platen cover closed (same as BP) |
| | 3 | APS1-0 | IN | PM3 | APS 1 input | 0 | - | |
| | 4 | APS2-0 | IN | PM4 | APS 2 input | 0 | - | 0: Original present |
| | 5 | APS3-0 | IN | PM5 | APS 3 input | 0 | - | 1: No original |
| | 6 | APSC-0 | IN | PM6 | APS center input | 0 | - | |
| | 7 | APSR-0 | IN | PM7 | APS rear input | 0 | - | |
| Port N | 0 | Spare | IN | PN0 | (Not used) E6 | 0 | - | |
| | 1 | PNCNT-0 | IN | PN1 | Scanner-control panel connection | 1 | - | 0: Control panel installed |
| | 2 | ROMCNT-0 | IN | PN2 | ROM board installation | 1 | - | 0: ROM board installed |
| | 3 | Spare | IN | PN3 | (Not used) E5 | 0 | - | |

LGC CPU PORT LIST (IC33)

| Port | Bit | Signal | I/O | Description | Initial | Remarks |
|---|---|---|---|---|---|---|
| Port1 | 0-7 | D[8]-[15] | I/O | CPU data bus (8-15) | 1 | Used for CPU data bus |
| Port6 | 0-7 | A[16]-A[23] | OUT | CPU address bus (16-23) | 1 | Used for CPU address bus |
| Port 7 | 1 | WR-0 | OUT | Write signal for 8-bit bus IC | 1 | 0: Write (used for WRLL) |
| | 2 | Not used | OUT | - | 1 | - |
| | 3 | RW-0 | OUT | Read/write signal (read/write bus | 1 | 0: Write enabled, 1: Read enabled (used for R/W) |
| | 4 | SRWR-0 | OUT | Write signal for 1-6 bit bus IC | 1 | 0: Write (used for SRWR) |
| | 5 | SRLLB-0 | OUT | SRAM 0-7 data enable | 1 | 0: 0-7 data access enabled (used for SRLLB) |
| | 6 | SRLUB-0 | OUT | SRAM 8-15 data enable | 1 | 0: 8-15 data access enabled (used for SRLUB) |
| | 7 | WAIT-0 | IN | Wait control signal (external control input signal) | 1 | 0: Wait signal inserted (used for WAIT) |
| Port 8 | 0 | EMECS-0 | OUT | ASIC CS signal | 1 | 0: ASIC enabled (used for CS) |
| | 1 | - | OUT | Not used | 1 | Not used |
| | 2 | CS2-0 | OUT | FROMCS signal (Switching is enabled at ASIC since the signal is transmitted via ASIC.) | 1 | 0: FROM enabled (used for CS) |
| | 3 | LLGCD/LEN-0 | OUT | CS output enable signal at downloading | 1 | 0: CS output enabled |
| | 4 | WDE-0 | OUT | Watchdog timer enable signal | 1 | 0: Watchdog timer disabled (3.3V SW OFF) |
| | 5 | WDT-0 | OUT | Watchdog timer timeout signal | 1 | 0: Watchdog timer timeout (used for WDT) |
| | 6 | VCMFNL-0 | OUT | Suction fan (low speed) ON signal | 1 | 0: Suction fan (low speed) ON (This signal will not be ON with bit-7) |
| | 7 | VCMFNH-0 | OUT | Suction fan (high speed) ON signal | 1 | 0: Suction fan (low speed) ON (This signal will not be ON with bit-6) |
| Port 9 | 0 | VSYNCEN-0 | OUT | VSYNC output enable signal | 1 | 0: VSYNC output enabled (at the time of the test printing) |
| | 1 | LDRDY-1 | OUT | Laser output enable signal | 1 | 0: Laser output stopped (Stopped when ASIC HDEN is synchronized) |
| | 2 | LE-0 | OUT | Laser enable signal | 1 | 0: Laser process enabled (ASIC internal process enabled) |
| | 3 | LDOFF-0 | OUT | Laser forcible OFF signal | 1 | 0: Laser process stopped (ASIC internal process stopped) |
| | 4 | LDON-0 | OUT | Laser forcible ON signal | 1 | 0: Laser forcible ON |
| | 5 | MVDEN-0 | OUT | Printer (vertical scanning direction) | 1 | 0: Printer enabled (vertical scanning direction) |
| | 6 | SDCLK-1 | OUT | SDCLK output (system clock: 17 MHz) | 1 | (Used for SDCLK) |
| Port A | 0 | TSIZE0-1 | OUT | Paper size - 0 (for counter) | 1 | Used for the option counter |
| | 1 | TSIZE1-1 | OUT | Paper size - 1 (for counter) | 1 | Used for the option counter |
| | 2 | TSIZE2-1 | OUT | Paper size - 2 (for counter) | 1 | Used for the option counter |
| | 3 | TSIZE3-1 | OUT | Paper size - 3 (for counter) | 1 | Used for the option counter |
| | 4 | FLCTR-0 | OUT | Counter for full color (not used) | 1 | 0: Counted up during the full color mode |
| | 5 | ADUCTR-0 | OUT | Back side counter signal | 1 | 0: Back side print job is counted up |
| Port C | 0 | DDIDI1-1 | OUT | Laser output forcible OFF signal | 1 | 0: Laser forcible OFF canceled (stopped at the last phase of ASIC) |
| | 1 | BUSEN-1 | OUT | CPU bus switching enable signal | 1 | 0: Bus switching disabled |
| | 2 | MTREN-0 | OUT | Pulse motor ON enable signal | 1 | 0: Motor ON enabled |
| | 3 | SDA | I/O | EEPROM data signal | 1 | |
| | 4 | SCL | OUT | EEPROM clock signal | 1 | |
| | 5 | WP-1 | OUT | EEPROM write-protect signal | 1 | 0: EEPROM writing enabled |
| Port D | 0 | POMON-0 | OUT | Polygonal motor ON signal | 1 | 0: Polygonal motor ON |
| | 1 | PSFANONL-0 | OUT | Power supply fan (low speed) ON signal | 1 | 0: Power supply fan (low speed) ON (This signal will not ON with bit-2) |
| | 2 | PSFANONH-0 | OUT | Power supply fan (high speed) ON signal | 1 | 0: Power supply fan (high speed) ON (This signal will not ON with bit-1) |
| | 3 | BTMFED-1 | IN | Lower transport sensor paper | 0 | 1: Sensor detected paper |
| | 4 | UPFED-1 | IN | Upper transport sensor paper | 0 | 1: Sensor detected paper |
| | 5 | FCOVSW-1 | IN | Front cover opening/closing signal | 0 | 1: Front cover opened |
| Port F | 0 | STINT-1 | IN | SYS send interrupt signal | 0 | 1: SYS send interrupted (used for INT) |
| | 1 | DEVCNT-0 | IN | Developer unit installation signal | 1 | 0: Developer unit installed |
| | 2 | CMINT-1 | IN | SYS receive interrupt signal | 0 | 1: SYS receive interrupted (used for INT) |
| | 3 | ERSLP-0 | OUT | Discharge LED ON signal | 1 | 0: Discharge LED ON signal |
| | 4 | PWRDN-1 | IN | Output OFF signal from power | 0 | 1: Power supply output OFF (used for INT) |
| | 5 | RLYOFF-0 | OUT | Relay forcible OFF signal for HTR | 1 | 0: Relay forcible OFF |
| | 6 | MINT1-1 | IN | Motor-1 interrupt signal | 0 | 1: Motor-1 interrupt signal (used for INT) |
| Port J | 0 | HVTM-0 | OUT | HVT main charger grid ON signal | 1 | 0: Main charger bias ON |
| | 1 | HVTT-0 | OUT | HVT transfer ON signal | 1 | 0: Transfer bias ON |
| | 2 | HVTAC-0 | OUT | HVT developer bias (AC) ON | 1 | 0: Developer bias ON |
| | 3 | HVTGB-0 | OUT | HVT guide bias ON signal | 1 | 0: Guide bias ON |
| | 4 | HVTTCHG-0 | OUT | HVT transfer positive/negative | 1 | 0: Positive voltage output, 1: Negative voltage output |
| | 5 | FUSCUT-0 | OUT | Fuser unit initial fuse cutoff ON | 1 | 0: Cutoff ON |
| | 6 | PUFANH-0 | OUT | PU-FAN (high speed) ON signal | 1 | 0: PU-FAN (high speed) ON (This signal will not be ON with bit-7) |
| | 7 | PUFANL-0 | OUT | PU-FAN (low speed) ON signal | 1 | 0: PU-FAN (low speed) ON (This signal will not be ON with bit-6) |

| Port | Bit | Signal | I/O | Description | Initial | Remarks |
|---|---|---|---|---|---|---|
| Port K | 0 | MINT2-1 | IN | Motor-2 interrupt signal | 0 | 1: Motor-2 interrupt signal (used for INT) |
| | 1 | MINT3-1 | IN | Motor-3 interrupt signal | 0 | 1: Motor-3 interrupt signal (used for INT) |
| | 2 | PSTPSW-1 | IN | Registration sensor paper present signal | 0 | 1: Registration sensor detected paper |
| | 3 | 24VCHK-0 | IN | 24V OFF (cover open) signal | 1 | 0: 24V OFF (cover opened) |
| | 4 | CSTSIDESW-1 | IN | Drawer side cover opening/closing signal | 0 | 1: Drawer side cover opened |
| | 5 | IPCSW-0 | IN | IPC board connection signal | 1 | 0: IPC board connected |
| | 6 | FMBSY-0 | IN | FROM busy signal | 1 | 0: FROM busy signal |
| | 7 | SDCSW-1 | IN | Side cover opening/closing signal | 0 | 1: Side cover opened |
| Port L | 0 | CSTCTR-0 | OUT | External counter signal | 1 | 0: External counter countup |
| | 1 | EXTCTR-0 | OUT | Exit counter signal | 1 | 0: Count up when paper is exited |
| | 2 | MCRUN-0 | OUT | Machine operation signal | 1 | 0: Machine is operating |
| | 3 | CTRON-0 | OUT | Total counter signal | 1 | 0: Total counter countup |
| | 4 | KCTRO-0 | OUT | Key counter signal | 1 | 0: Key counter countup |
| | 5 | LEDON-0 | OUT | LED ON signal for debugging (not used) | 1 | 0: LED OFF |
| | 6 | YOBIFANH-0 | OUT | Spare fan (high speed) ON signal (not used) | 1 | 0: Spare fan (high speed) ON (This signal will not be ON with bit-7) |
| | 7 | YOBIFANL-0 | OUT | Spare fan (low speed) ON signal (not used) | 1 | 0: Spare fan (low speed) ON (This signal will not be ON with bit-6). |
| Port M | 0 | MTH-1 | IN | Center thermistor voltage input | - | |
| | 1 | STH-1 | IN | Side thermistor voltage input | - | |
| | 2 | ETH-1 | IN | Edge thermistor voltage input | - | |
| | 3 | HMS-1 | IN | Temperature/humidity sensor - | - | |
| | 4 | TEMP-1 | IN | Temperature/humidity sensor - | - | |
| | 5 | DRTH-1 | IN | Drum thermistor voltage input (analog) | - | |
| | 6 | ATS-1 | IN | Auto-toner sensor voltage input (analog) | - | |
| | 7 | KISYU6 | IN | - | 1 | - |
| Port N | 0 | EWSCN-0 | IN | EWS relay board connection signal | 1 | 0: EWS relay board connected |
| | 1 | GCCTCP-1 | IN | Pixel counter match signal | 0 | 1: Pixel counter value matched |
| | 2 | HSYNCERR- | IN | HSYNC error signal | 0 | 1: HSYNC error |
| | 3 | PVDEN-0 | IN | Image data output (vertical scanning direction) sync signal | 1 | 0: Image data output (vertical scanning direction) synchronized |

LGC ASIC PORT LIST (IC22)

| Port | Bit | Signal | I/O | Description | Initial | Remarks |
|---|---|---|---|---|---|---|
| Port A | 0 | REVSW-1 | IN | Reverse sensor paper present signal | 0 | 1: Sensor detected paper (not used for e-STUDIO205L/305) |
| | 1 | FUSCNT-1 | IN | Fuser unit installation signal | 1 | 0: Fuser unit not installed |
| | 2 | LCCNT-0 | IN | LCF connection signal | 1 | 0: LCF connected |
| | 3 | KCTRC-0 | IN | Optional counter connection signal | 1 | 0: Optional counter connected |
| Port B | 0 | WR-P-0 | OUT | WR_P signal (WR signal for ASIC) | 1 | 0: Write enabled (used for WR_P) |
| | 1 | PULSARDIR-0 | OUT | CPU data bus switch signal for ASIC | 1 | 0: Data input enabled (used for BUSDIR) |
| | 2 | NVRAMBUSOE | OUT | CPU data bus enable signal (for NVRAM) | 1 | 0: Data output enabled (used for BUSEN) |
| | 3 | IPCBUSOE-0 | OUT | CPU data bus enable signal (for IPC) | 1 | 0: Data output enabled (used for BUSEN) |
| | 4 | RW-0 | IN | Read/write signal from CPU | 1 | 0: Write enabled (used for R/W input) |
| | 5 | MOTCNT-0 | IN | MOT board connection signal | 1 | 0: MOT board connected |
| | 6 | SFBEMP-1 | IN | Bypass tray paper present signal | 1 | 0: Paper present |
| | 7 | KISYU4 | IN | - | | - |
| Port C | 0 | FROMCS-0 | OUT | CS signal for FROM (automatic switching on D/L) | 1 | 0: FROM enabled (used for CS) |
| | 1 | D/LROMCS-0 | OUT | CS signal for ROM (output only on D/L) | 1 | 0: D/L ROM enabled (used for CS) |
| | 2 | CSRAM-0 | OUT | CS for SRAM | 1 | 0: SRAM enabled (used for CS) |
| | 3 | CSNVRAM-0 | OUT | CS for NVRAM | 1 | 0: NVRAM enabled (used for CS) |
| | 4 | CSIPC-0 | OUT | CS for IPC | 1 | 0: IPC enabled (used for CS) |
| | 5 | CLRGC-0 | OUT | Lower drawer feed clutch ON signal | 1 | 0: Lower drawer feed clutch ON |
| | 6 | OFFSET2 | OUT | OFFSET signal-2 | 1 | *e-STUDIO205L/255/305 (OCT motor) |
| | 7 | OFFSET1 | OUT | OFFSET signal-1 | 1 | OFFSET1 OFFSET2 Status |
| Port D | 0 | MINT3-1 | OUT | Motor-3 interrupt output | 0 | 1: Motor-3 interrupt output (used for interruption) |
| | 1 | ADUCL-0 | OUT | ADU clutch ON signal | 1 | 0: ADU clutch ON |
| | 2 | REVSOL-0 | OUT | Reverse solenoid ON signal | 1 | 0: Reverse solenoid ON |
| | 3 | HVCLK-1 | OUT | HVT developer bias (AC) clock output | 1 | (Used for timer output) |
| | 4 | MMTRCK-1 | OUT | Main motor clock output | 1 | (Used for timer output) |
| | 5 | POMCK-1 | OUT | Polygonal motor clock output | 1 | (Used for timer output) |
| | 6 | PFPCK-1 | OUT | PFP motor clock output | 1 | (Used for timer output) |
| | 7 | CURGC-0 | OUT | Upper drawer feed clutch ON signal | 1 | 0: Upper drawer feed clutch ON |
| Port E | 0 | EEPROMCS | OUT | EEPROM CS signal (for toner) | 1 | 1: EEPROM for toner enabled (used for EEPROM) |
| | 1 | EEPROMCK | OUT | EEPROM clock signal (common) | 1 | (Used for EEPROM) |
| | 2 | EEPROMDI | IN | EEPROM data input signal (common) | 1 | (Used for EEPROM) |
| | 3 | EEPROMDO | OUT | EEPROM data output signal (common) | 1 | (Used for EEPROM) |
| | 4 | EEPROMCS1 | OUT | EEPROM CS signal (for developer) | 1 | 1: EEPROM for developer unit enabled (used for EEPROM) |
| | 5 | DACLD-1 | OUT | DAC data load signal | 1 | 1: DAC data load (used for DAC) |
| | 6 | DACCK-1 | OUT | DAC clock signal | 1 | (Used for DAC) |
| | 7 | DACDT-1 | OUT | DAC data signal | 1 | (Used for DAC) |
| Port F | 0 | INOPTSOL-0 | OUT | Inner receiving tray unit solenoid ON signal | 1 | 0: Solenoid ON (control is changeable depending on an option installed) |
| | 1 | KISYU2 | IN | - | - | - |
| | 2 | KISYU1 | IN | - | - | - |
| | 3 | KISYU0 | IN | - | - | - |
| | 4 | Not used | IN | - | 1 | - |
| | 5 | HVSDWN-1 | IN | HVT leak signal | 1 | 0: HVT leaked |
| | 6 | MMTRPLL-0 | IN | Main motor PLL lock signal | 1 | 0: Main motor normal rotation |
| | 7 | POMPL-0 | IN | Polygonal motor PLL lock signal | 1 | 0: Polygonal motor normal rotation |
| Port G | 0 | - | IN | Not used (fixed at "1" from ASIC specification) | 1 | Fixed at "1" |
| | 1 | EXTSW-1 | IN | Exit sensor paper present signal | 1 | 0: Sensor detected paper |
| | 2 | SCSW-0 | OUT | Extension I/O switching signal | 1 | |
| | 3 | FUSCHK-0 | IN | Fuser unit initial detection signal | 0 | 1: Fuser unit initial detection - fuse already cut off |
| | 4 | CTRCNT2-0 | IN | Optional counter count enable signal | 1 | 0: Count enabled |
| | 5 | HTR1ON-0 | OUT | HTR1 ON signal | 1 | 0: HTR1 ON |
| | 6 | HTR2ON-0 | OUT | HTR2 ON signal | 1 | 0: HTR2 ON |
| | 7 | HTRASTON-0 | OUT | Sub-HTR ON signal | 1 | 0: Sub-HTR ON |
| Port H | 0 | SACK-0 | IN | SYS interface - SYS ACK signal | 1 | (Used for SYS IF) |
| | 1 | SBSY-0 | OUT | SYS interface - LGC BSY signal | 1 | (Used for SYS IF) |
| | 2 | SERR-0 | IN | SYS interface - SYS ERR signal | 1 | (Used for SYS IF) |
| | 3 | STS-0 | OUT | SYS interface - LGC STS signal | 1 | (Used for SYS IF) |
| | 4 | CACK-0 | OUT | SYS interface - LGC ACK signal | 1 | (Used for SYS IF) |
| | 5 | CBSY-0 | IN | SYS interface - SYS BSY signal | 1 | (Used for SYS IF) |
| | 6 | CERR-0 | OUT | SYS interface - LGC ERR signal | 1 | (Used for SYS IF) |
| | 7 | CMD-0 | IN | SYS interface - SYS CMD signal | 1 | (Used for SYS IF) |
| Port I | 0 | PIFDI[0] | I/O | PFP/LCF interface signal-0 | 1 | (Used for the option drawer IF) |
| | 1 | PIFDI[1] | I/O | PFP/LCF interface signal-1 | 1 | (Used for the option drawer IF) |
| | 2 | PIFDI[2] | I/O | PFP/LCF interface signal-2 | 1 | (Used for the option drawer IF) |
| | 3 | PIFDI[3] | I/O | PFP/LCF interface signal-3 | 1 | (Used for the option drawer IF) |
| | 4 | PIFDI[4] | I/O | PFP/LCF interface signal-4 | 1 | (Used for the option drawer IF) |
| | 5 | PIFDI[5] | I/O | PFP/LCF interface signal-5 | 1 | (Used for the option drawer IF) |
| | 6 | PIFDI[6] | I/O | PFP/LCF interface signal-6 | 1 | (Used for the option drawer IF) |
| | 7 | PIFDI[7] | I/O | PFP/LCF interface signal-7 | 1 | (Used for the option drawer IF) |

| Port | Bit | Signal | I/O | Description | Initial | Remarks |
|---|---|---|---|---|---|---|
| Port | 0 | PIFDI[8] | I/O | PF/LCF interface signal-8 | 1 | (Used for the option drawer IF) |
| J | 1 | PIFDI[9] | I/O | PFP/LCF interface signal-9 | 1 | (Used for the option drawer IF) |
| | 2 | PIFDI[10] | I/O | PFP/LCF interface signal-10 | 1 | (Used for the option drawer IF) |
| | 3 | PIFDI[11] | I/O | PFP/LCF interface signal-11 | 1 | (Used for the option drawer IF) |
| | 4 | SCSWB-0 | OUT | PFP/LCF interface switching signal-B | 1 | (Used for the option drawer IF) |
| | 5 | SCSWC-0 | OUT | PFP/LCF interface switching signal-C | 1 | (Used for the option drawer IF) |
| | 6 | CLKB-1 | OUT | PFP/LCF interface clock signal-B | 1 | (Used for the option drawer IF) |
| | 7 | CLKC-1 | OUT | PFP/LCF interface clock signal-C | 1 | (Used for the option drawer IF) |
| Port | 0 | CMINT-1 | OUT | SYS interface CMD interrupt signal | 0 | 1: CMD interrupt output (used for interruption) |
| K | 1 | STINT-1 | OUT | SYS interface STS interrupt signal | 0 | 1: STS interrupt output (used for interruption) |
| | 2 | MINT1-1 | OUT | Motor-1 interrupt signal | 0 | 1: Motor-1 interrupt output (used for interruption) |
| | 3 | MINT2-1 | OUT | Motor-2 interrupt signal | 0 | 1: Motor-2 interrupt output (used for interruption) |
| | 4 | 1STCLH-0 | OUT | 1st transport clutch (high speed) ON signal | 1 | 0: Clutch ON (This signal will not be ON with bit-5) |
| | 5 | 1STCLL-0 | OUT | 1st transport clutch (low speed) ON signal | 1 | 0: Clutch ON (This signal will not be ON with bit-4) |
| | 6 | D/LROMCS2-0 | OUT | CS2 signal for D/L ROM | 1 | 0: D/L PLD enabled (used for CS) |
| | 7 | CSPLS-0 | OUT | ASIC CS signal | 1 | 0: ASIC enabled (used for CS) |
| Port | 0 | - | OUT | ASIC sequence monitor-0 (used for debugging) | - | |
| L | 1 | - | OUT | ASIC sequence monitor-1 (used for debugging) | - | |
| | 2 | - | OUT | ASIC sequence monitor-2 (used for debugging) | - | |
| PortM | 0-3 | A[20]-[23] | IN | CPU address bus (20-23) | 1 | Used for CPU address bus |
| Port | 0 | ADUMCK-1 | OUT | ADU motor clock signal | 1 | (Used for motor control) |
| STPA | 1 | ADUMDIR-1 | OUT | ADU motor rotational direction signal (will be fixed in future) | 1 | (Used for motor control) |
| | 2 | ADUMEN-1 | OUT | ADU motor ON signal | 1 | (Used for motor control) |
| | 3 | CLTRML-1 | OUT | MFP lower drawer tray-up motor ON signal | 1 | 000: Stopped, 100: Upper tray raised |
| | 4 | CLTRMBK-1 | OUT | Drawer tray-up motor braking signal (for both upper and lower) | 1 | 001: Lower tray raised, 111: Braked (other operation not enabled) |
| | 5 | CLTRMU-1 | OUT | MFP upper drawer tray-up motor ON signal | 1 | |
| | 6 | RGTCL-0 | OUT | Registration clutch ON signal | 1 | 0: Registration clutch ON |
| | 7 | TNRMTRON-0 | OUT | Toner motor ON signal | 1 | 0: Toner motor ON |
| Port | 0 | EXTMCK-1 | OUT | Exit motor clock signal | 1 | (Used for motor control) |
| STPB | 1 | EXTMDIR-0 | OUT | Exit motor rotational direction signal | 1 | (Used for motor control) |
| | 2 | EXTMEN-1 | OUT | Exit motor ON signal | 1 | (Used for motor control) |
| | 3 | SCSWD-0 | OUT | Extension I/O switching signal | 1 | |
| | 4 | MMTRON-0 | OUT | Main motor ON signal | 1 | 0: Main motor ON |
| | 5 | MMTRCCW-1 | OUT | Main motor rotational direction signal | 1 | 0: Main motor normal rotation 1: Reverse rotation |
| | 6 | MMTRBK-0 | OUT | Main motor braking signal | 1 | 0: Main motor braked |
| | 7 | SFBCLT-0 | OUT | Bypass clutch ON signal | 1 | 0: Bypass clutch ON |
| Port | 0 | RETS[0] | IN | Extension I/O signal-0 | 1 | |
| STPC | 1 | RETS[1] | IN | Extension I/O signal-1 | 1 | |
| | 2 | RETS[2] | IN | Extension I/O signal-2 | 1 | |
| | 3 | RETS[3] | IN | Extension I/O signal-3 | 1 | |
| | 4 | RETS[4] | IN | Extension I/O signal-4 | 1 | |
| | 5 | RETS[5] | IN | Extension I/O signal-5 | 1 | |
| | 6 | RETS[6] | IN | Extension I/O signal-6 | 1 | |
| | 7 | RETS[7] | IN | Extension I/O signal-7 | 1 | |
| Port | 0 | REVMCK-1 | OUT | Reverse motor clock signal | 1 | (Used for motor control) |
| STPD | 1 | REVMDIR-0 | OUT | Reverse motor rotational direction signal | 1 | (Used for motor control) |
| | 2 | REVMEN-1 | OUT | Reverse motor ON signal | 1 | (Used for motor control) |
| | 3 | KISYU3 | IN | - | - | - |
| | 4 | SIZE[0] | IN | Extension I/O2 signal-0 | 1 | |
| | 5 | SIZE[1] | IN | Extension I/O2 signal-1 | 1 | |
| | 6 | SIZE[2] | IN | Extension I/O2 signal-2 | 1 | |
| | 7 | SIZE[3] | IN | Extension I/O2 signal-3 | 1 | |

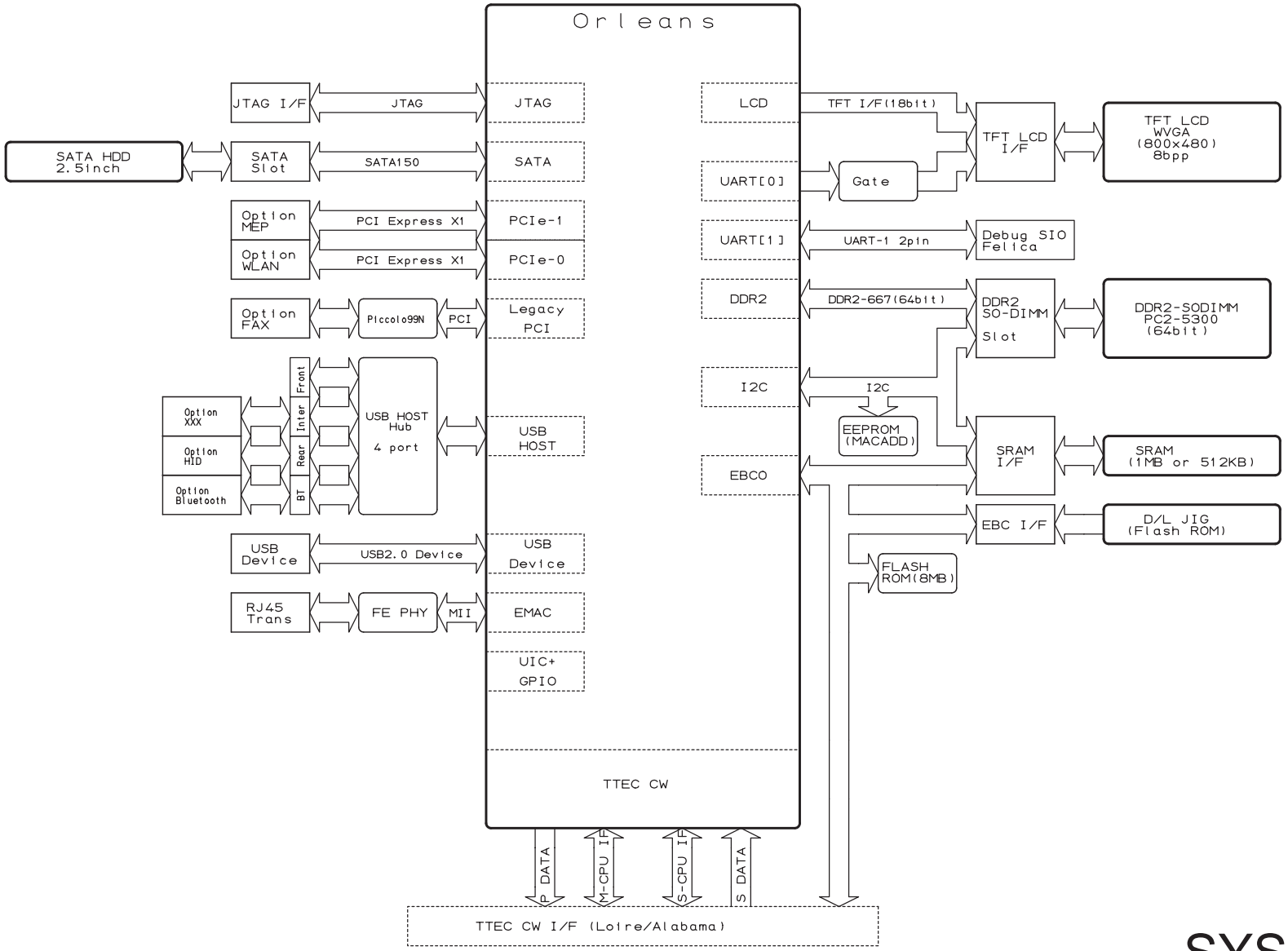
e-STUDIO205L/255/305/355/455
LGC ASIC PORT LIST (IC18)

| Port | CPU I/O PIN | Signal | I/O | Description | ACTIVE |
|---|---|---|---|---|---|
| 1 | P91 | LDRDY | I | Laser forcible OFF signal (in HDEN) | L |
| 2 | PC0 | DDISI1 | I | Laser forcible OFF signal (input) | H |
| 3 | P94 | LDON | I | Laser forcible ON signal | L |
| 4 | P93 | LDOFF | I | Image data forcible OFF signal | L |
| 5 | P92 | LE | I | Laser enable signal | L |
| 6 | P95 | MVDEN | I | Scanning (vertical direction) enable signal (from CPU) | L |
| 7 | PN3 | PVDEN | O | Scanning (vertical direction) enable signal (to CPU) | L |
| 8 | PN1 | GCCTCP | O | Pixel counter match signal | H |
| 9 | PN2 | HSYNCERR | O | HSYNC error signal | H |
| 10 | - | IVSYNC | O | Vertical scanning direction sync signal (to SYS board) | L |
| 11 | - | IRCLK | O | Image data sync clock signal (to SYS board) | - |
| 12 | - | IHSYNC | O | Horizontal scanning direction sync signal (to SYS board) | L |
| 13 | - | IDATXA[0-7] | I | Image data from SYS board | - |
| 14 | - | IHDEN | I | Scanning (horizontal direction) enable signal (from SYS board) | L |
| 15 | - | IVDEN | I | Scanning (vertical direction) enable signal (from SYS board) | L |
| 16 | - | IDCLK | I | Image data sync clock signal (from SYS board) | - |
| 17 | - | LVDS1OUT-0 | O | Laser ON/OFF signal (to LDR board) | |
| 18 | - | LVDS1OUT-1 | O | (2 LVDS signals used as a pair) | - |
| 19 | - | WRAPC1 | O | Write APC signal (to LDR board) | L |
| 20 | - | DDISO1 | O | Laser forcible OFF (output) signal (to LDR board) | H |
| 21 | - | BDIN | I | Horizontal scanning direction sync signal (from SNS board) | L |
| 22 | P90 | VSYNCEN | - | VSYNC output enable signal | L |

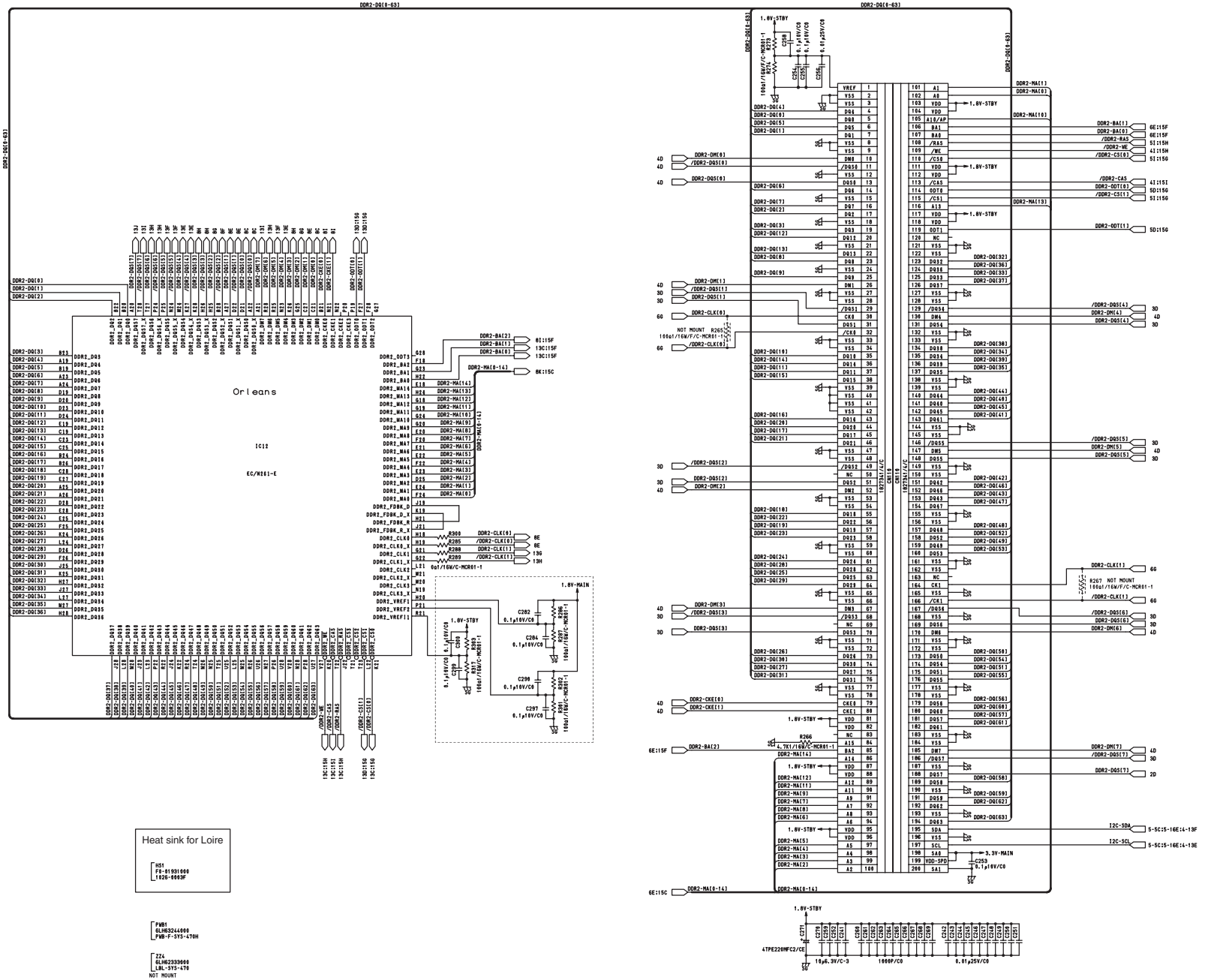
# Loire/Alabama System Board
# Circuit Diagram

| Sheet No. | Contents | Note |
|---|---|---|
| 001 | Index | |
| 002 | Block Diagram | |
| 003 | Orleans - DDR2, SO-DIMM SLOT | |
| 004 | Orleans - EBC (BootROM, SRAM I/F), GPIO, FAN | |
| 005 | Orleans - ETHERNET, SATA, USB HOST/DEVICE, I2C, LCDC, JTAG | |
| 006 | Orleans - PCI(FAX I/F), PCI EXPRESS(WLAN, MeP) | |
| 007 | Orleans - TTEC CW , SLG I/F, LGC I/F, IMG I/F | |
| 008 | Orleans - POWER, GND, CLOCK | |
| 009 | POWER - (CONNECTOR), RESET, DC-DC | |

# Loire Alabama SYSTEM Board Block Diagram

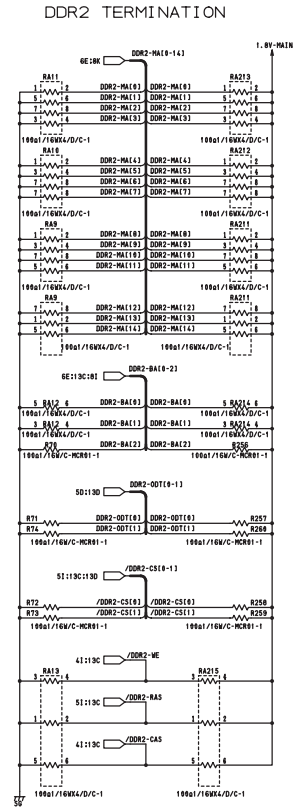


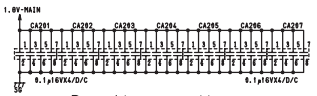

SYS 2/9



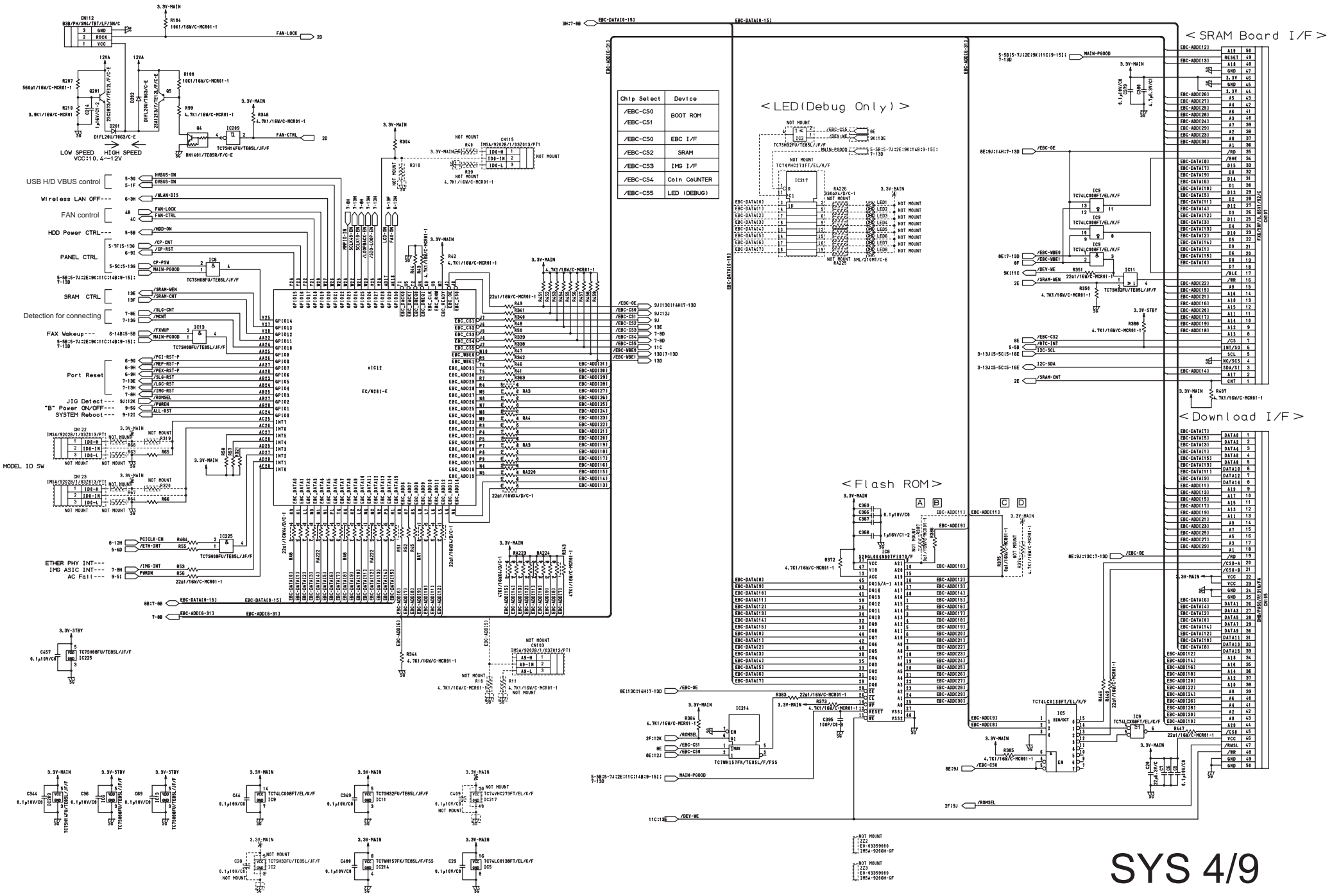







SYS 3/9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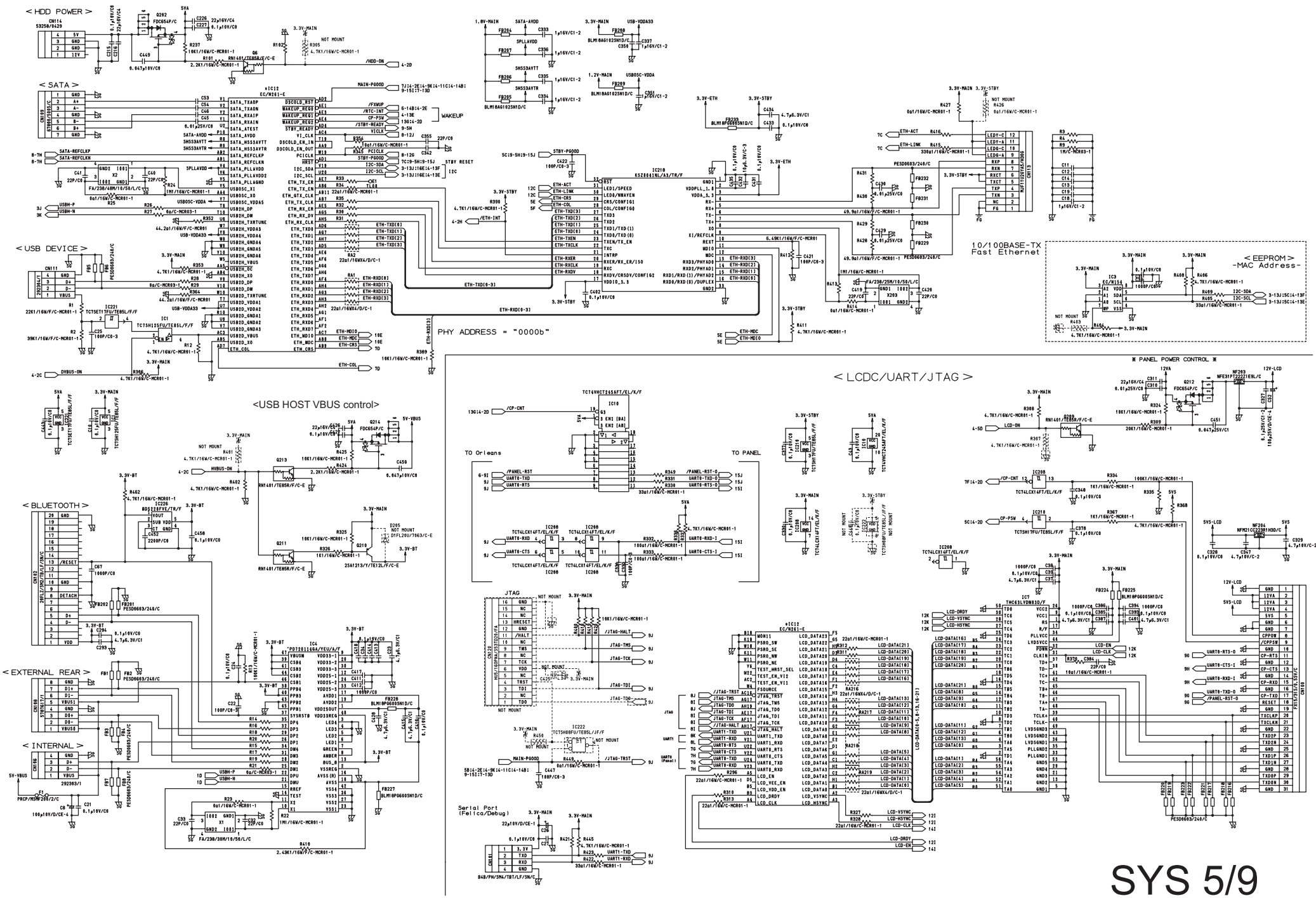
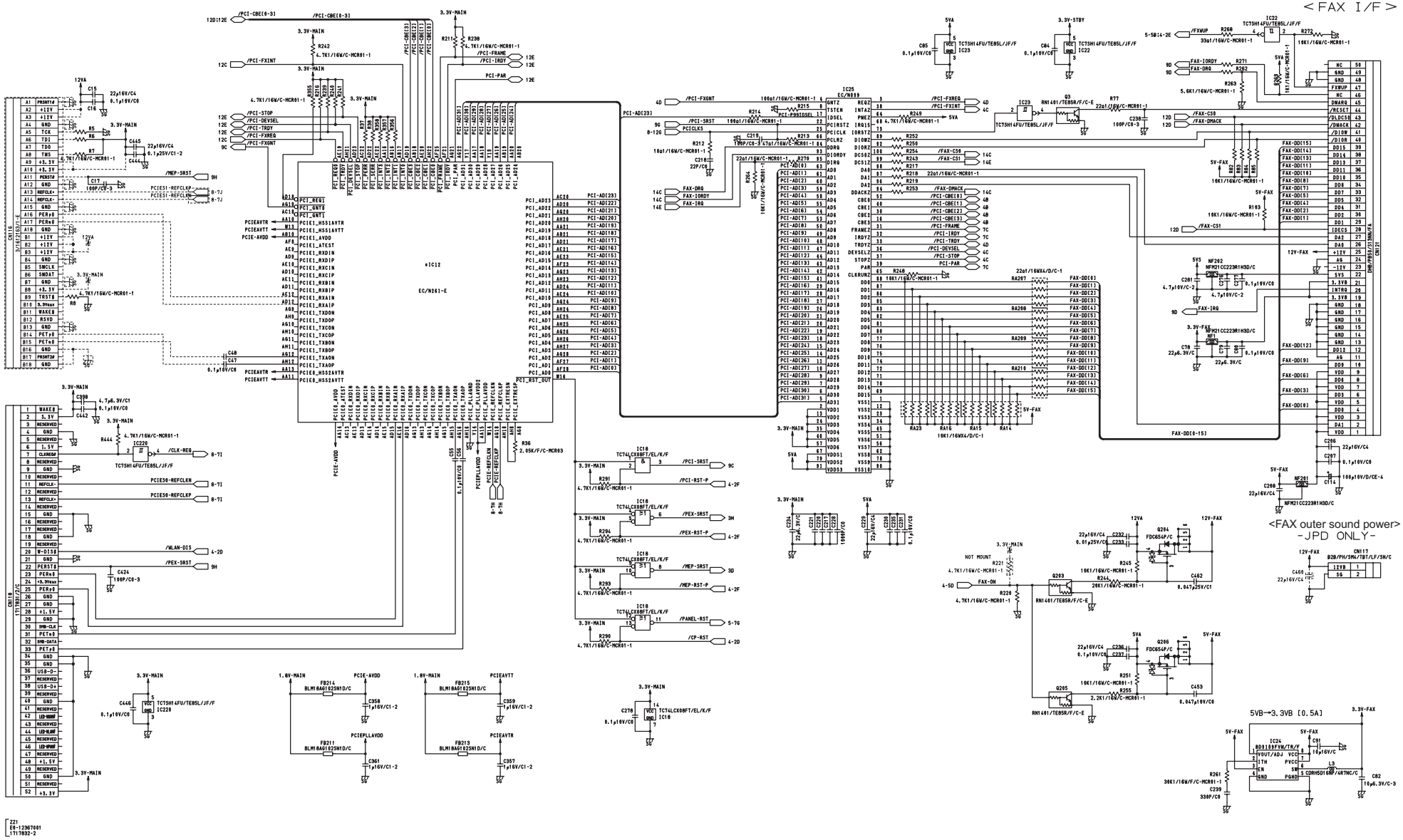
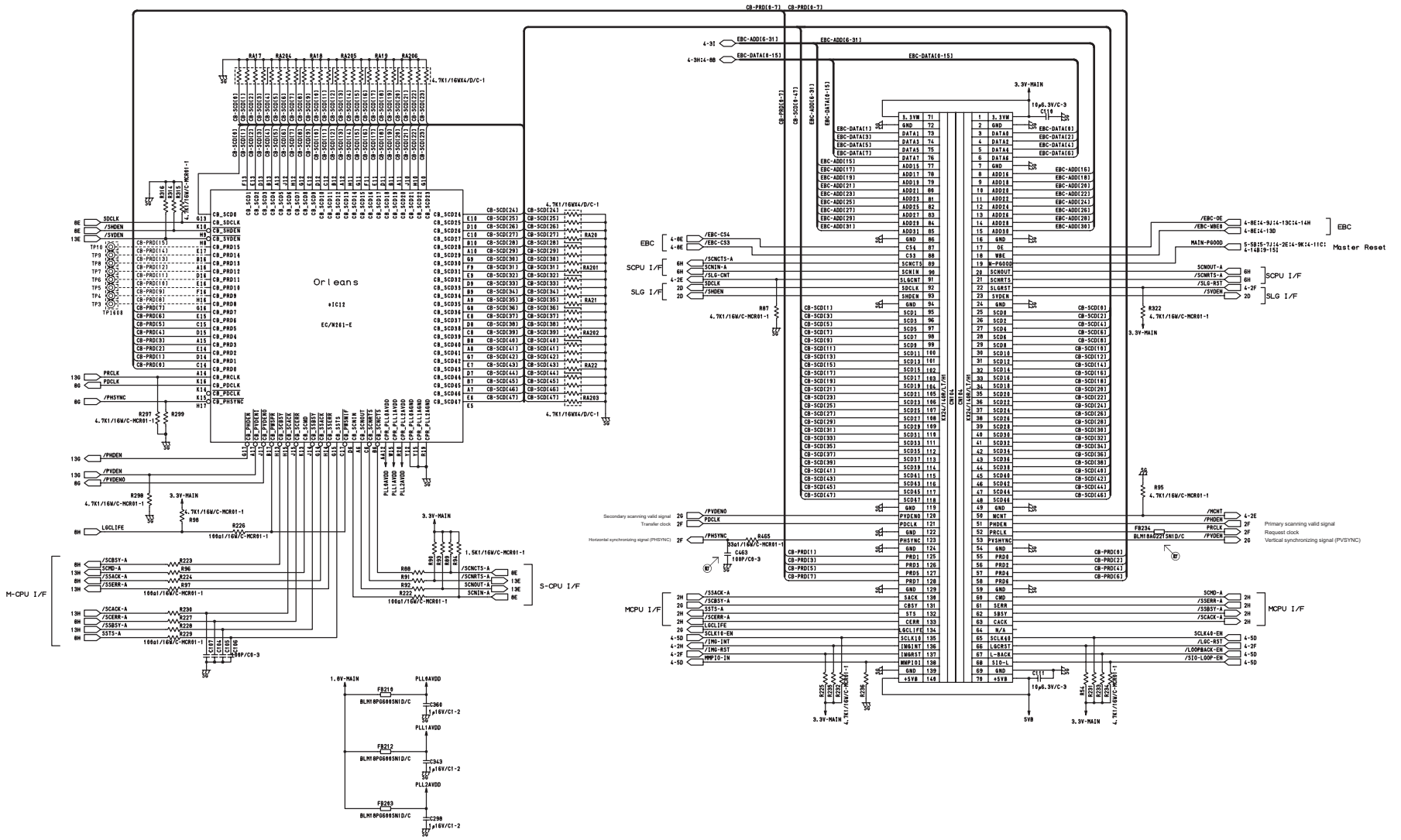
< LED(Debug Only) >
< SRAM Board I/F >
< Download I/F >
< Flash ROM >
Chip Select
Device
/EBC-CS0
/EBC-CS1
BOOT ROM
/EBC-CS0
EBC I/F
/EBC-CS2
SRAM
/EBC-CS3
IMG I/F
/EBC-CS4
Coin CoUNTER
/EBC-CS5
LED (DEBUG)
USB H/D VBUS control
Wireless LAN OFF---
FAN control
HDD Power CTRL---
PANEL CTRL
SRAM CTRL
Detection for connecting
FAX Wakeup---
Port Reset
JIG Detect---
"B" Power ON/OFF---
SYSTEM Reboot---
MODEL ID SW
ETHER PHY INT---
IMG ASIC INT---
AC Fail---
LOW SPEED
HIGH SPEED
VCC:↑0.4~↓2V
EC/W161-E
SYS 4/9
WWW.SERVICE-MANUAL.NET

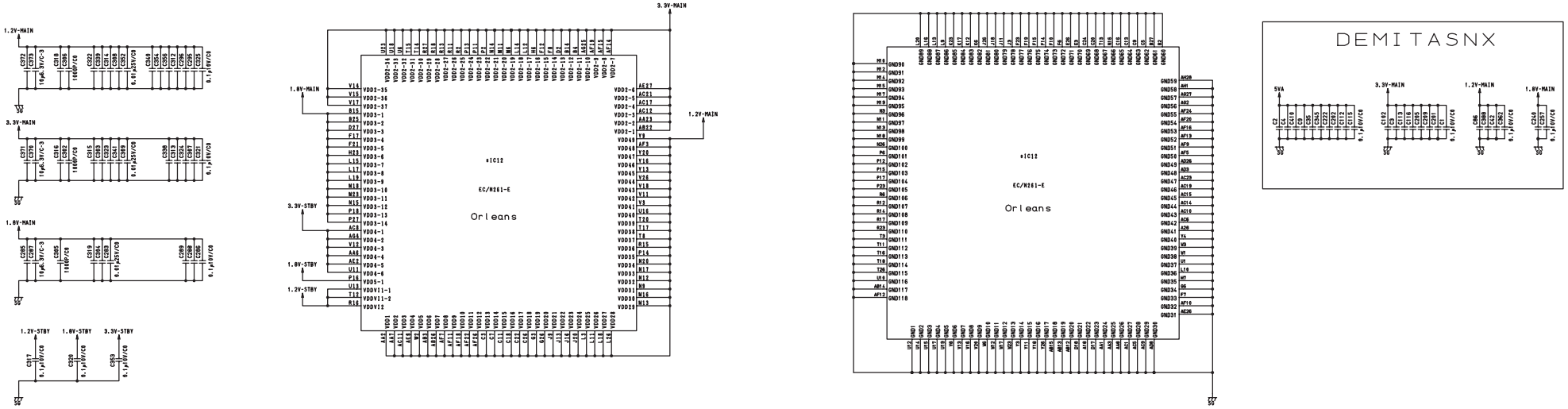




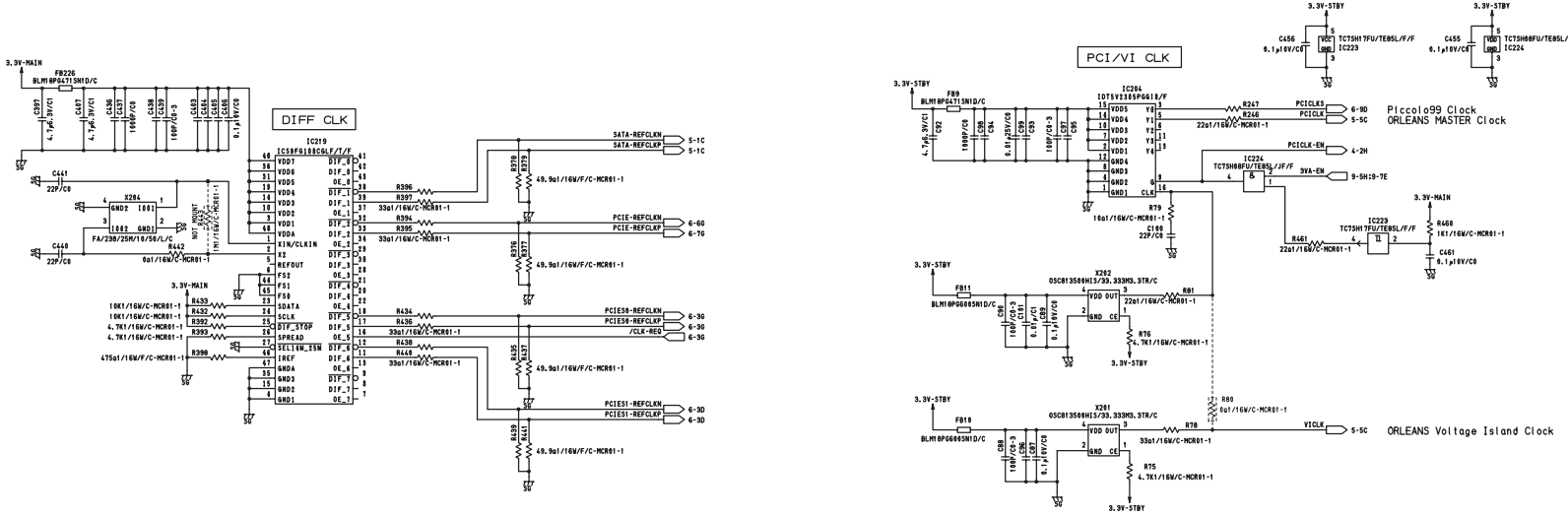



SYS 7/9

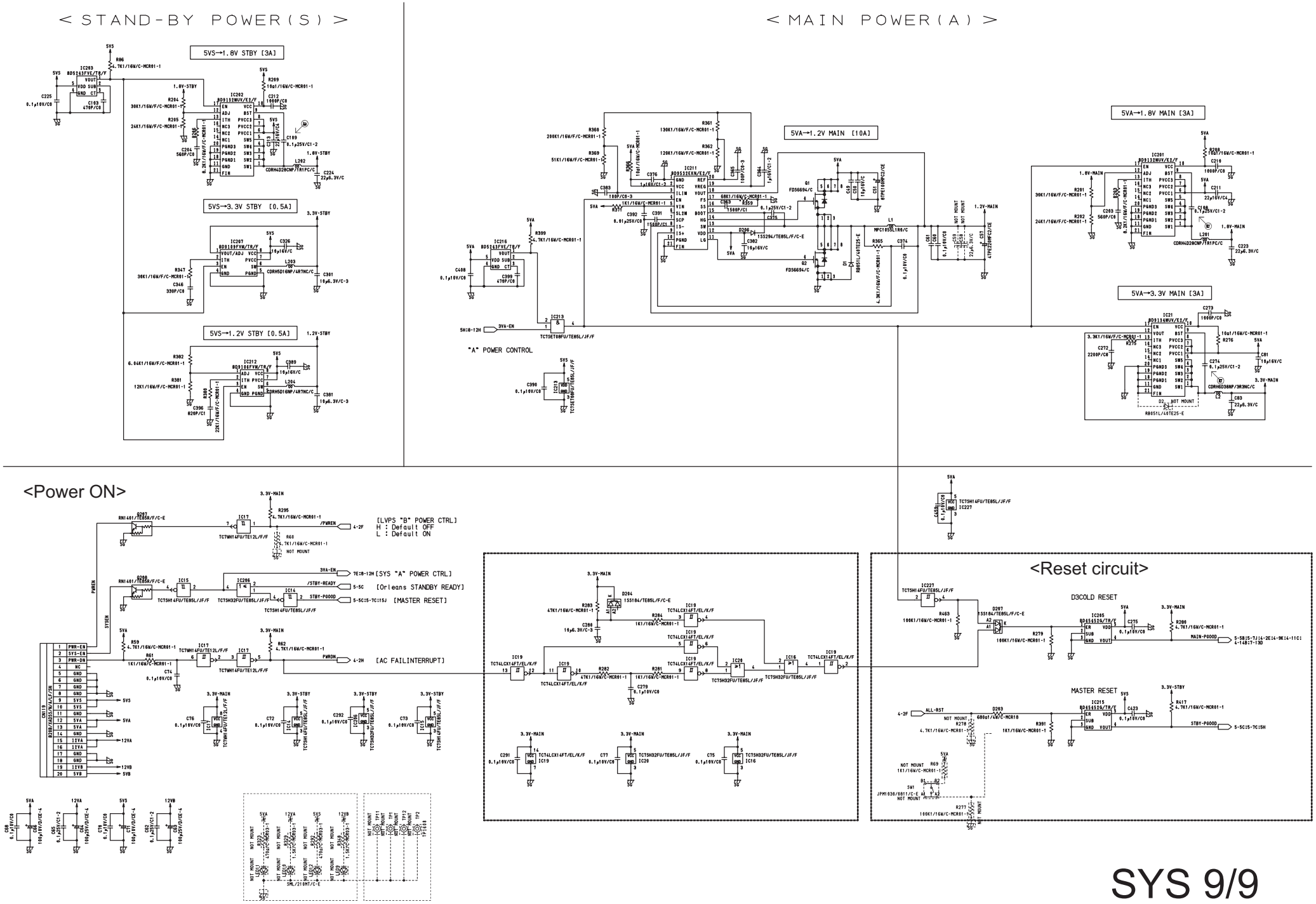
## POWER




## CLOCK

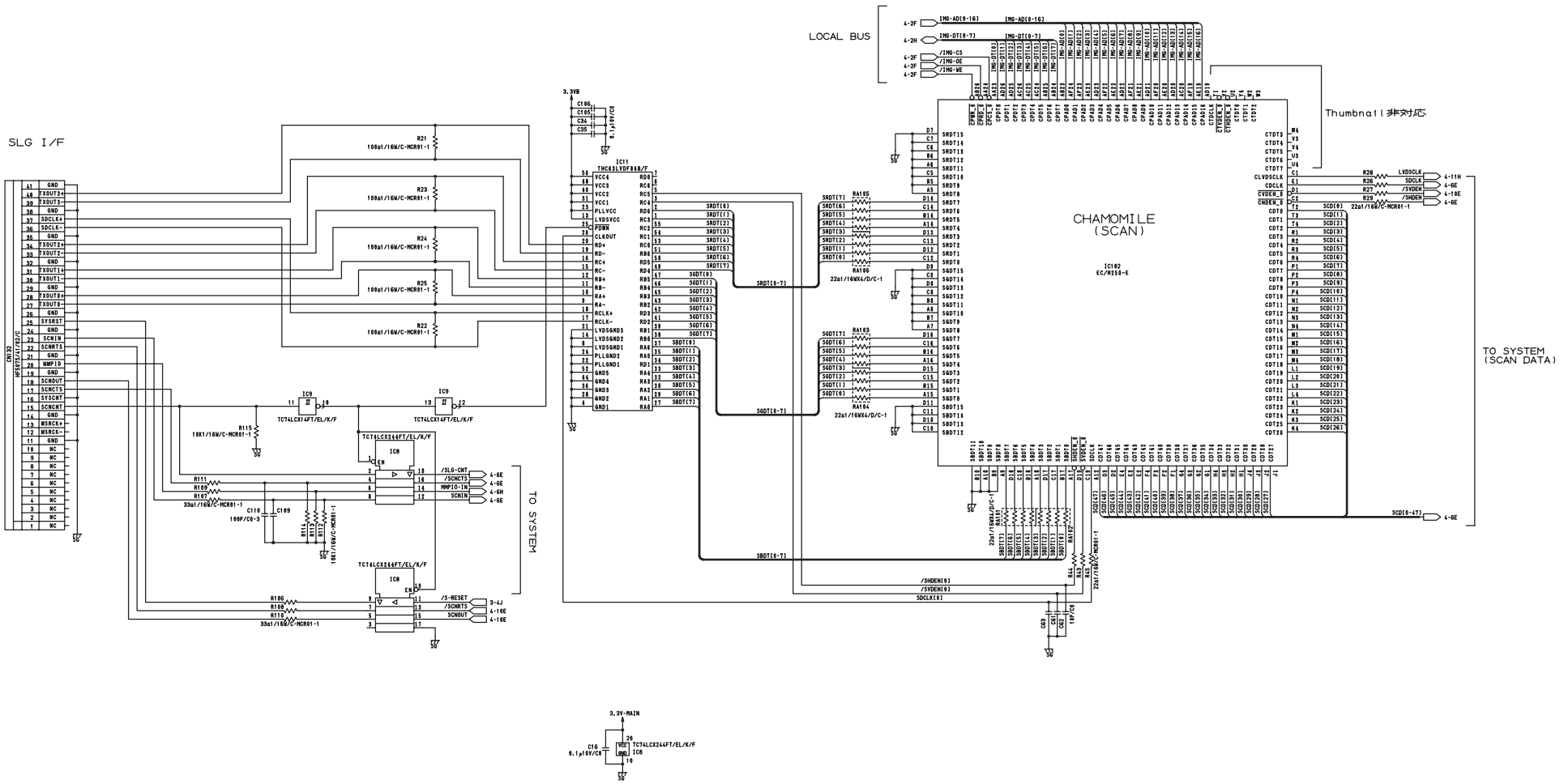



# SYS 8/9



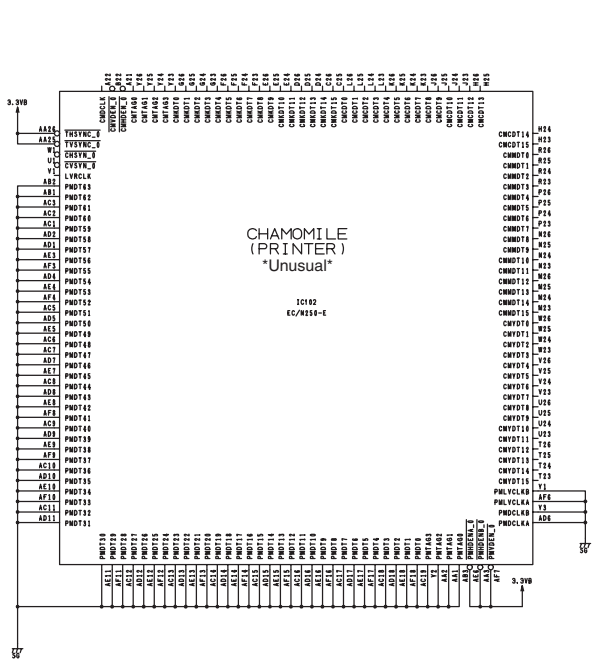
# Loire Image Board
# Circuit Diagram

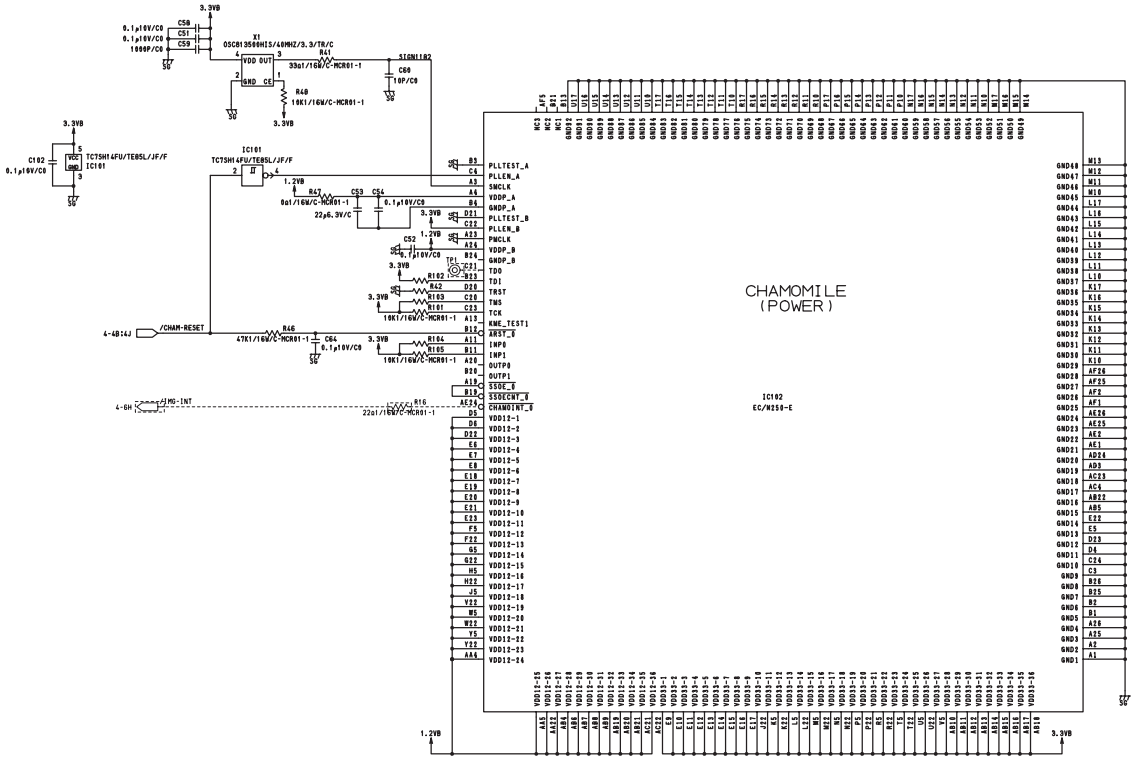
| Sheet No. | Contents | Note |
|---|---|---|
| 001 | Index | |
| 002 | CHAMOMILE(1/3) , SLG I/F | |
| 003 | CHAMOMILE (2/3 , 3/3) | |
| 004 | SYS I/F, LGC I/F , COIN COUNTER I/F | |



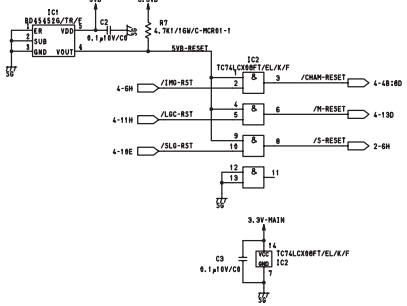



IMG 2/4




B POWER RESET



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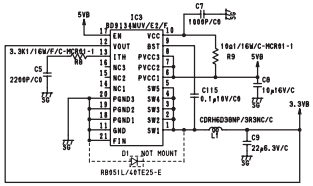

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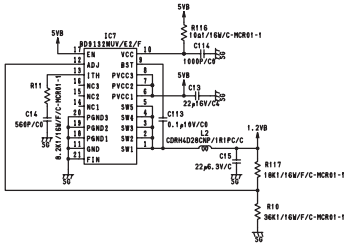
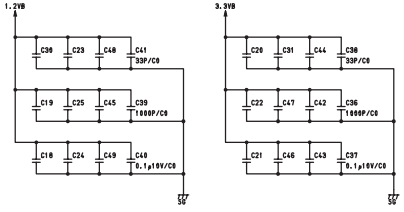
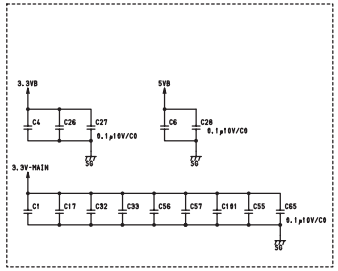
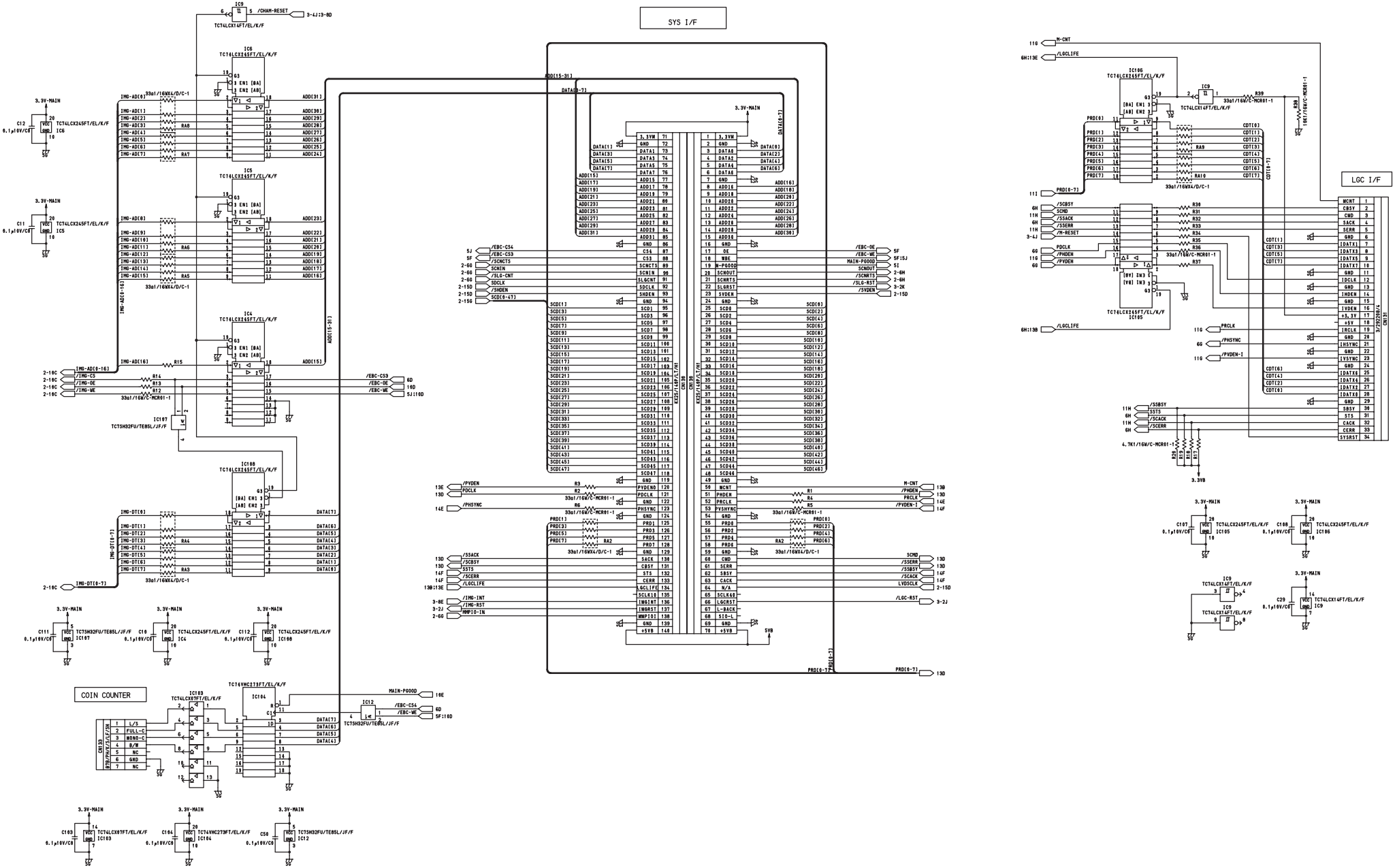


DECOUPLING CAP



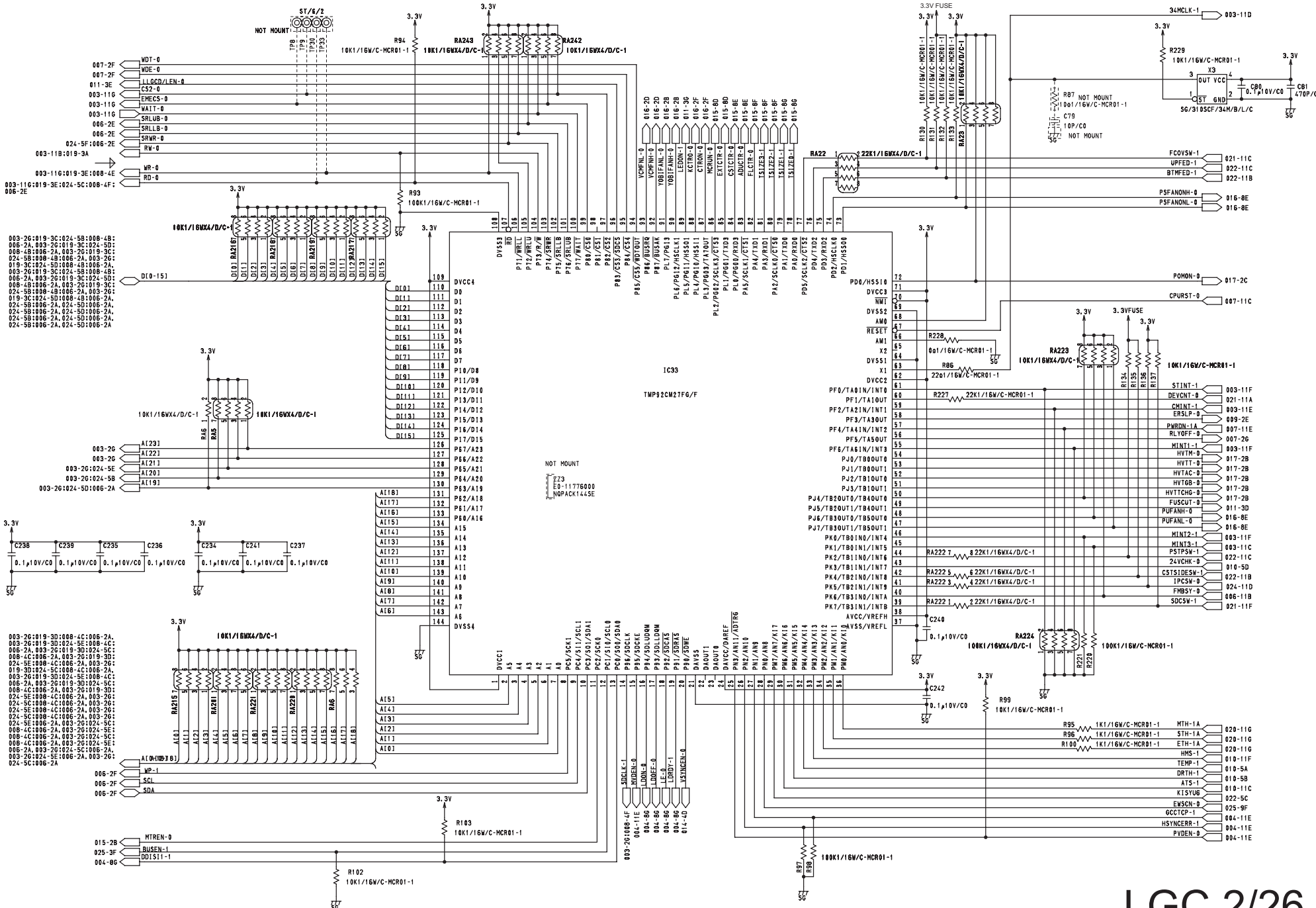


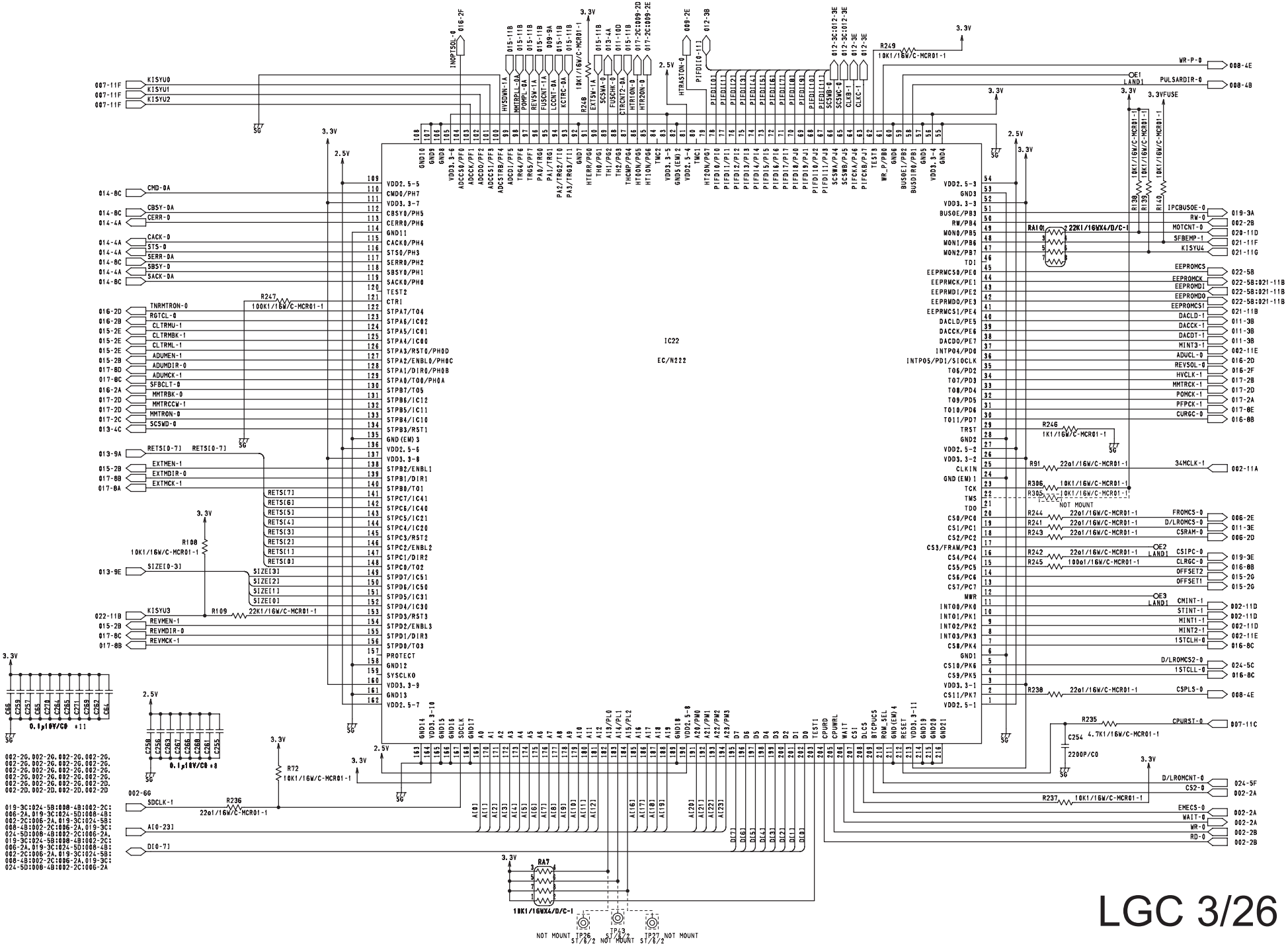
IMG 3/4

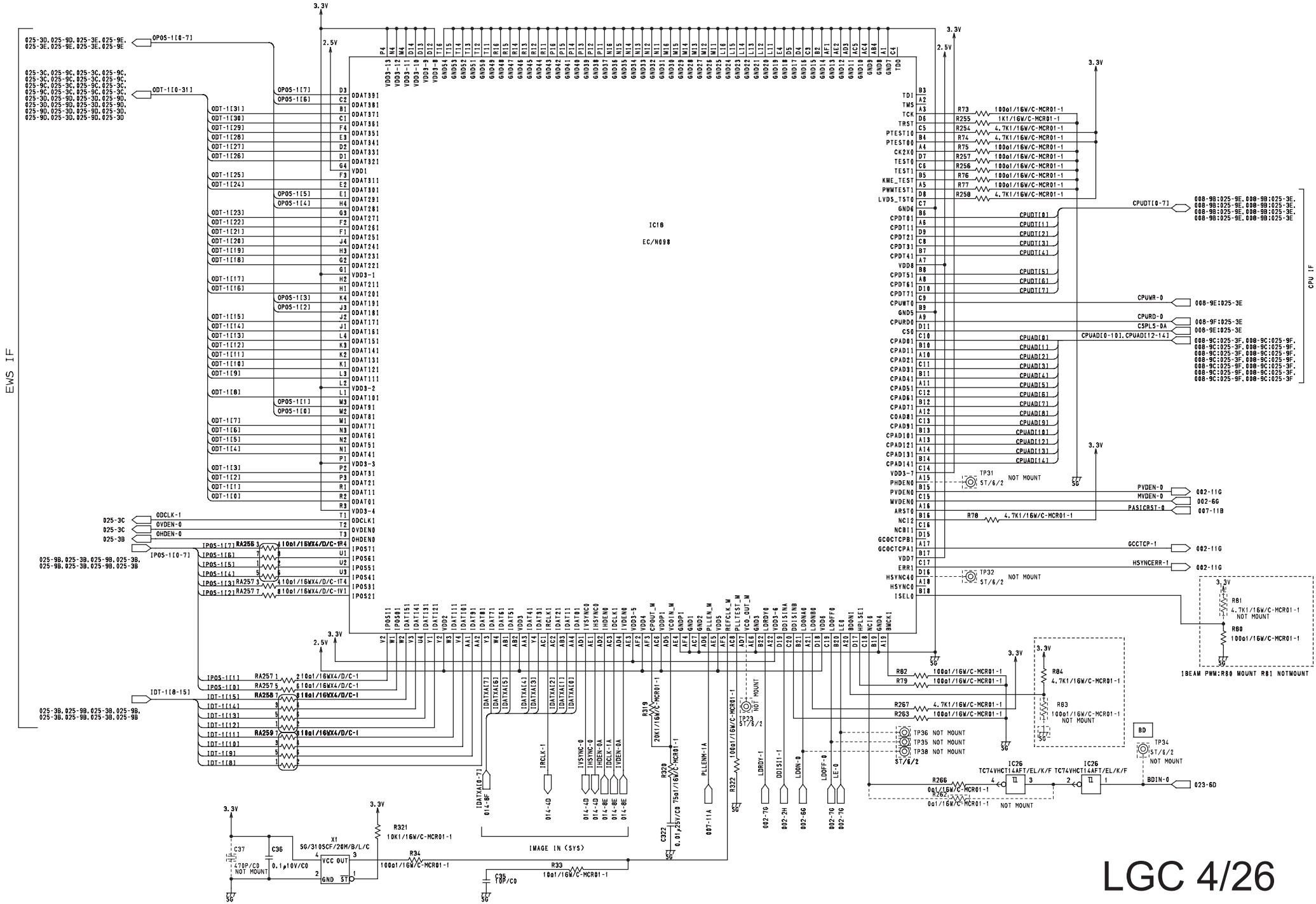


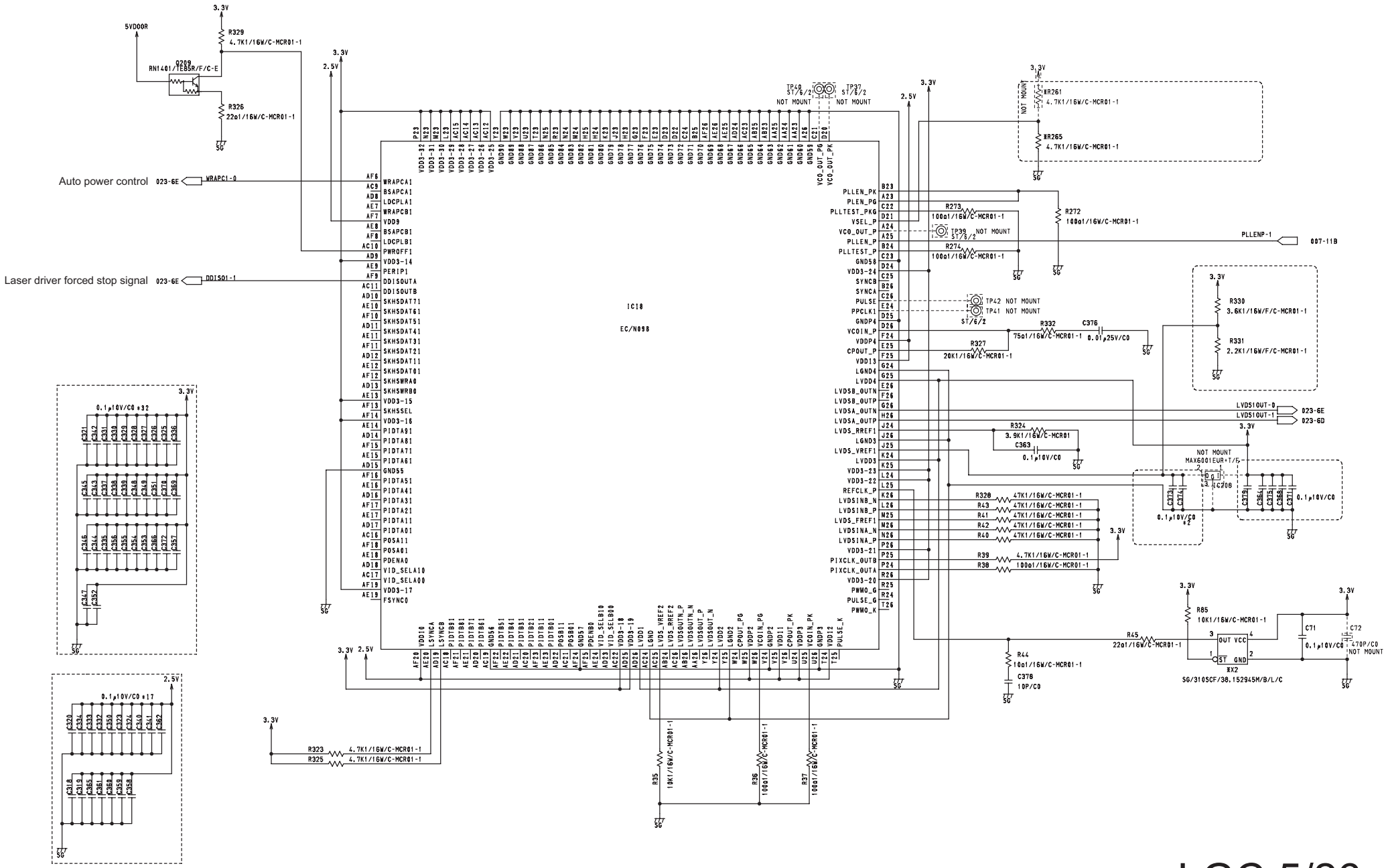
# Loire LGC board Circuit Diagram

| Sheet No. | | | |
|---|---|---|---|
| 001 | Index | 018 | Thermistor high-temperature detecting circuit |
| 002 | CPU | 019 | Bus buffer for finisher |
| 003 | ASIC | 020 | Connector 1 (LVPS, HVPS, Thermistor, MOT board etc.), Power supply circuit |
| 004 | Printer ASIC 1 | 021 | Connector 2 (Counter, Inner option, ADU, Bypass, Fan) |
| 005 | Printer ASIC 2 | 022 | Connector 3 (Drawer, Main motor, PFP) |
| 006 | Memory (SRAM, FROM, EEPROM, NVRAM, BATTERY) | 023 | Connector 4 (LSU, SYS) |
| 007 | Reset circuit, +3.3 VSW forming circuit | 024 | Connector 5 (D/L, Debug, Finisher) |
| 008 | Buffer for Printer ASIC | 025 | Connector 6, (Linux) |
| 009 | HTR lighting circuit, Discharge LED lighting circuit | 026 | Condenser for EMI countermeasure |
| 010 | 24 VOFF detecting circuit, Drum thermistor, Temperature and humidity sensor, Operational amplifier for ATS laser power | 027 | |
| 011 | DAC, D/L model identifying circuit, D/L LED, FUSE melt-cutting circuit | 028 | |
| 012 | PFP or LCF IF | 029 | |
| 013 | Expansion bus (Input) | 030 | |
| 014 | SYS board IF | 031 | |
| 015 | Motor ON Buffer, CST Tray up motor driver, Counter, JOB separator (OCT) motor | 032 | |
| 016 | Each clutch, fan and solenoid driver | 033 | |
| 017 | HVT IF, Main motor, Paper transport motor, Polygonal motor control, Relay circuit, MOT board IF | 034 | |
| | | 035 | |

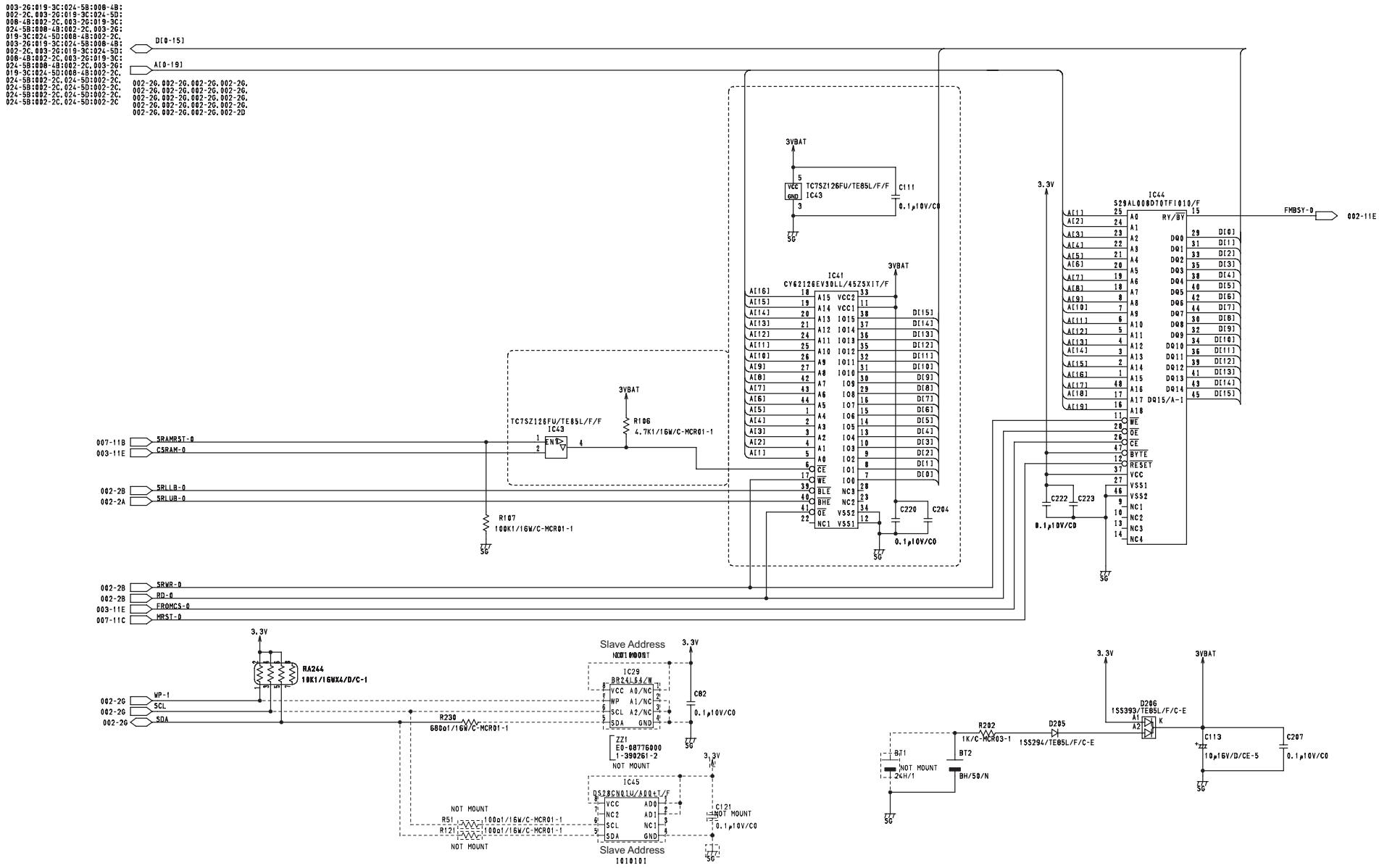




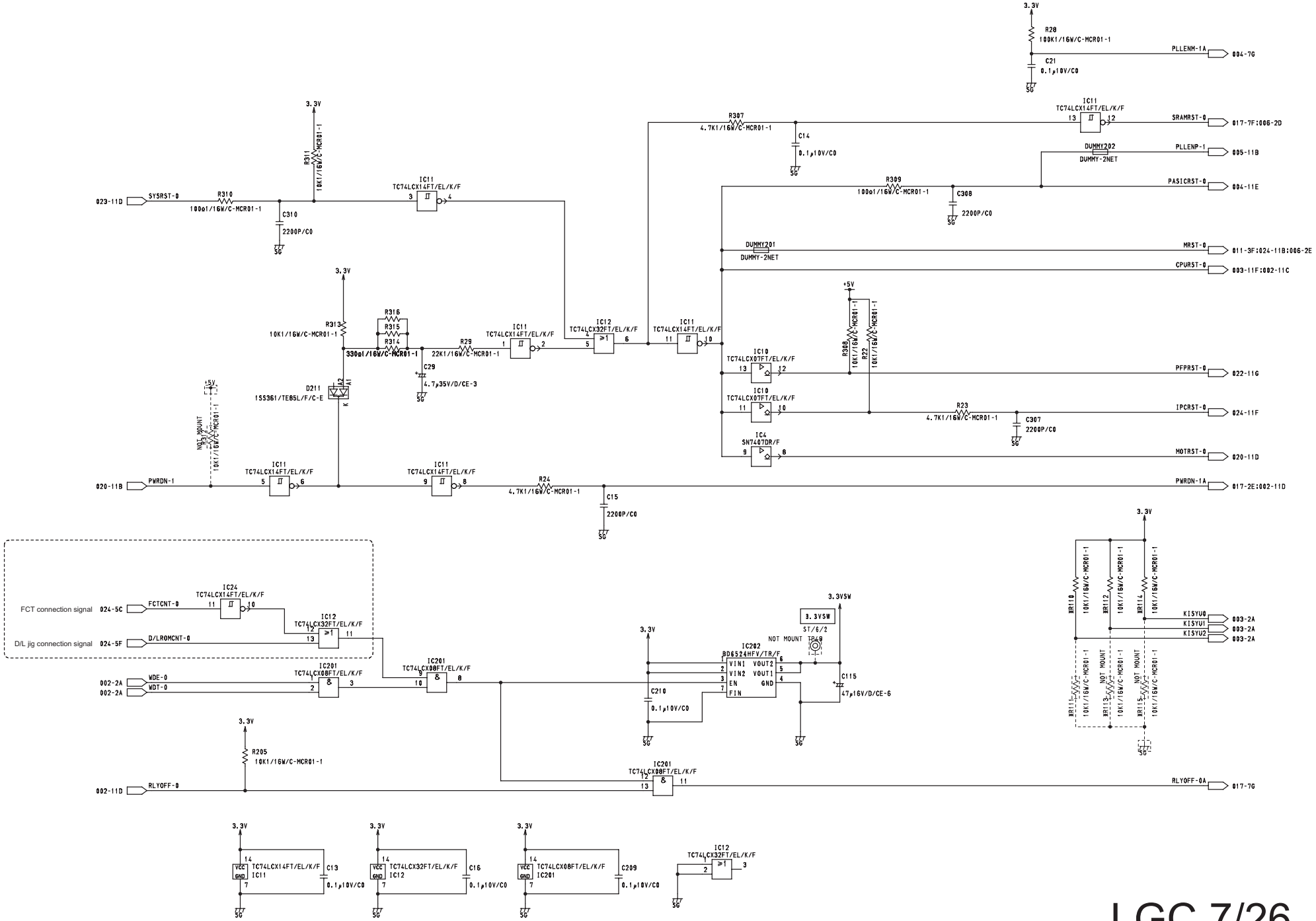




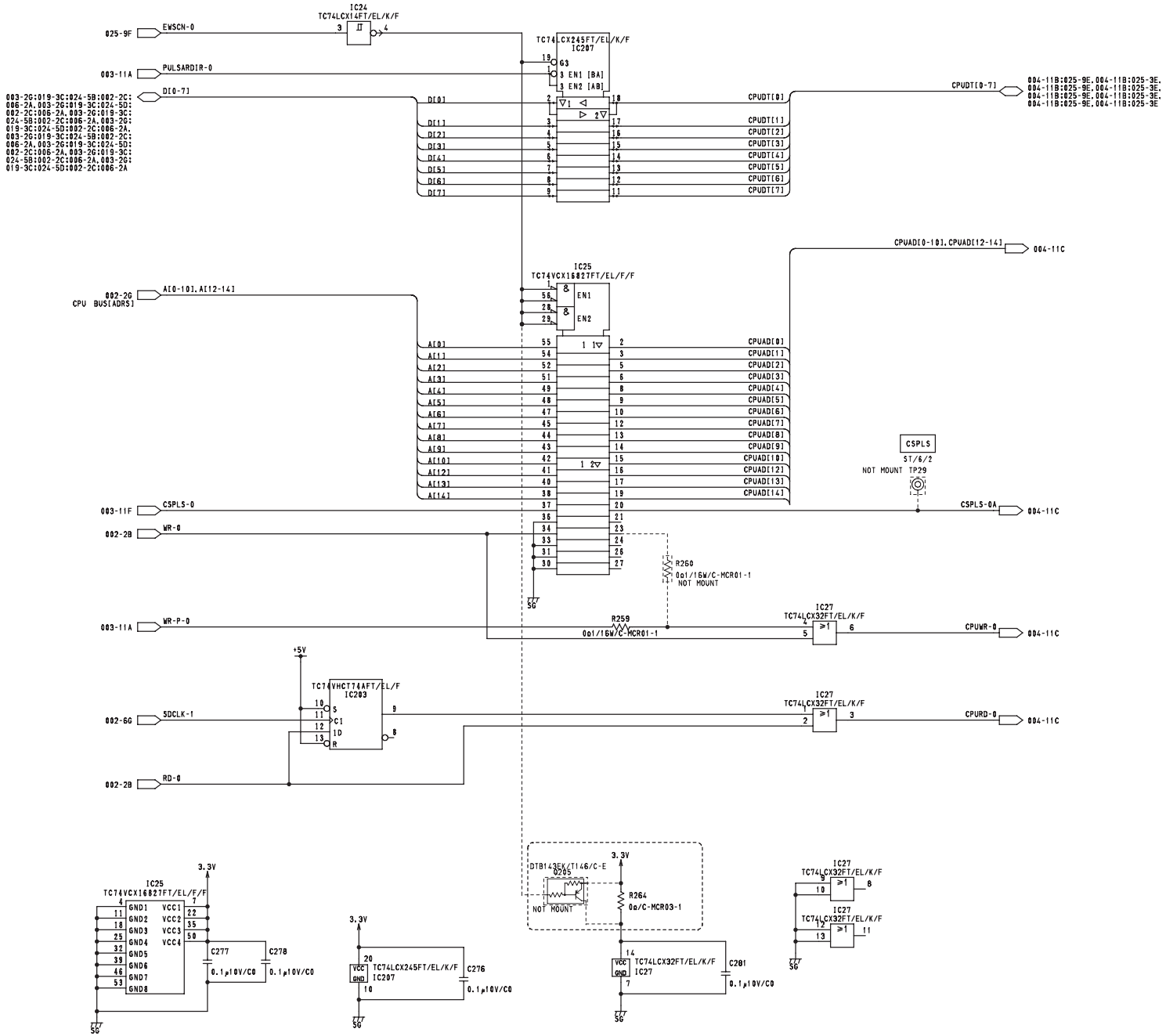

LGC 5/26




LGC 6/26




LGC 7/26

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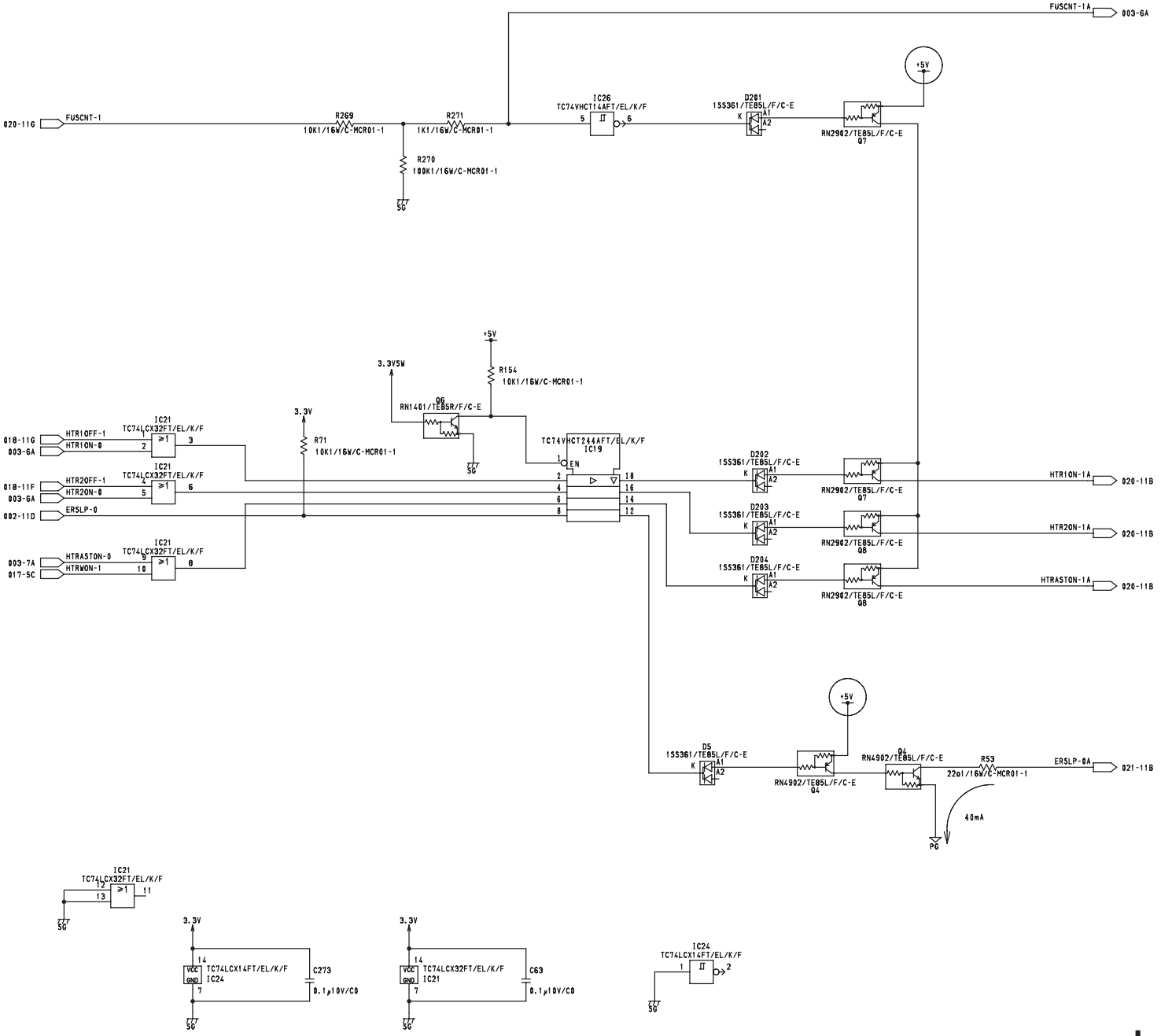


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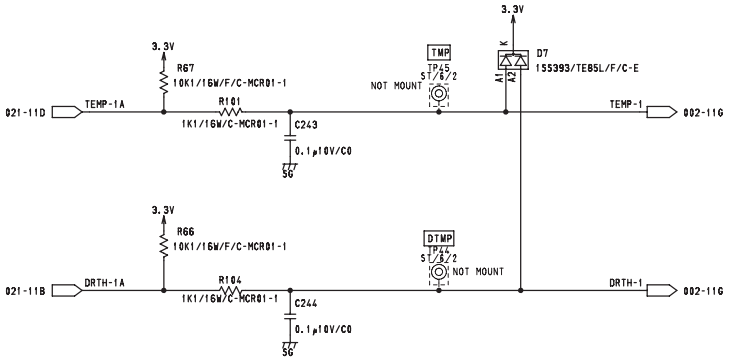
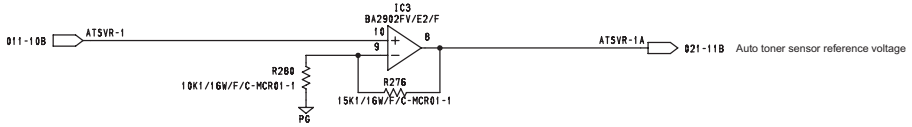
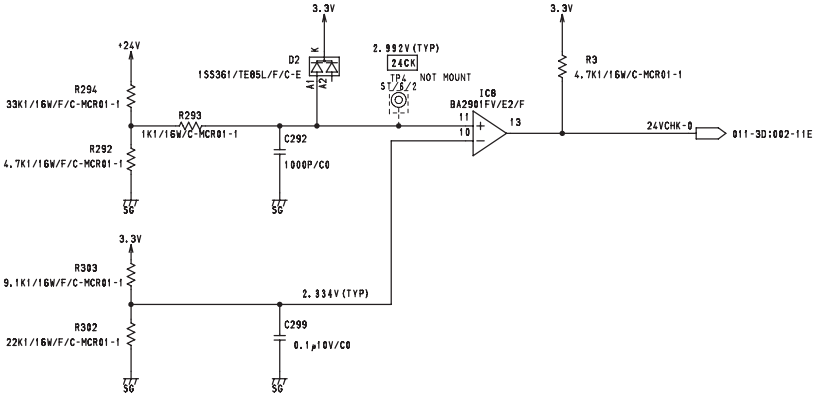
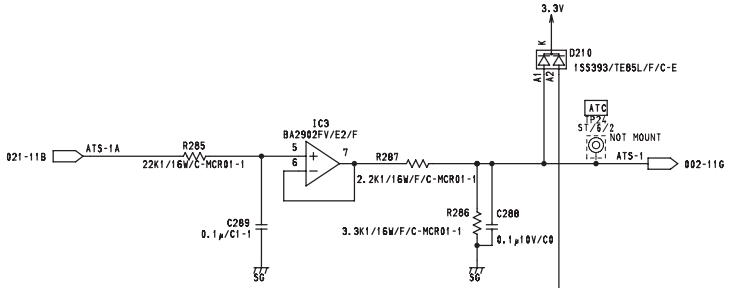
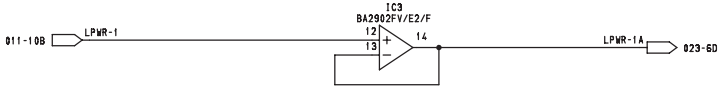
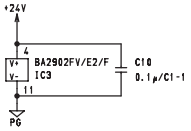


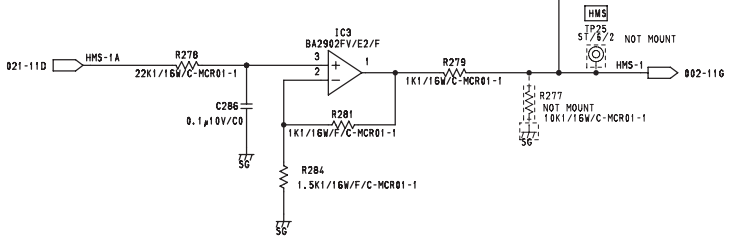



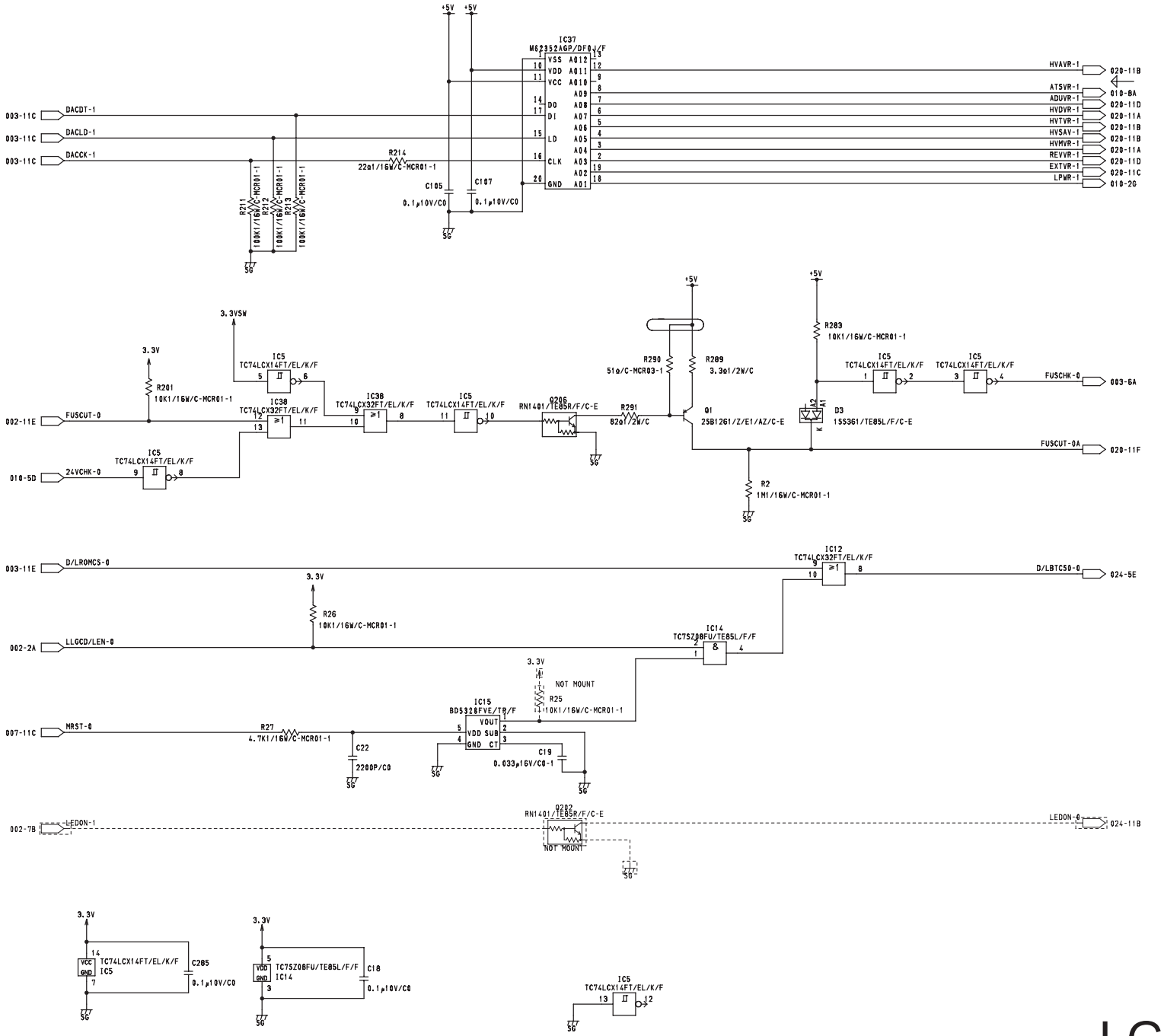



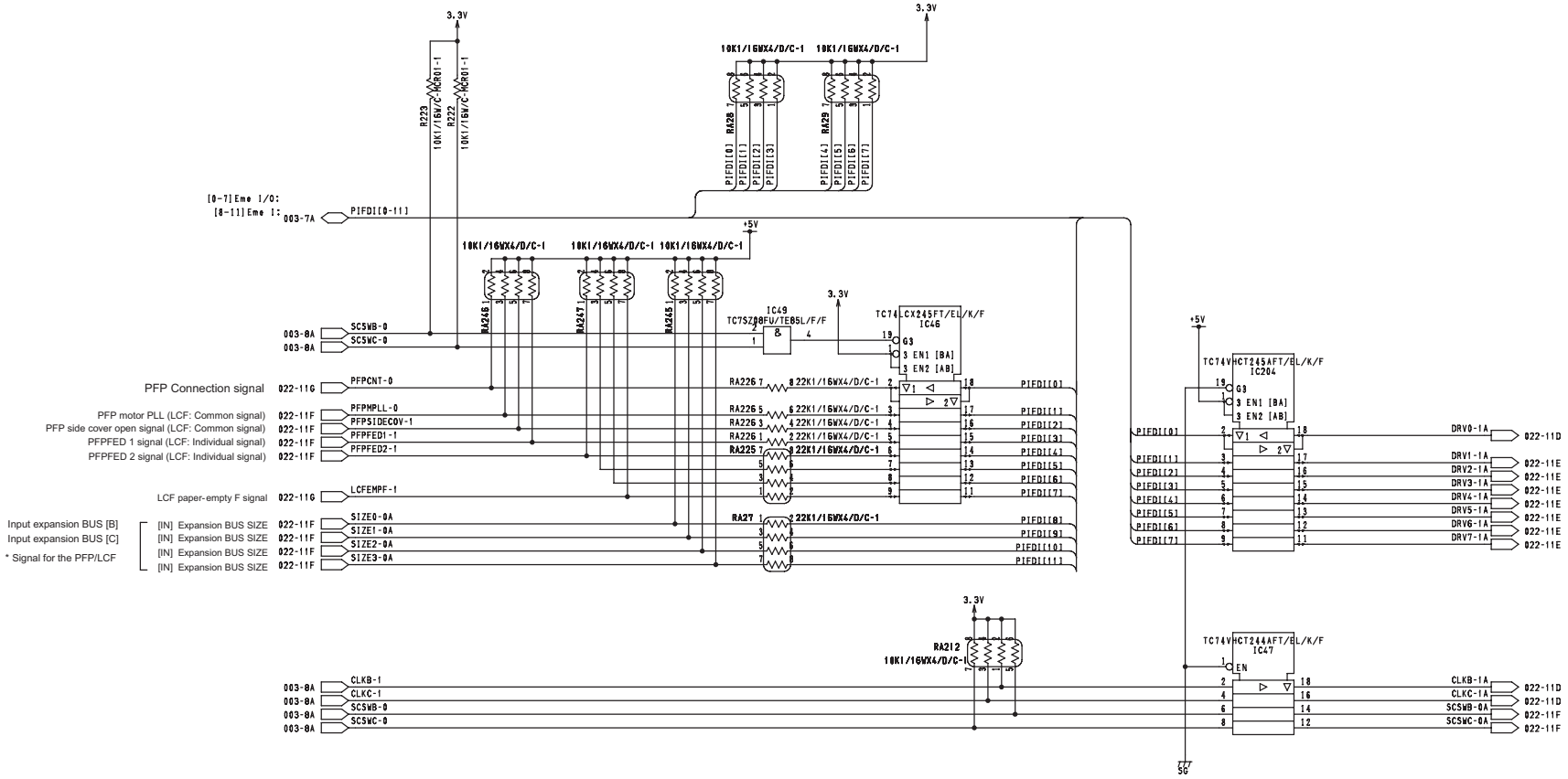



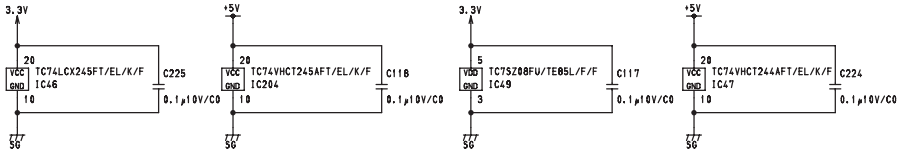



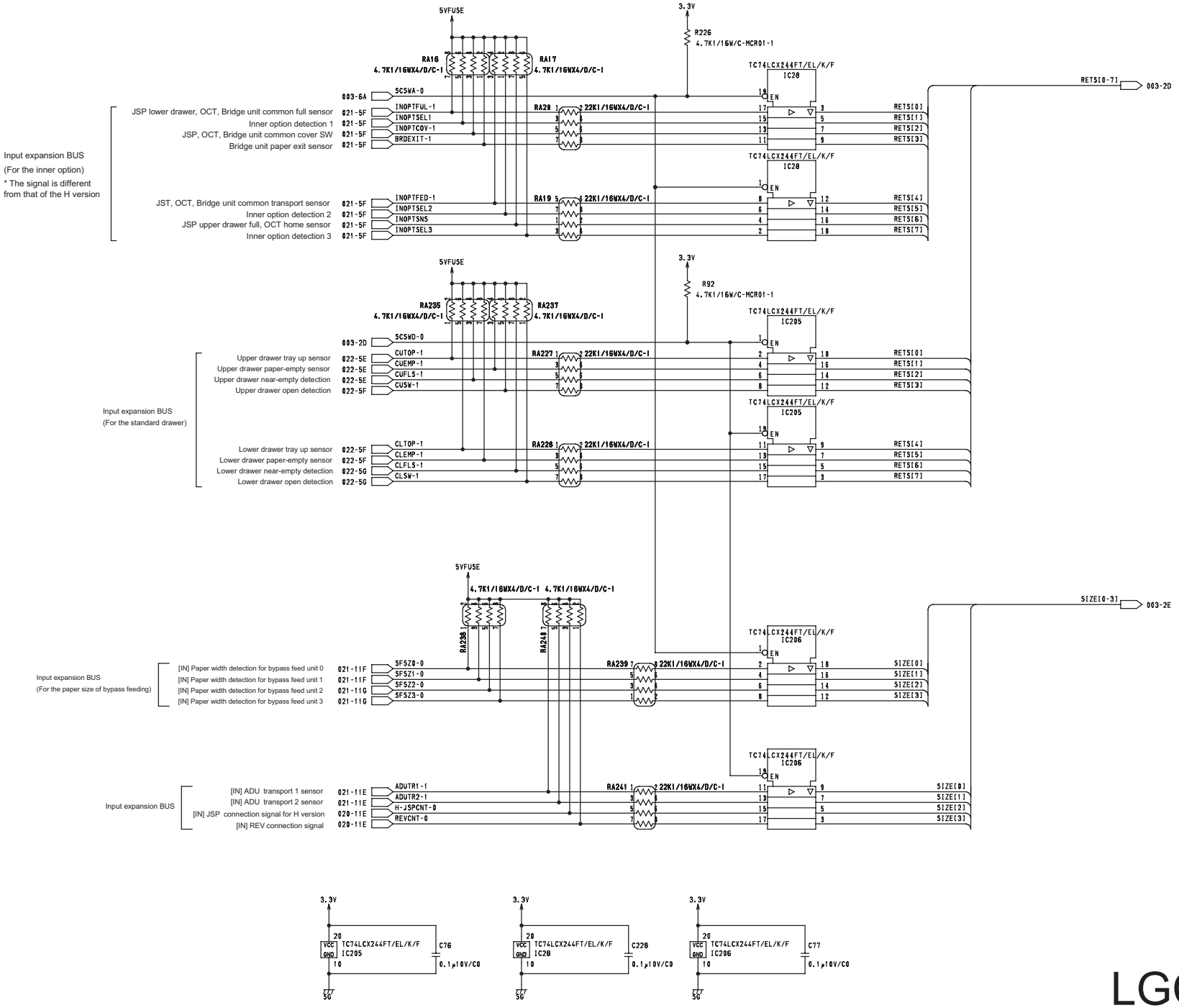

LGC 10/26

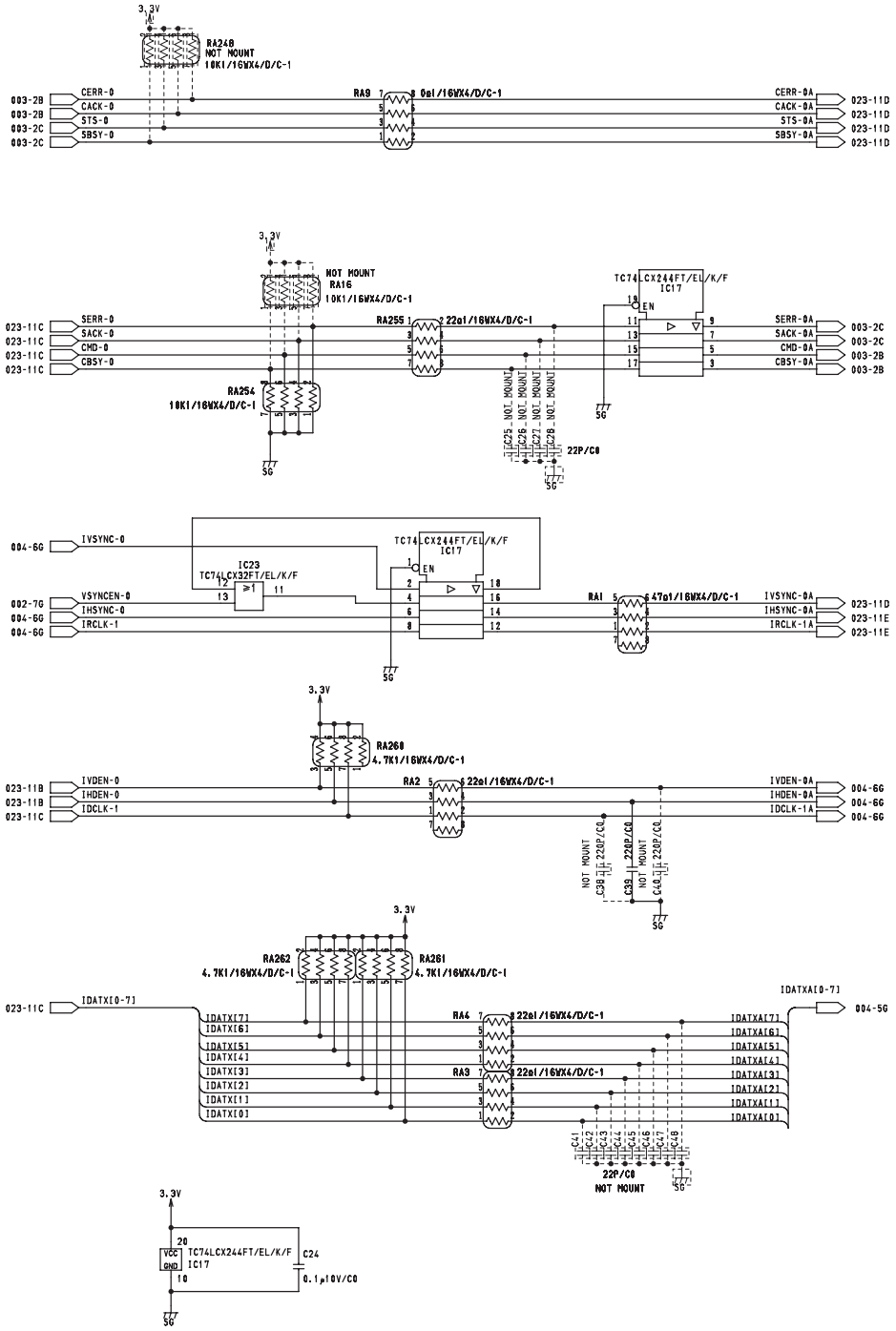


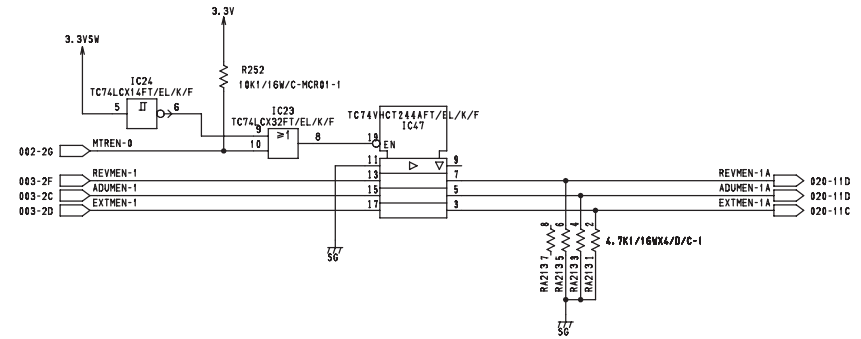

LGC 11/26

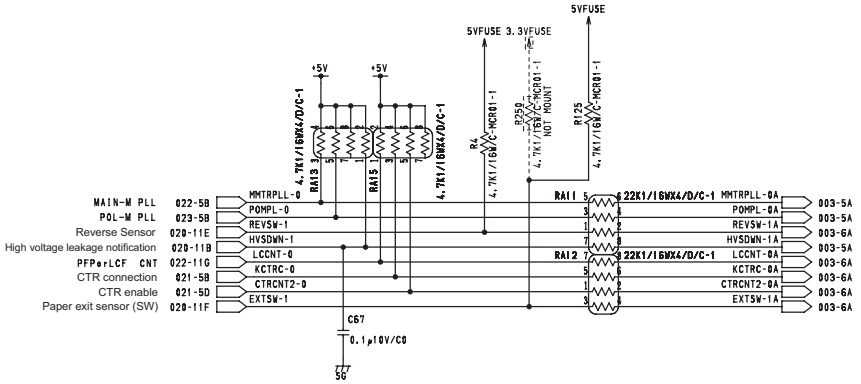


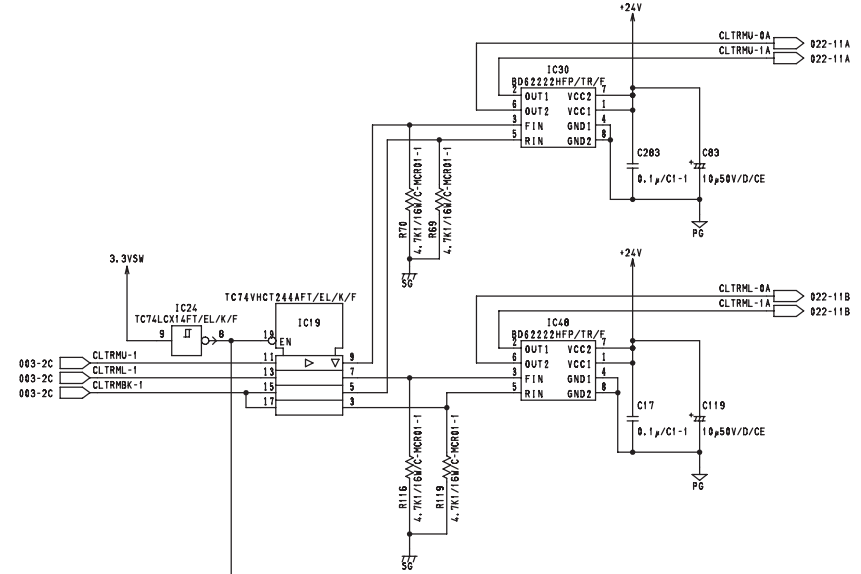



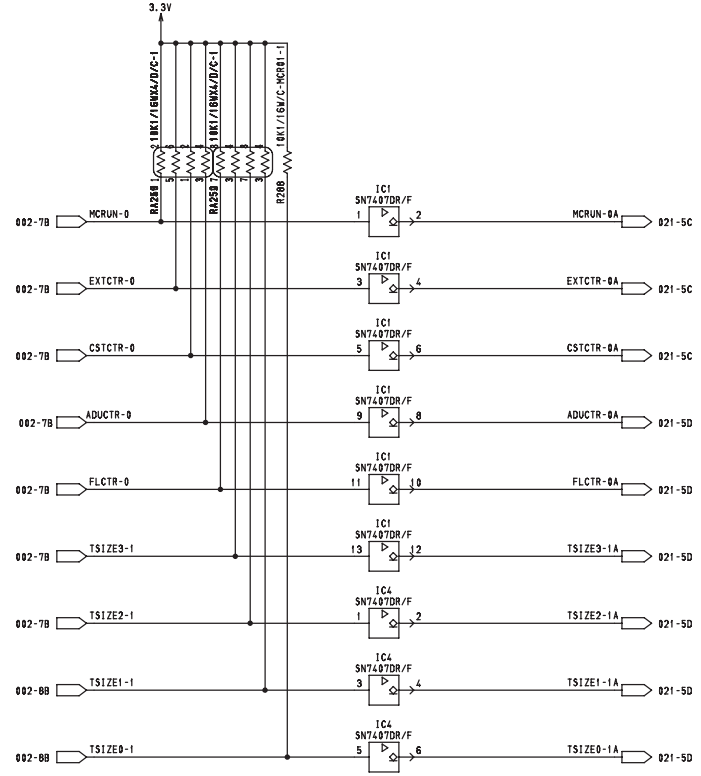


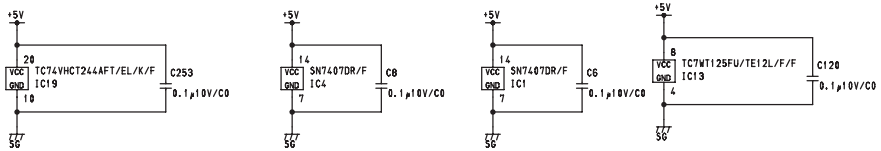


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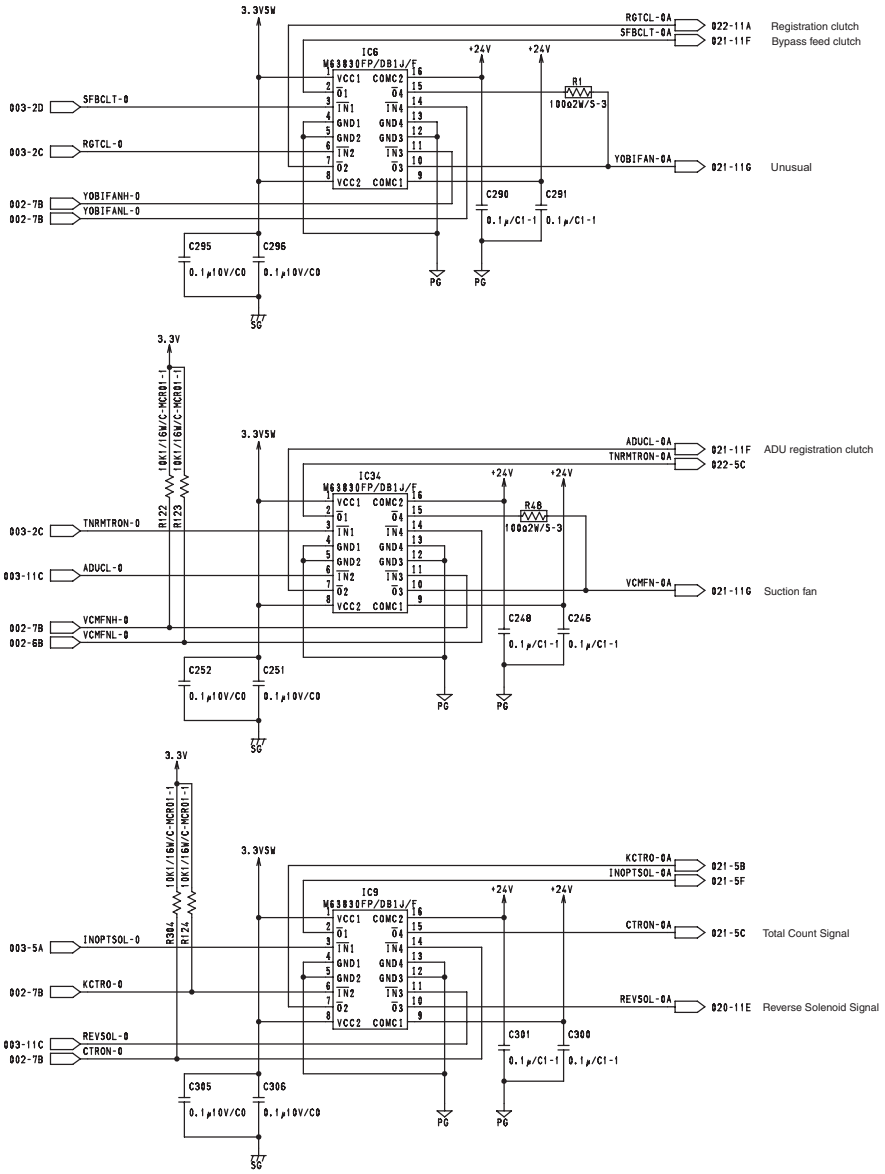
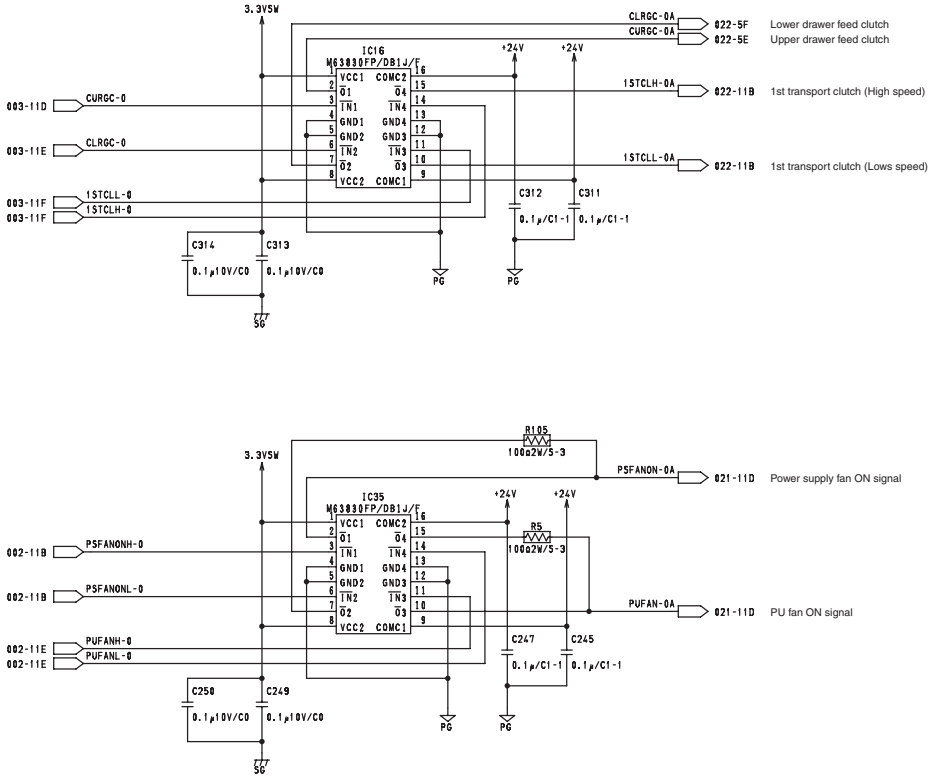
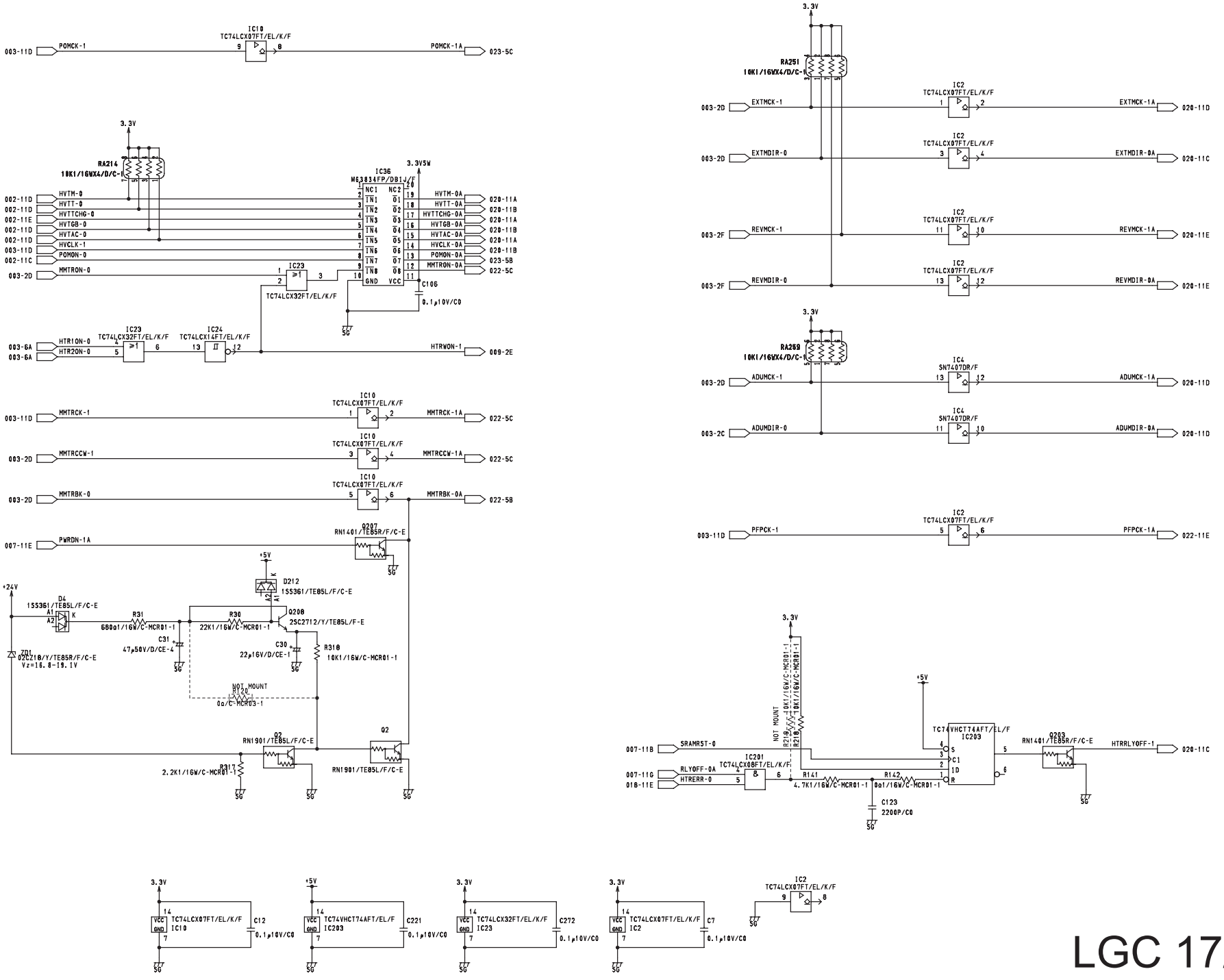
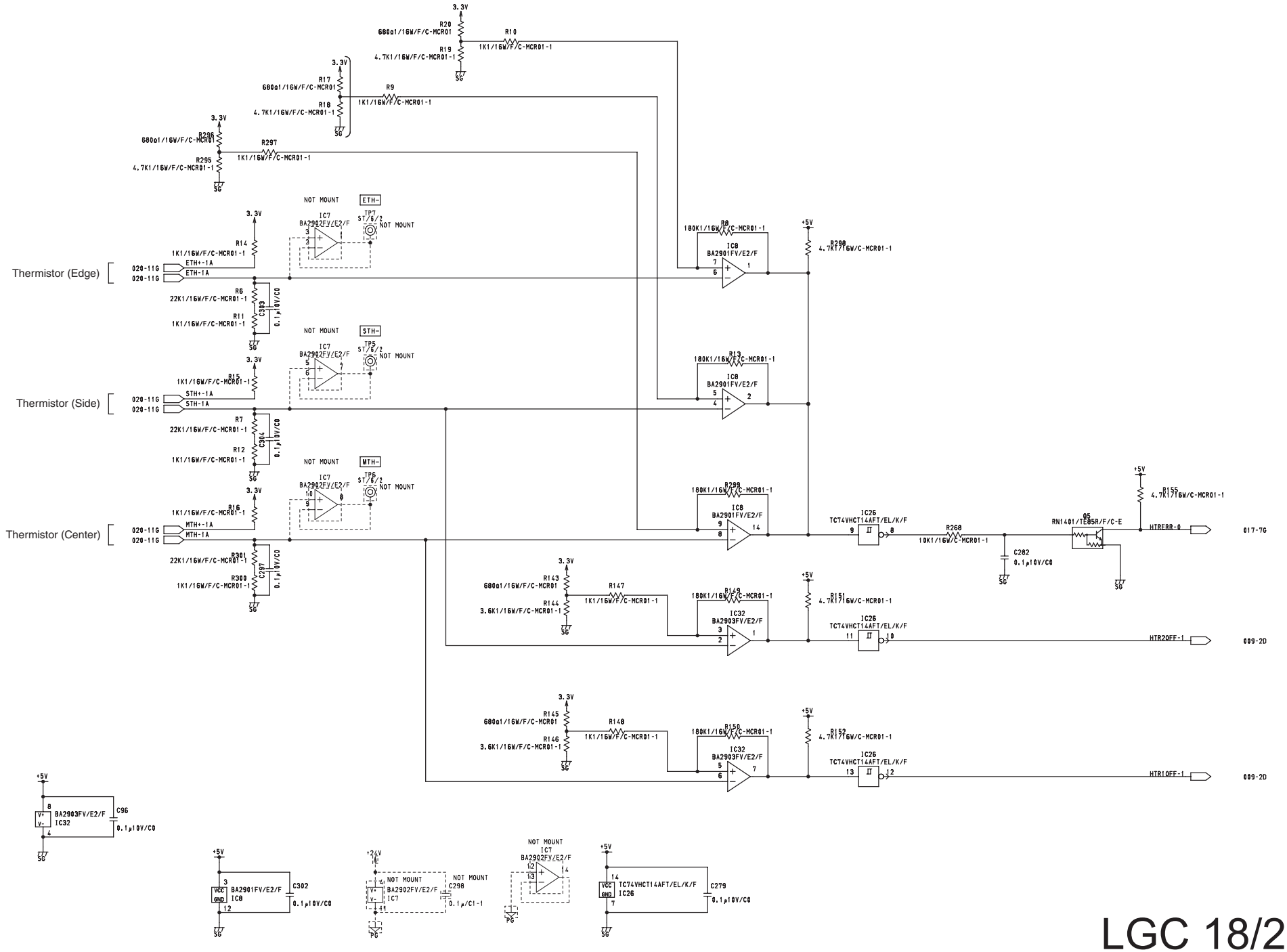


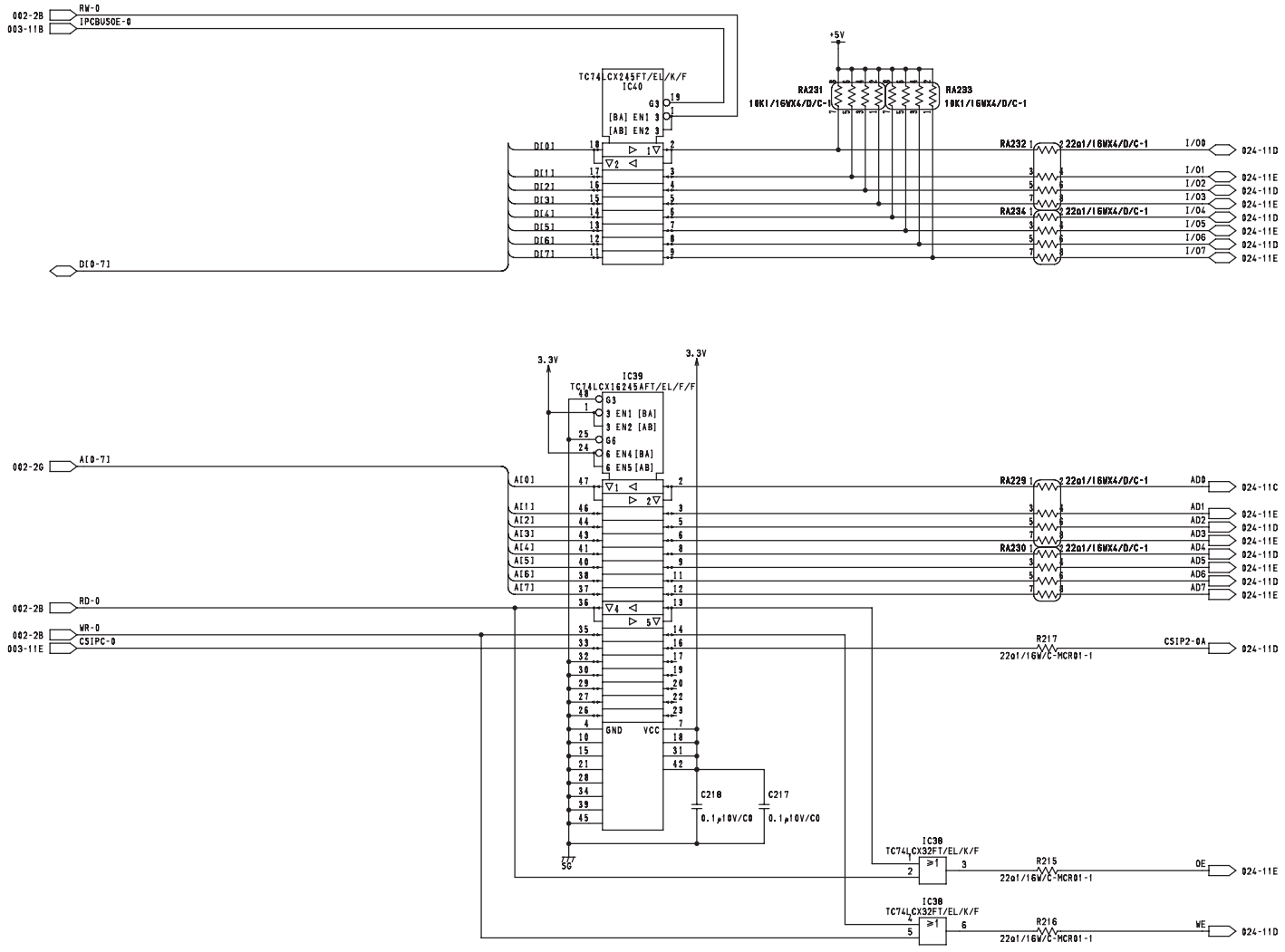

LGC 16/26

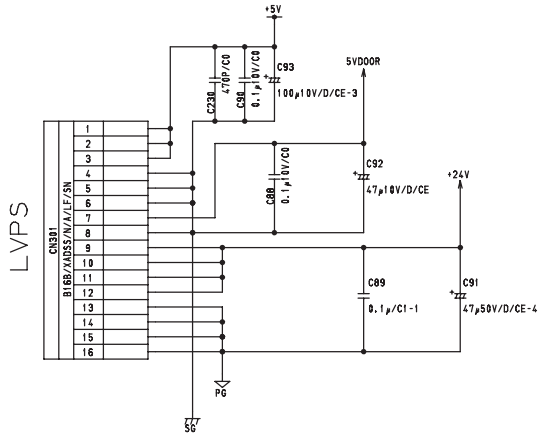


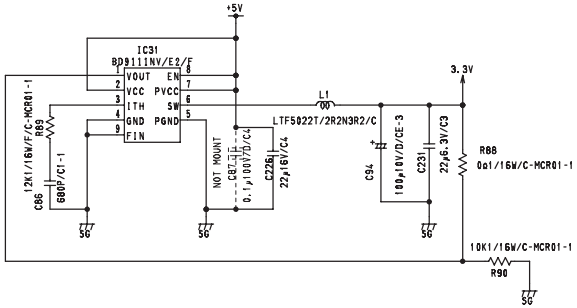

LGC 17/26

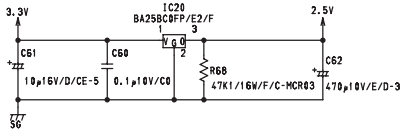


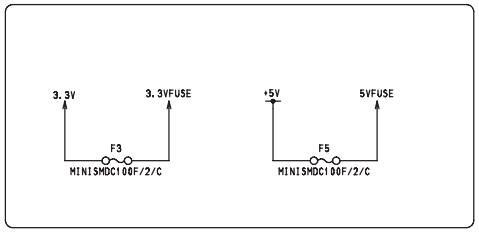

LGC 18/26

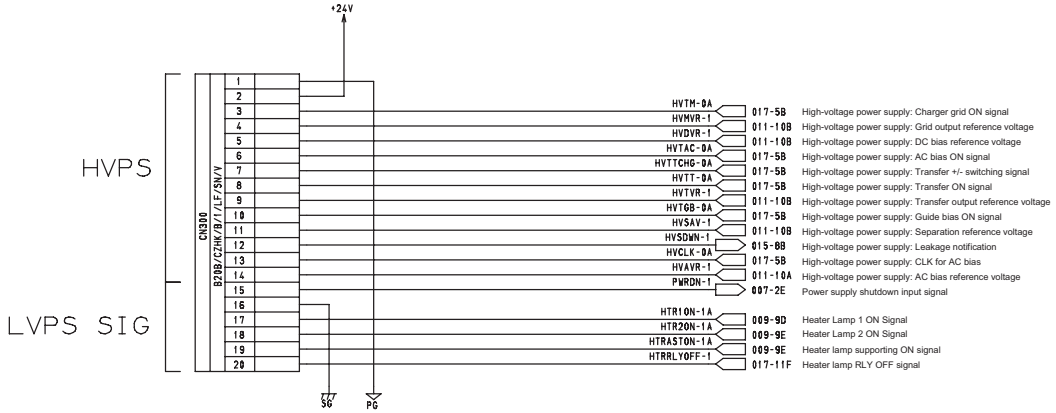


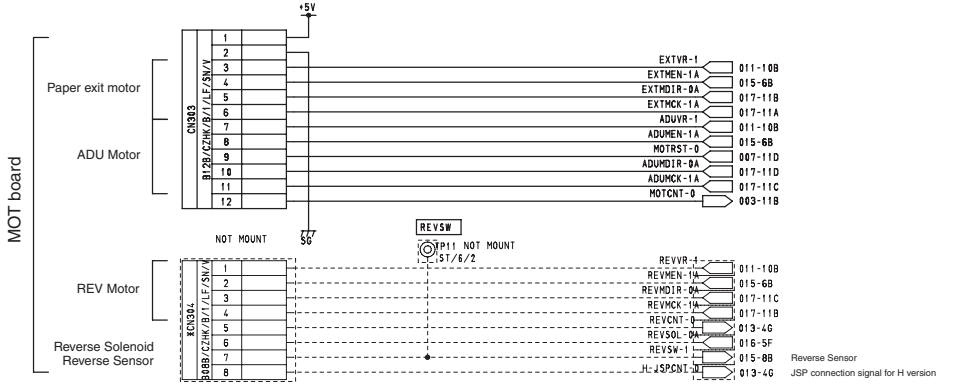


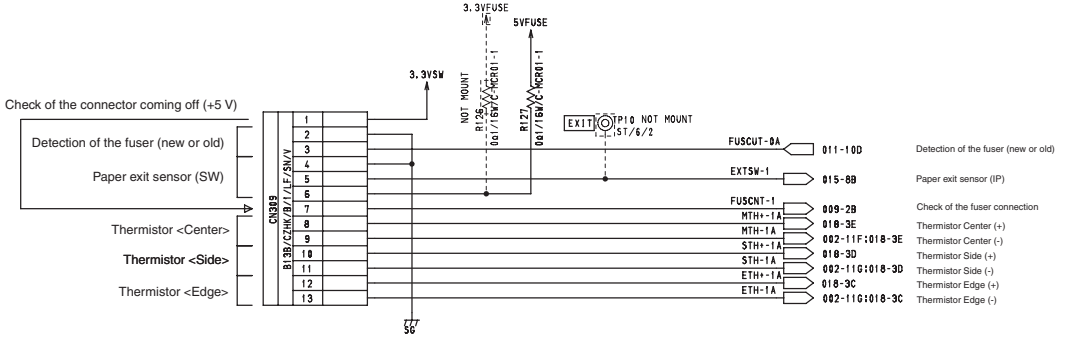



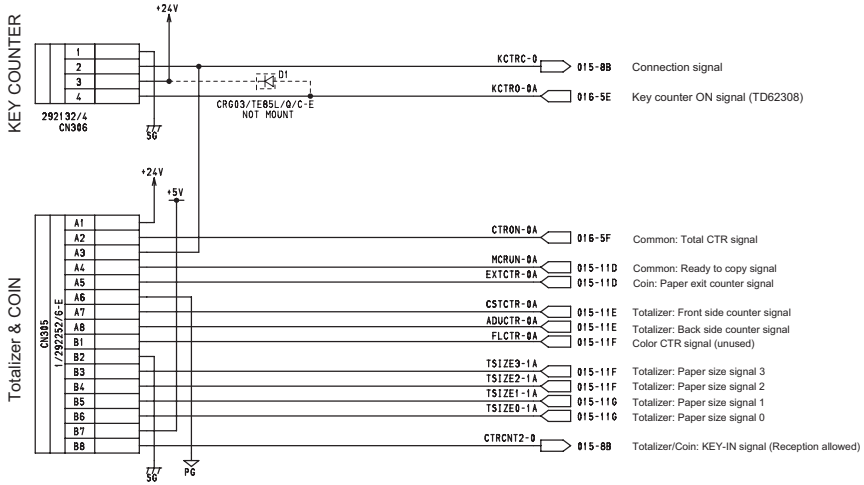



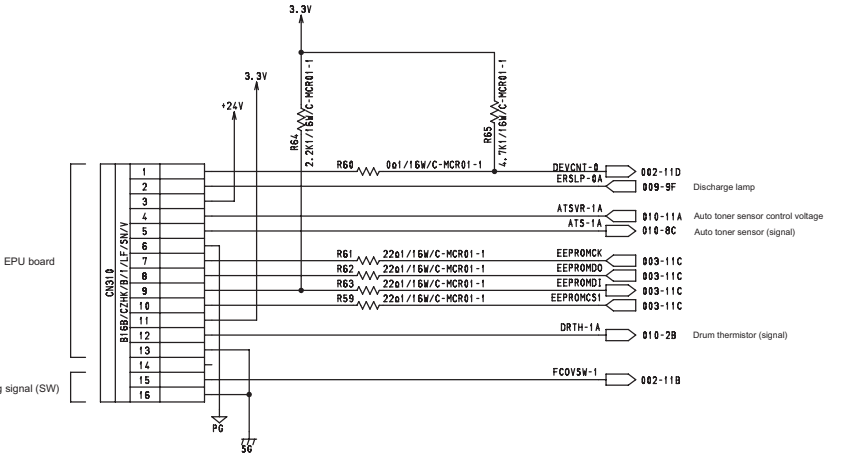



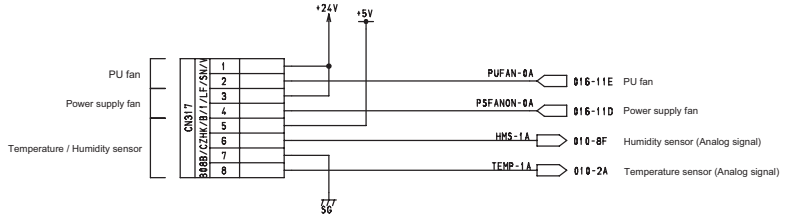



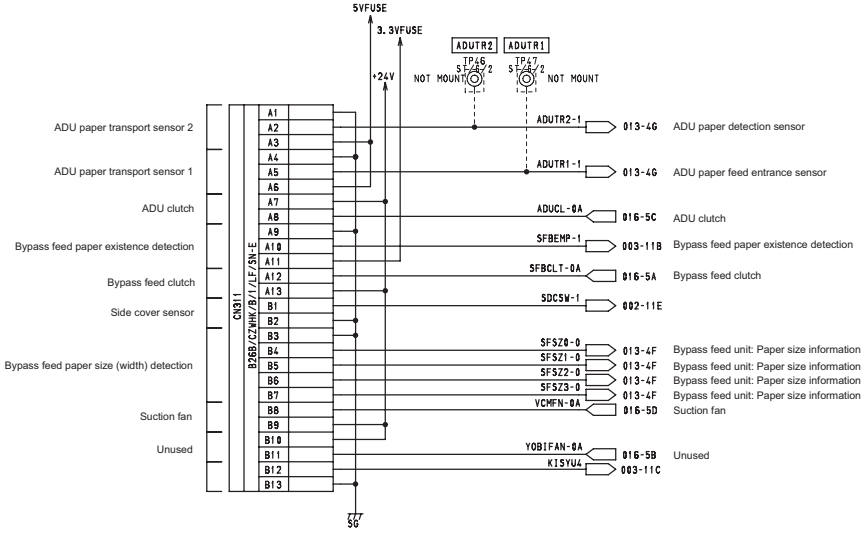




LGC 20/26

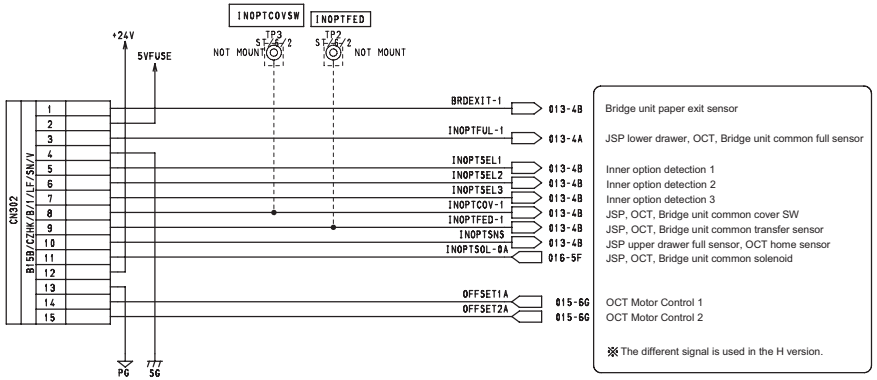


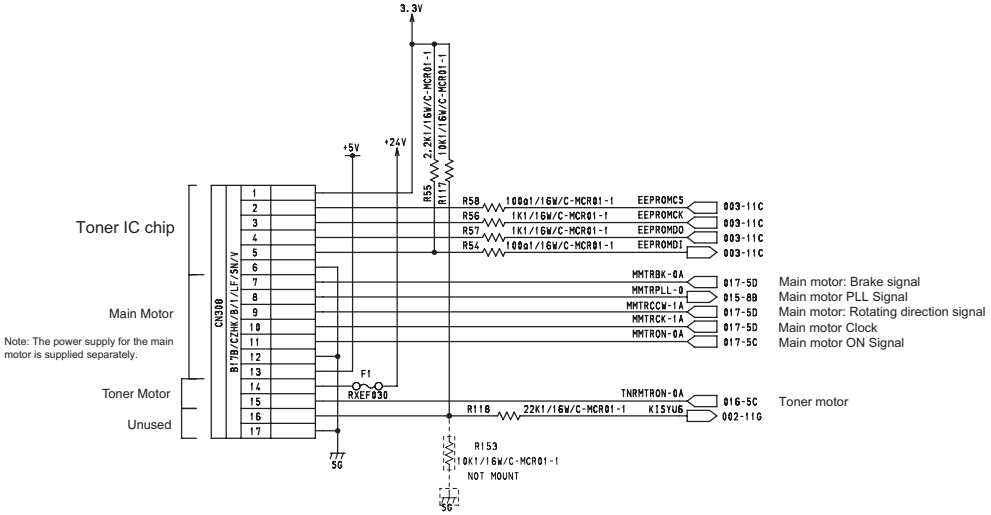



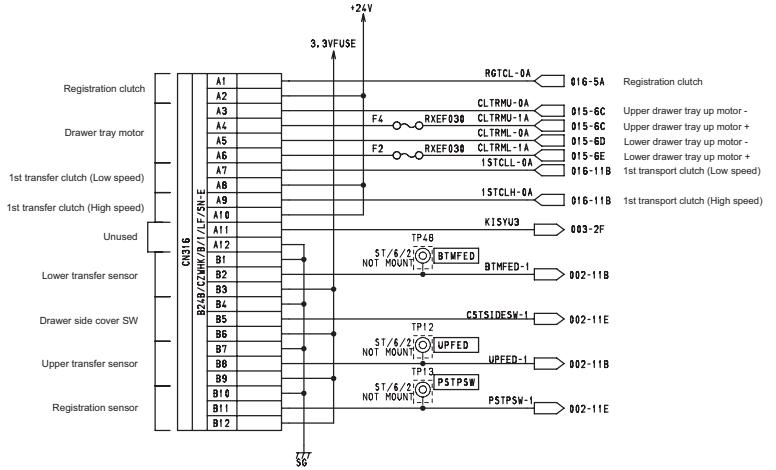



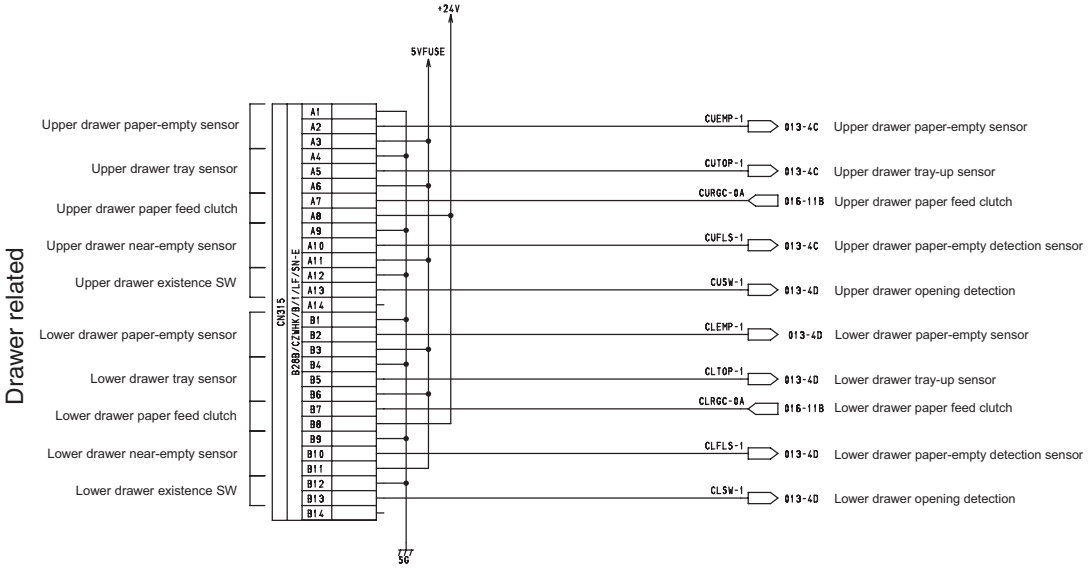



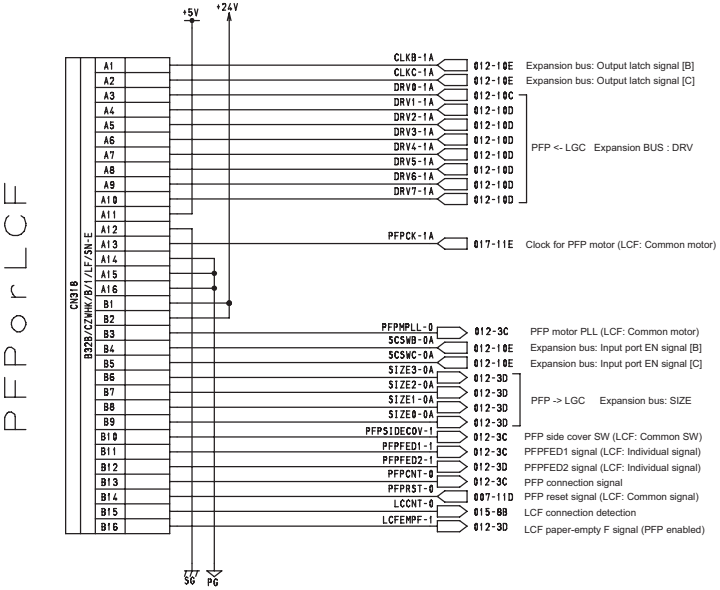

Common with the offset catch tray, bridge unit and job separator
(These in H version are connected on the MOT2 board.)



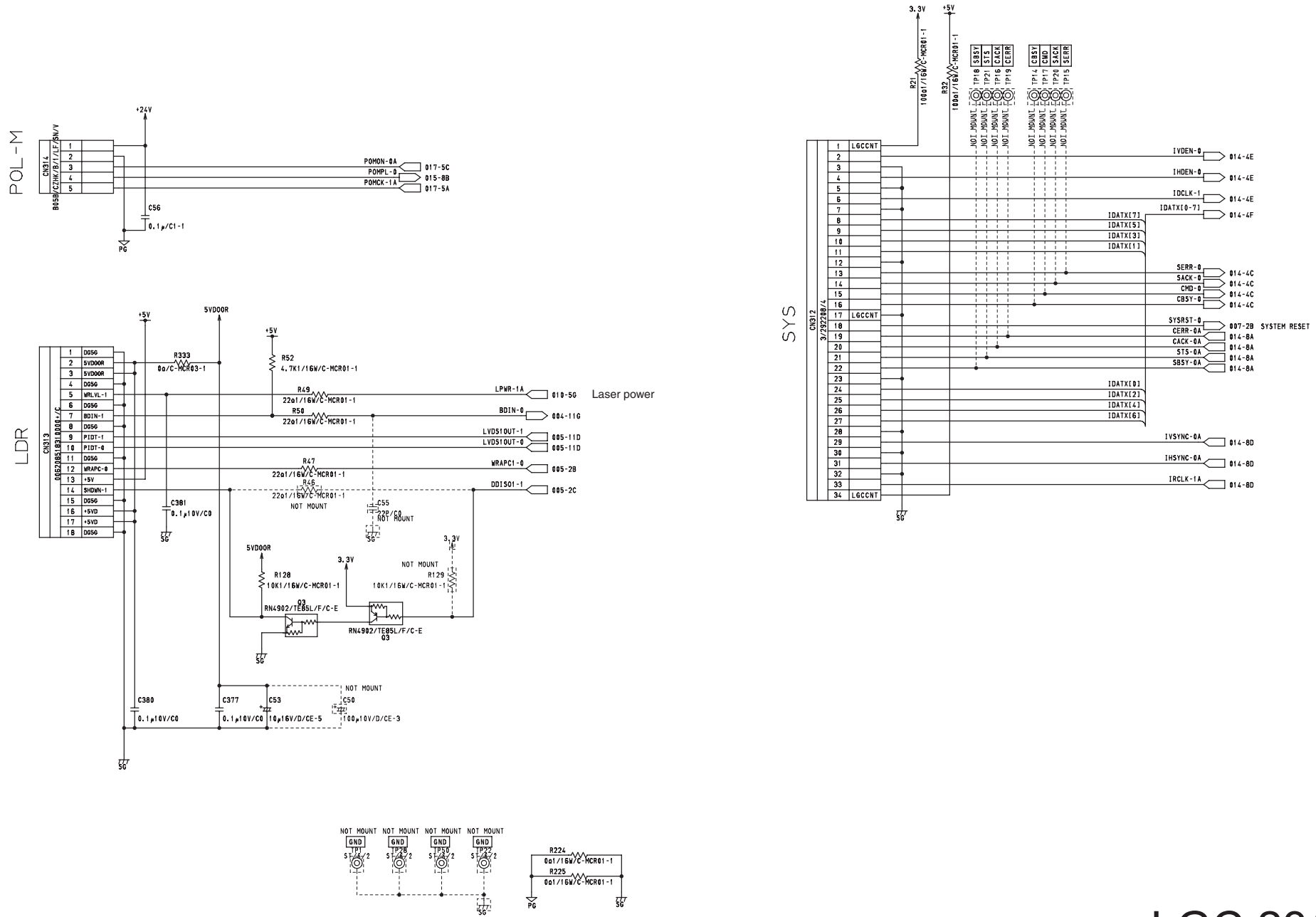


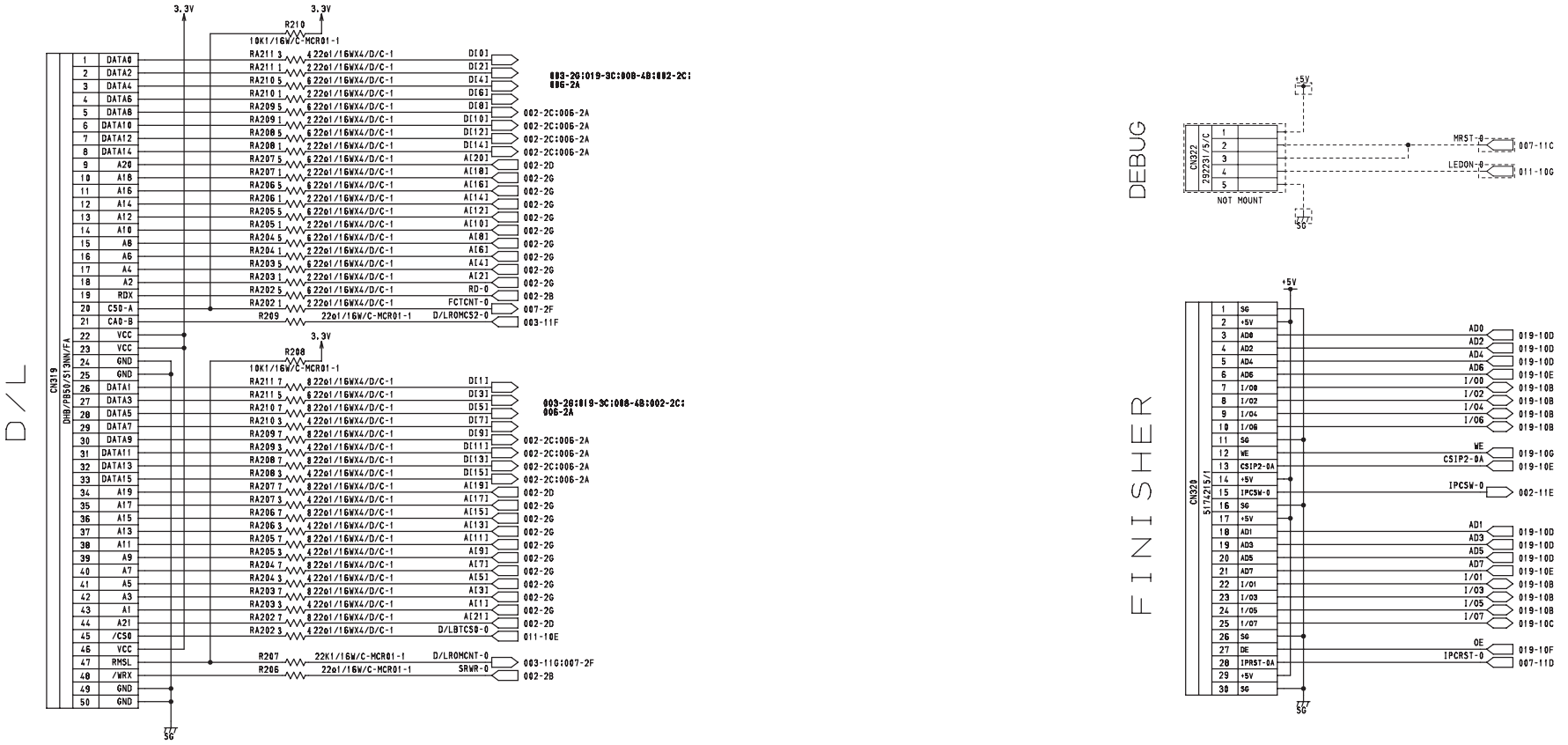



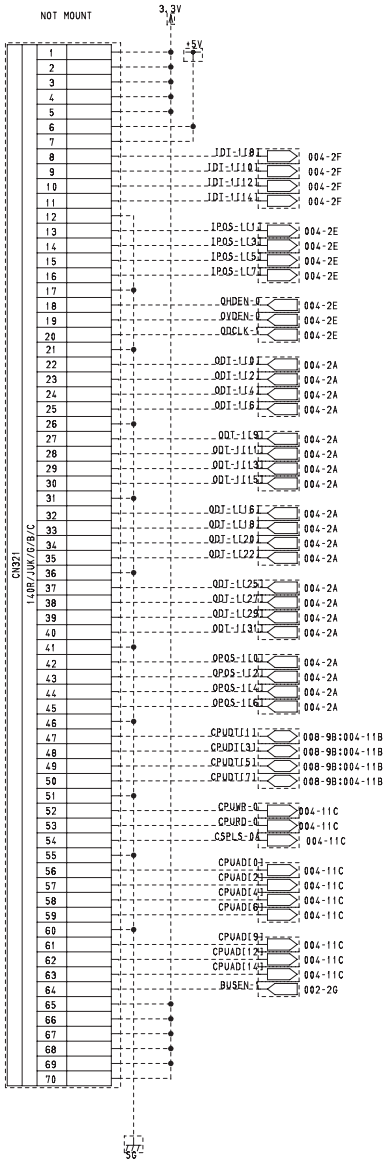



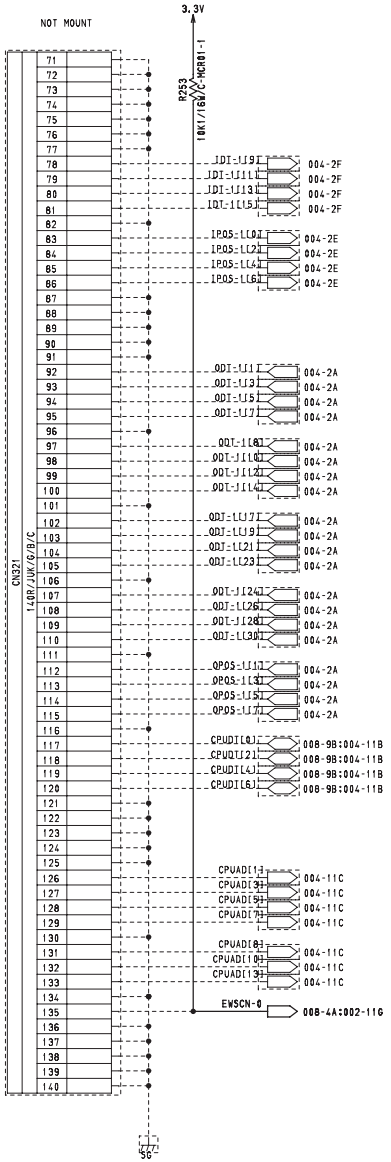

# LGC 22/26



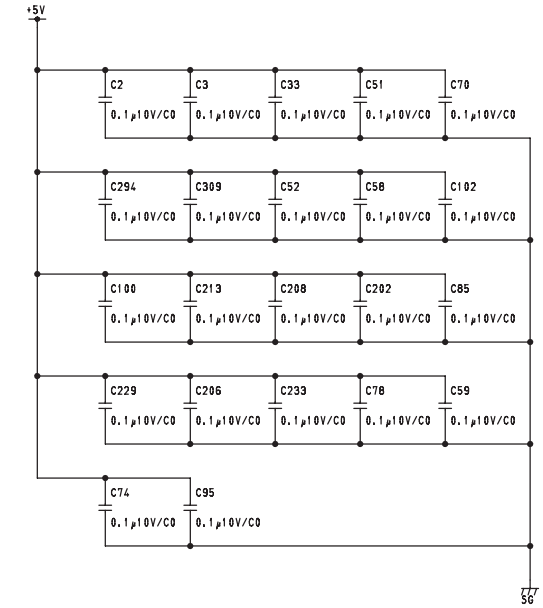


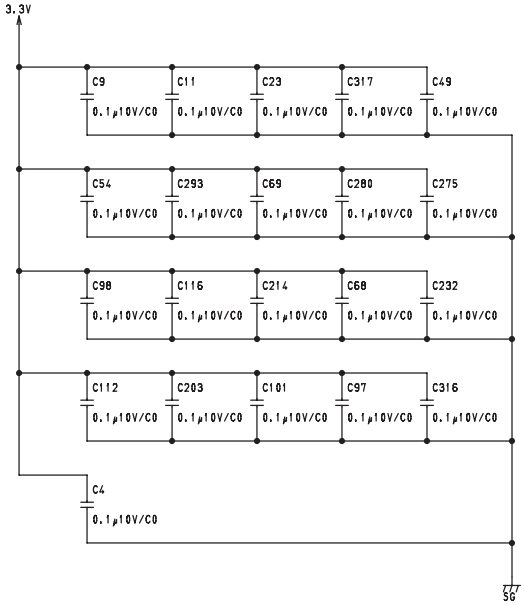
# EWS

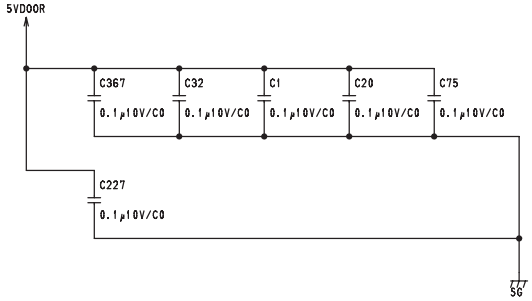


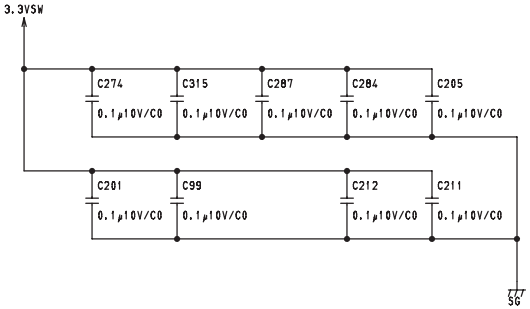




LGC 25/26

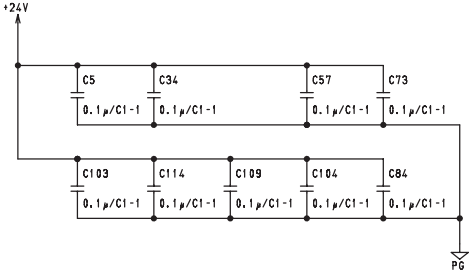




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LBL-LGC-470

%ZZ5
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LBL-LGC-471

NOT MOUNT

%ZZ6
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NOT MOUNT

%ZZ7
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NOT MOUNT

%ZZ8
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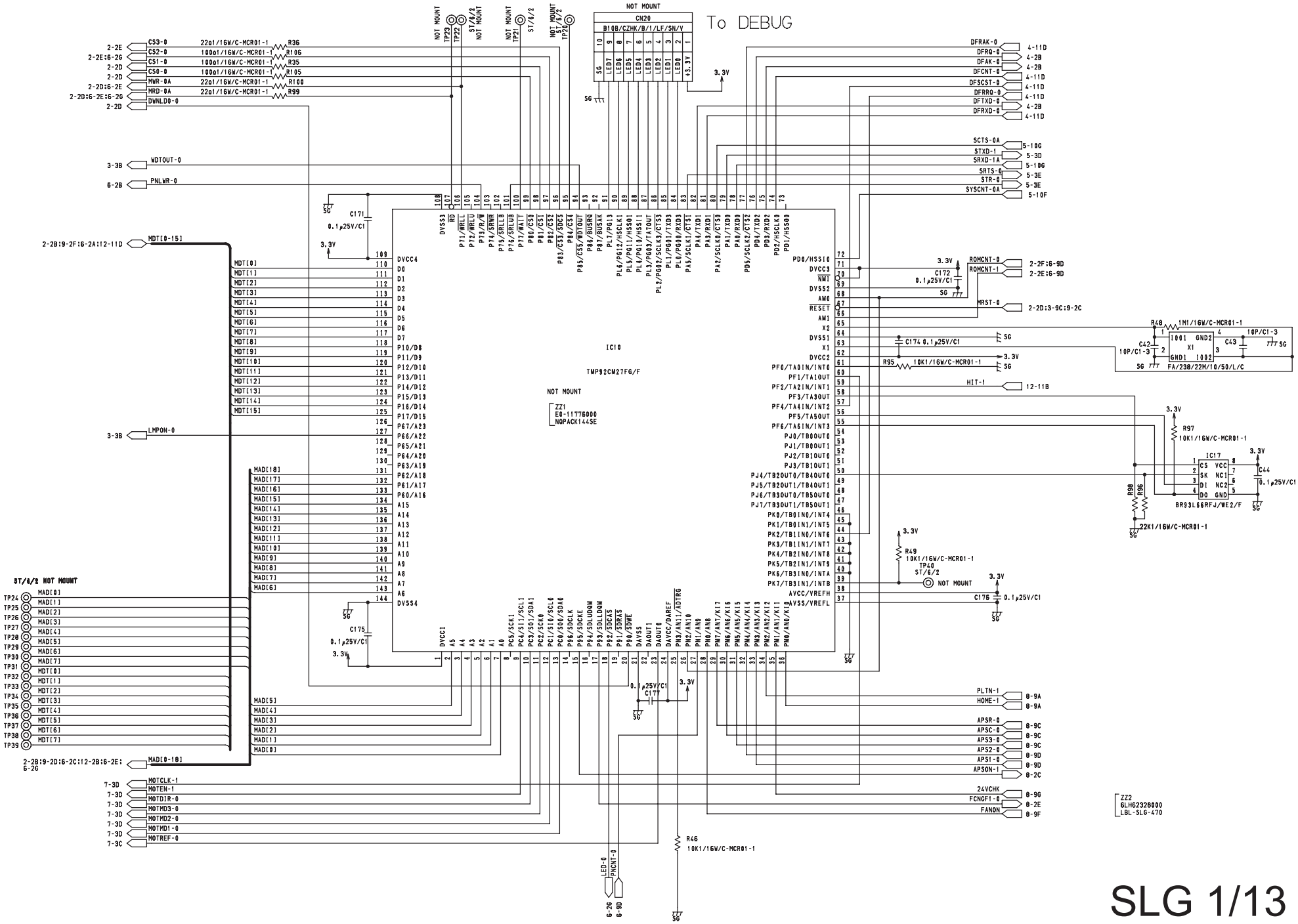
# LGC 26/26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B10B/CZHK/B/1/LF/SN/V
IC10
TMP92CM27FG/F
NOT MOUNT
ZZ1
E0-11776000
NQPACK144SE
ST/6/2 NOT MOUNT
R36
R106
R35
R105
R100
R99
R46
10K1/16W/C-MCR01-1
R49
R97
R98
R96
22K1/16W/C-MCR01-1
R48
1M1/16W/C-MCR01-1
R95
C171
C172
C174
C175
C176
C177
C42
C43
C44
10P/C1-3
0.1μ25V/C1
X1
FA/230/22M/10/50/L/C
IC17
BR93L66RFJ/WE2/F
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12-11B
ZZ2
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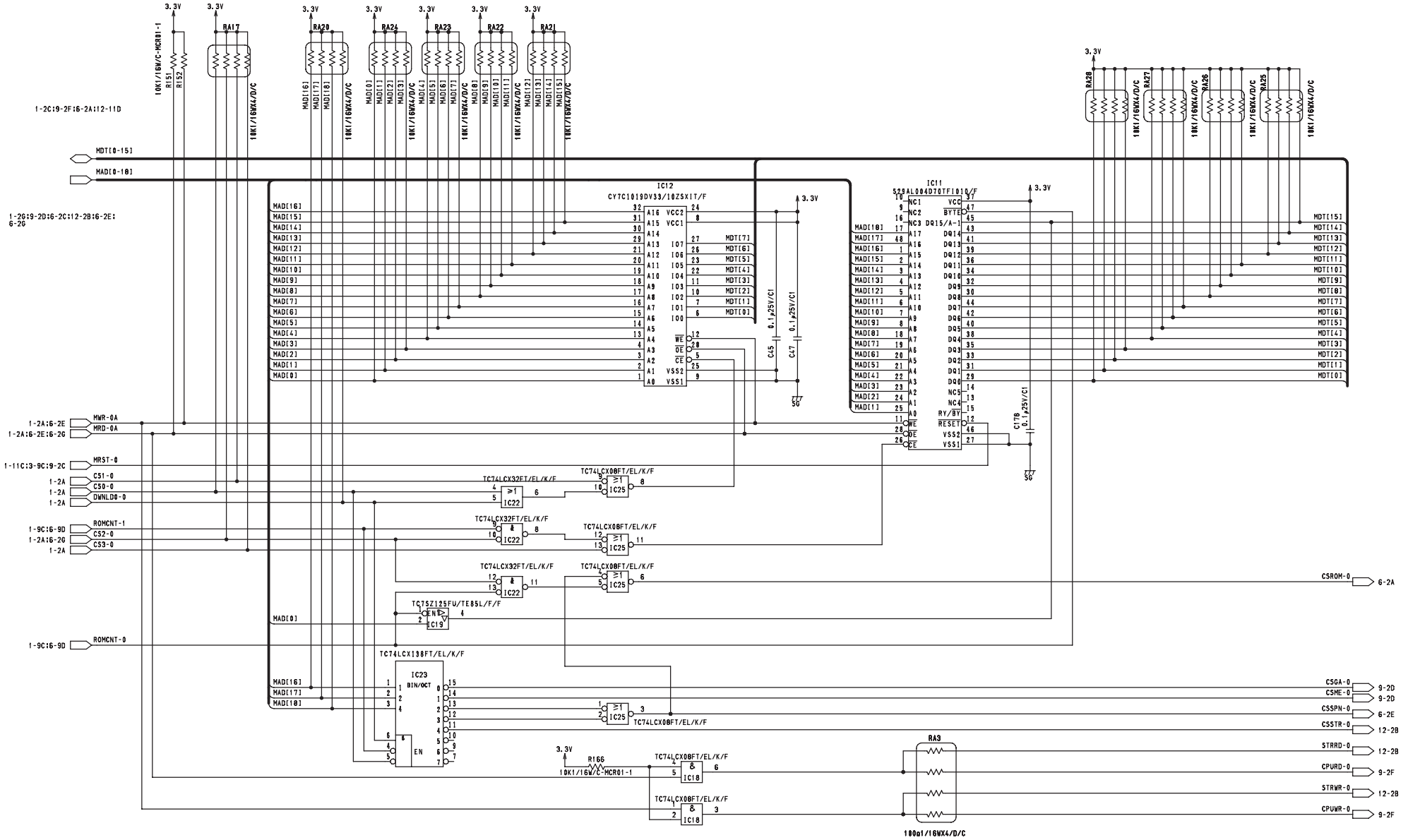
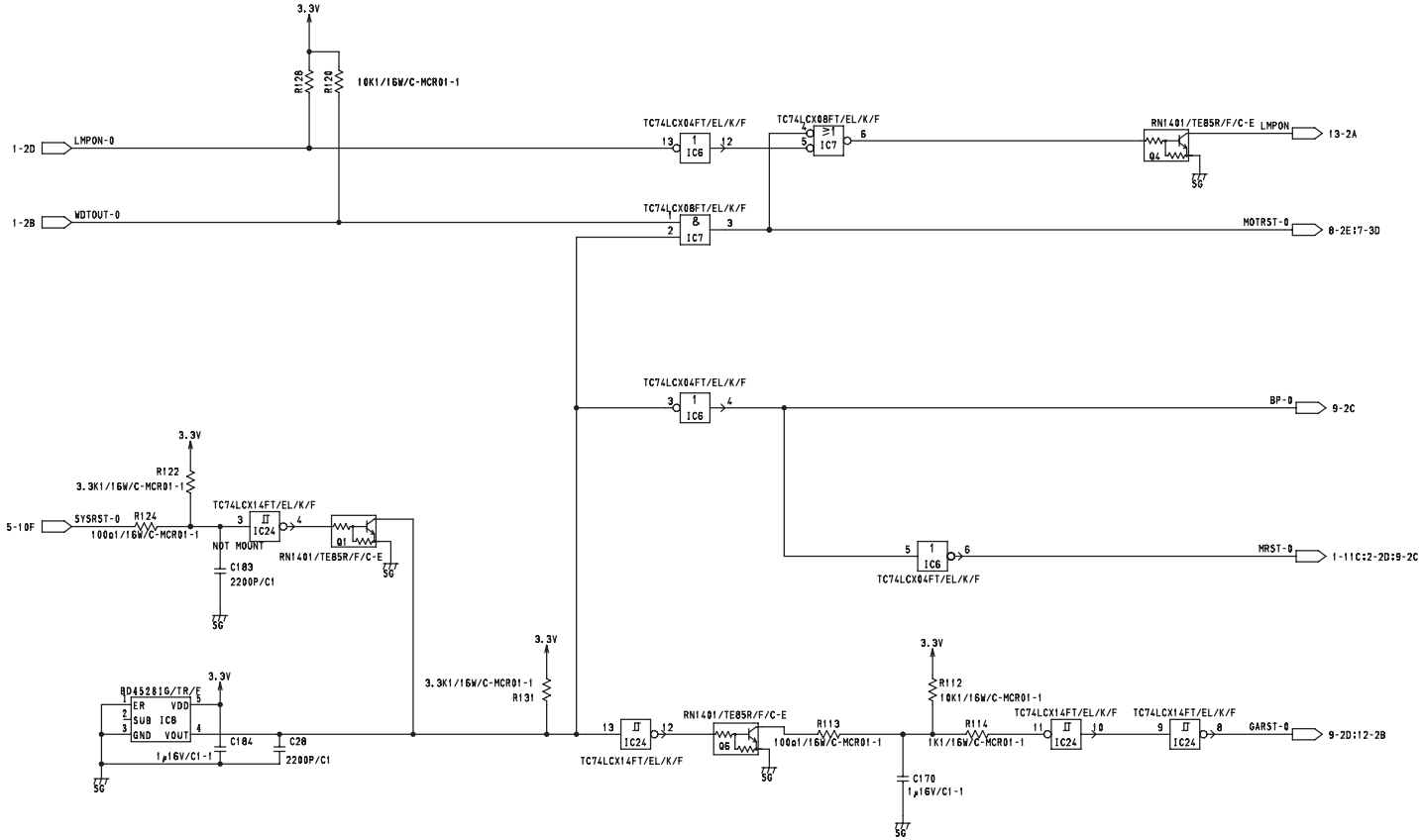
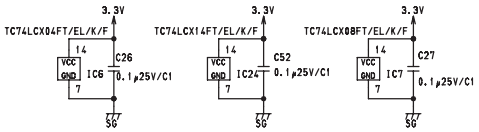
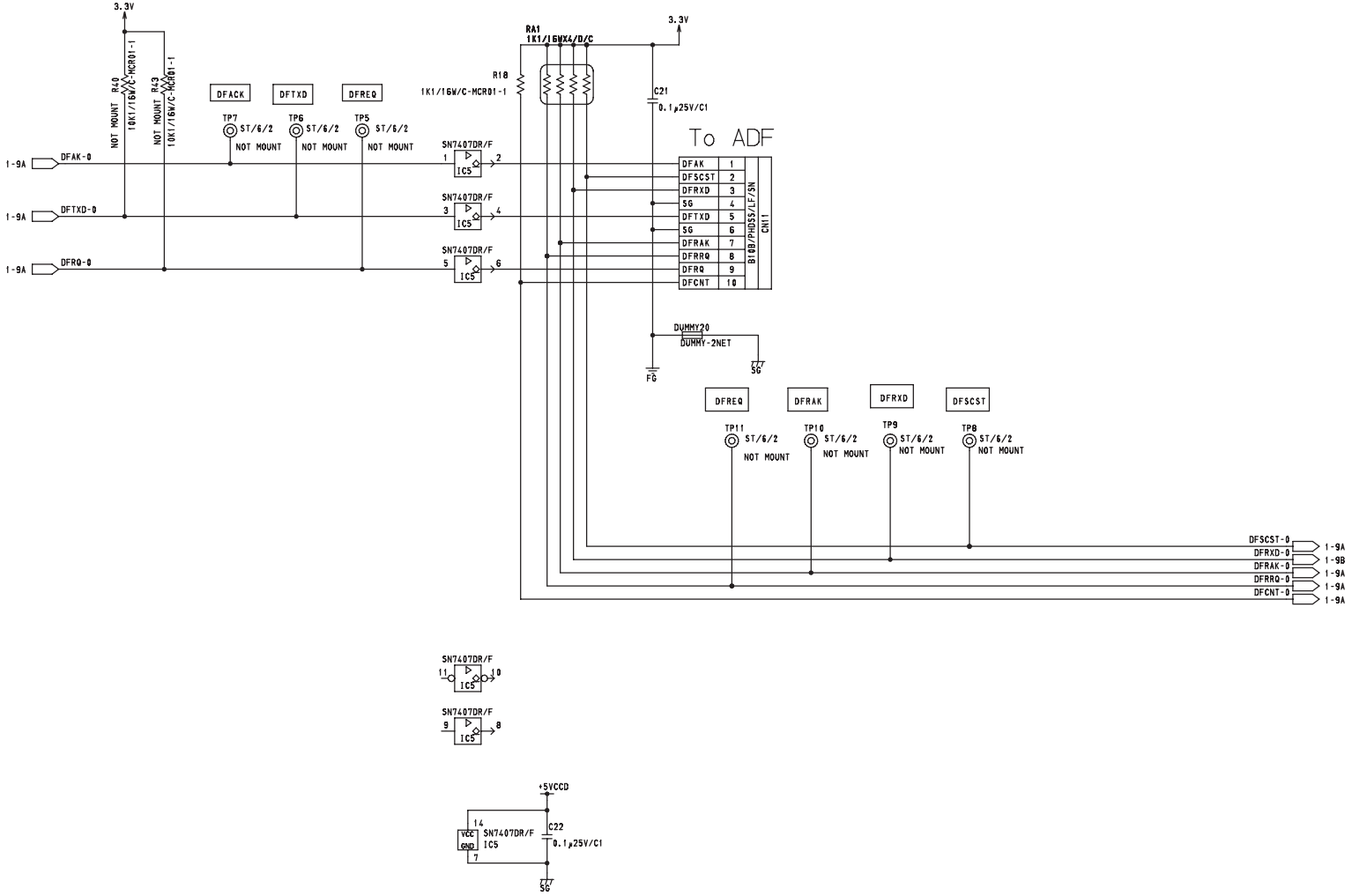
LBL-5LG-470
SLG 1/13
WWW.SERVICE-MANUAL.NET



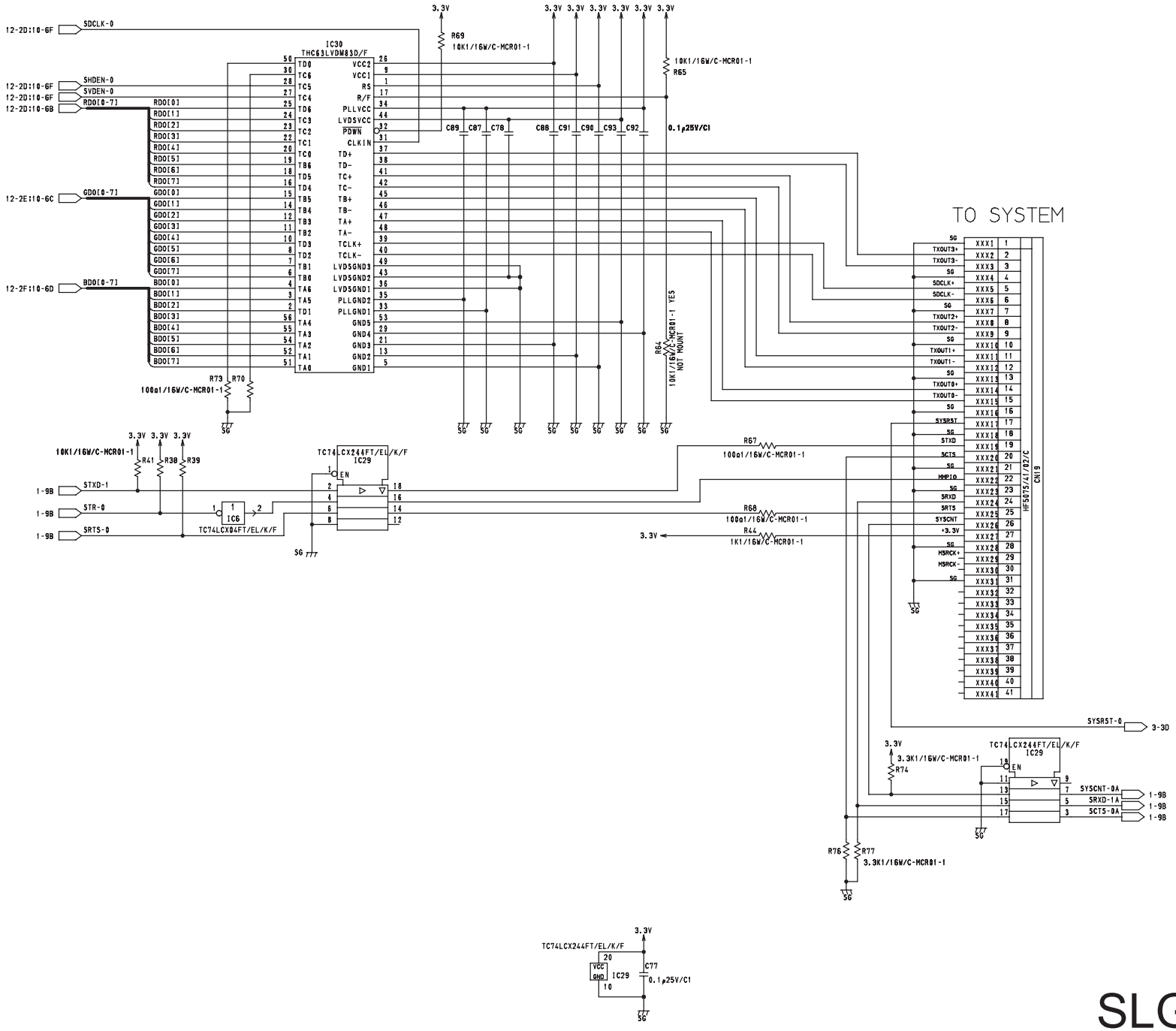

SLG 2/13



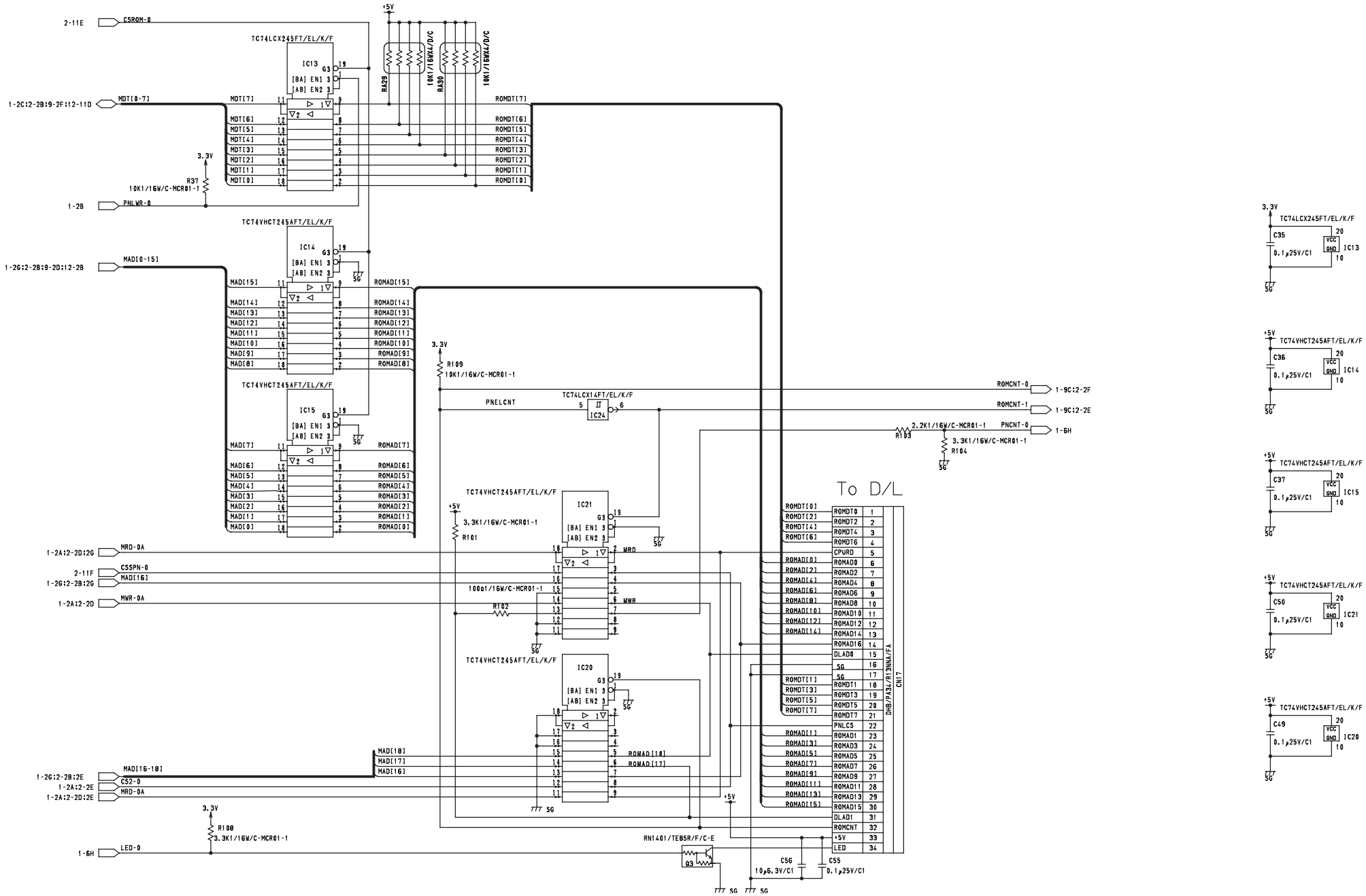





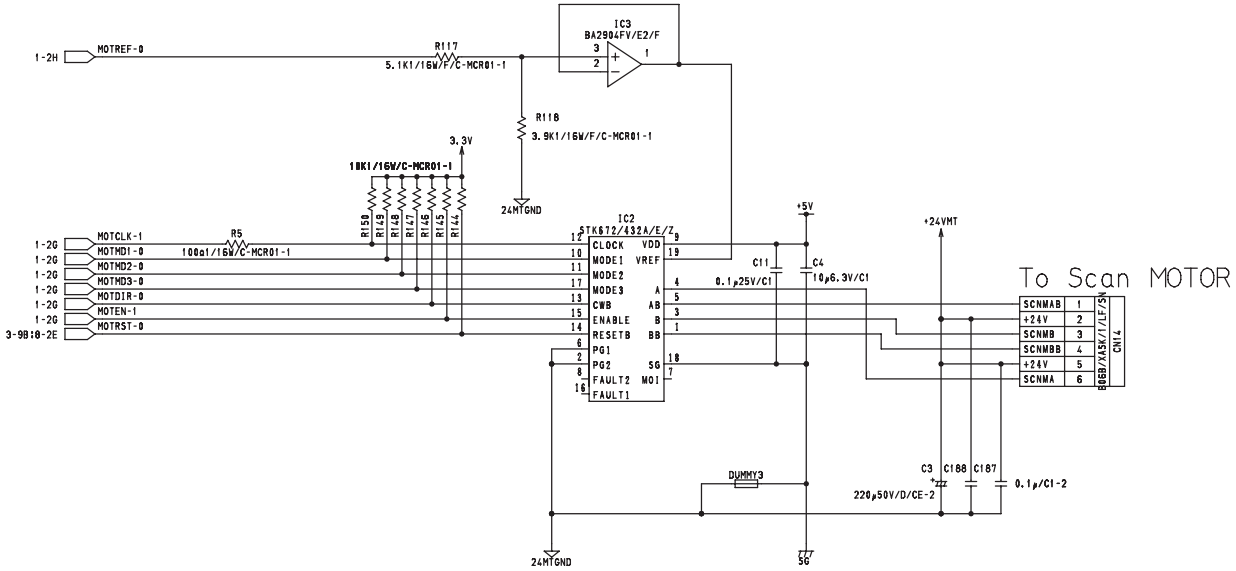

SLG 4/13

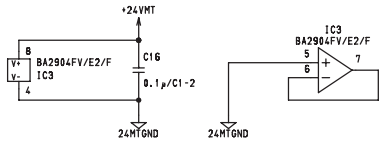



SLG 5/13

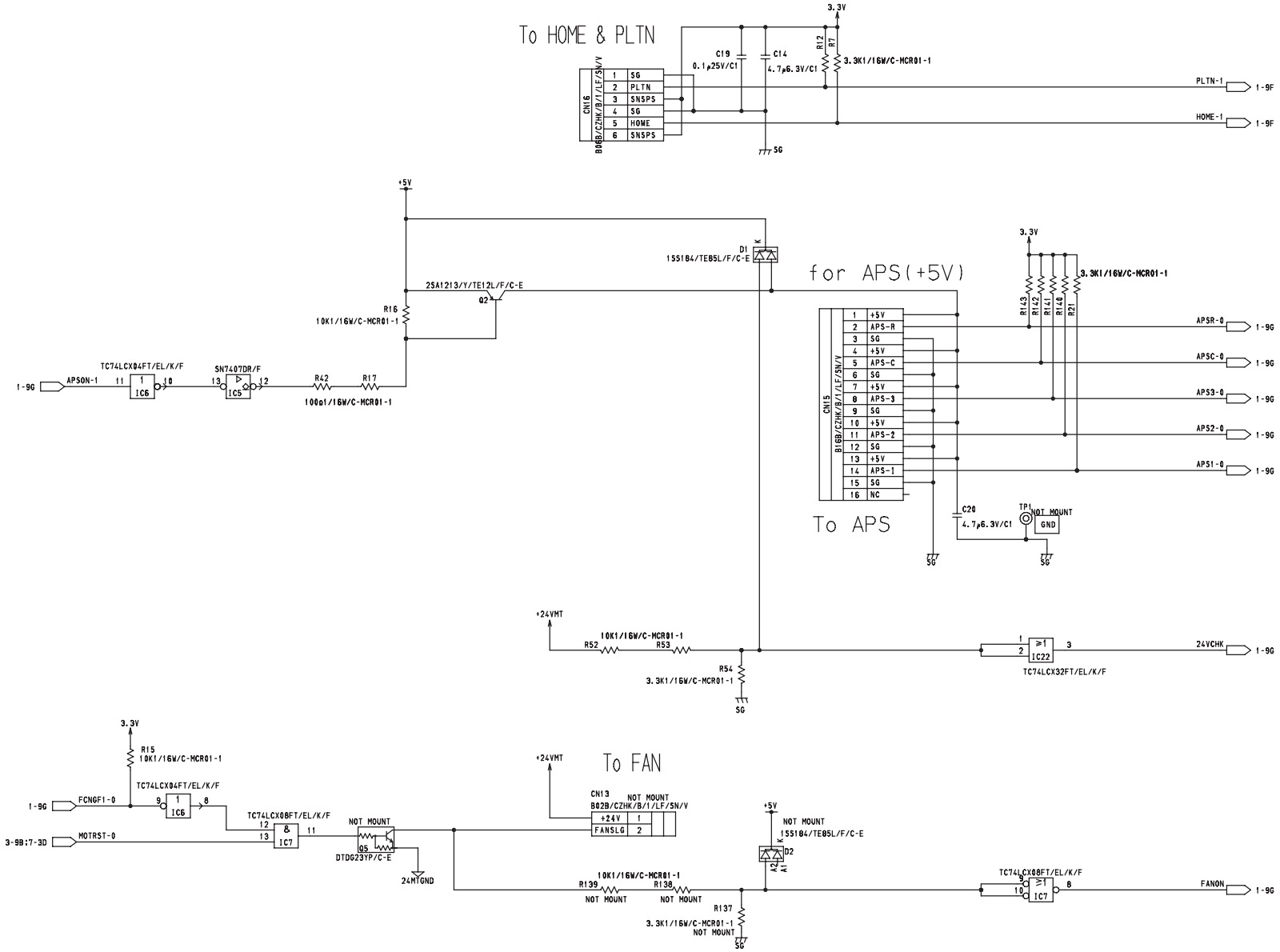



SLG 6/13

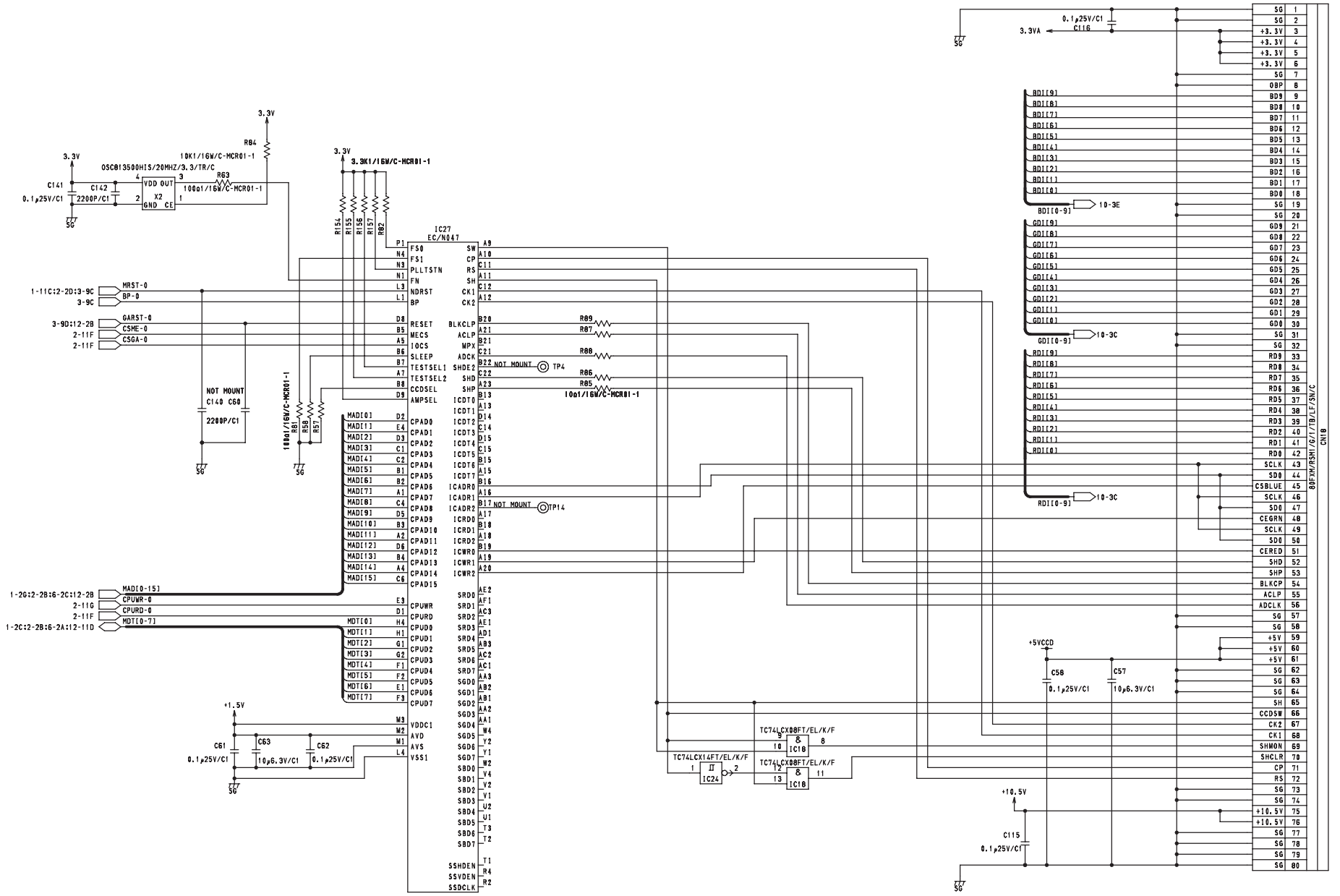


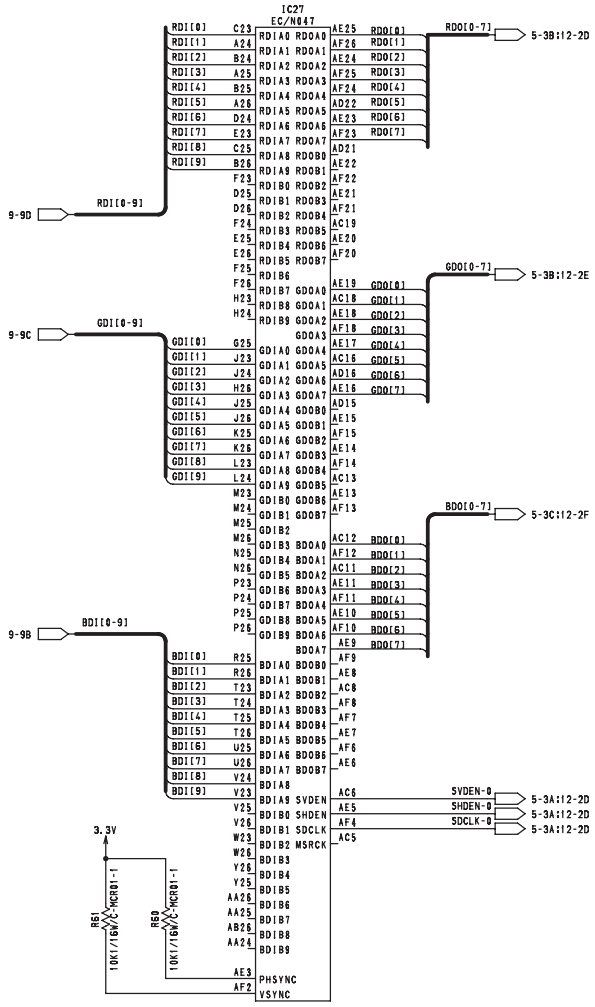

SLG 7/13

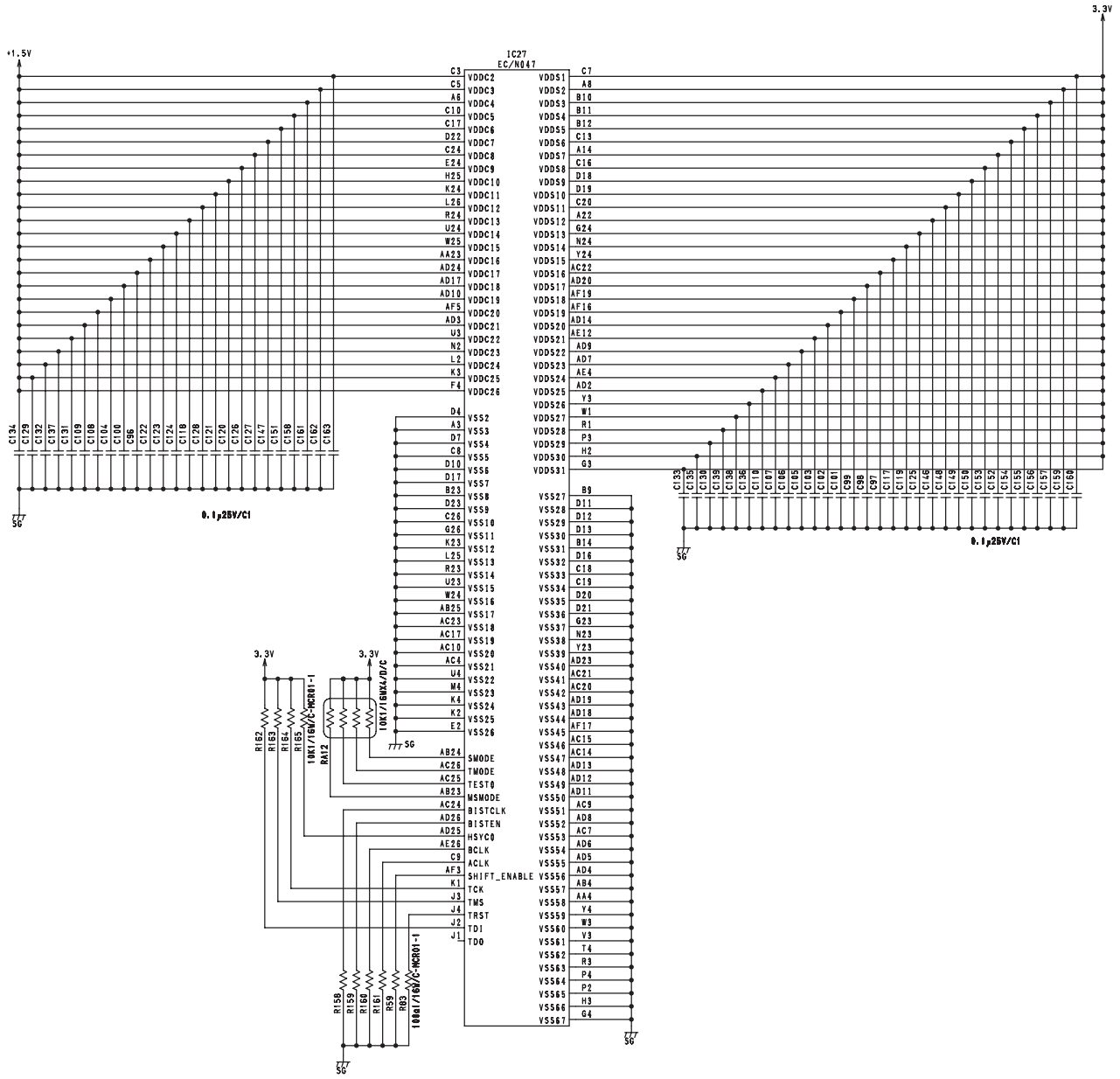



SLG 8/13

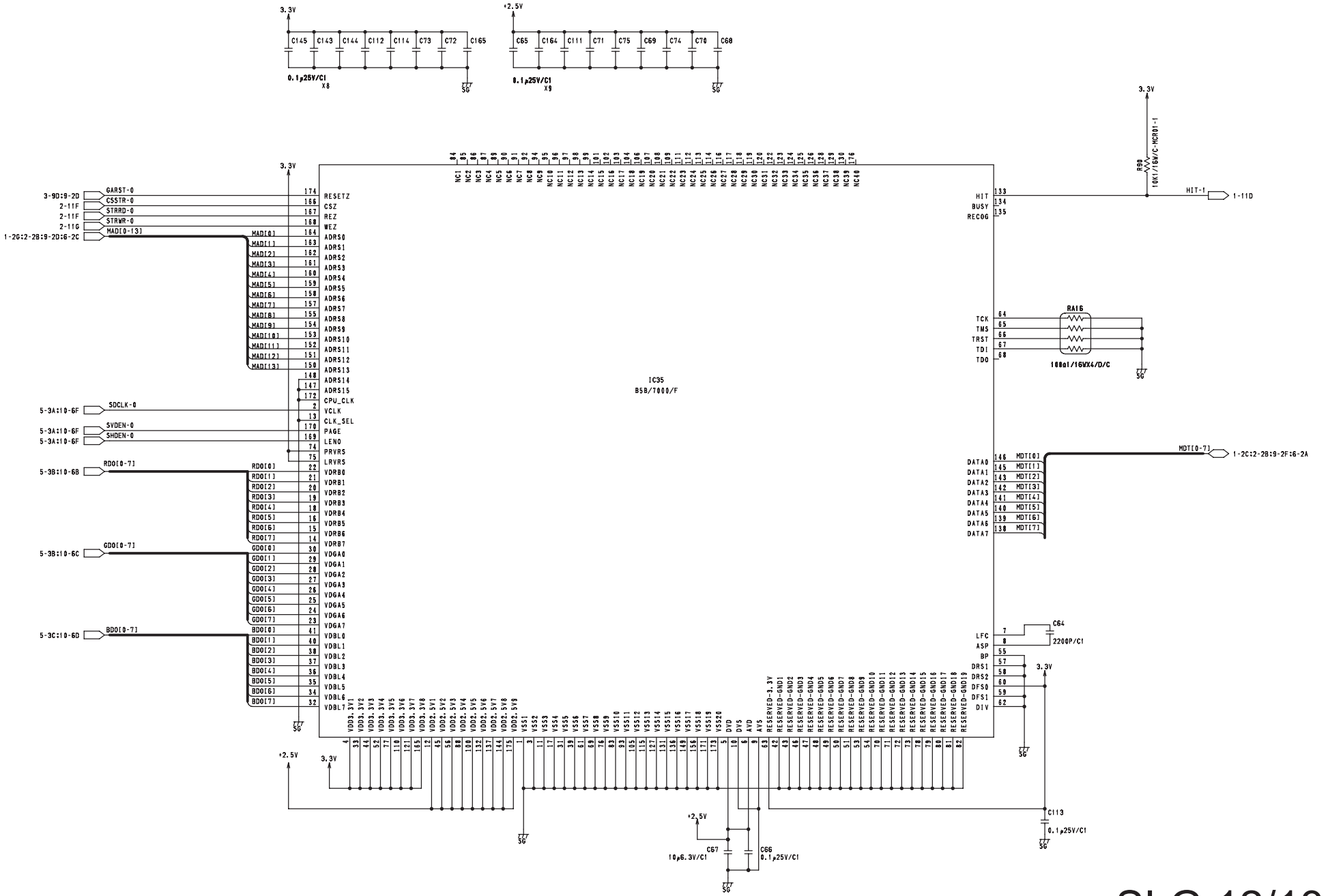



SLG 9/13

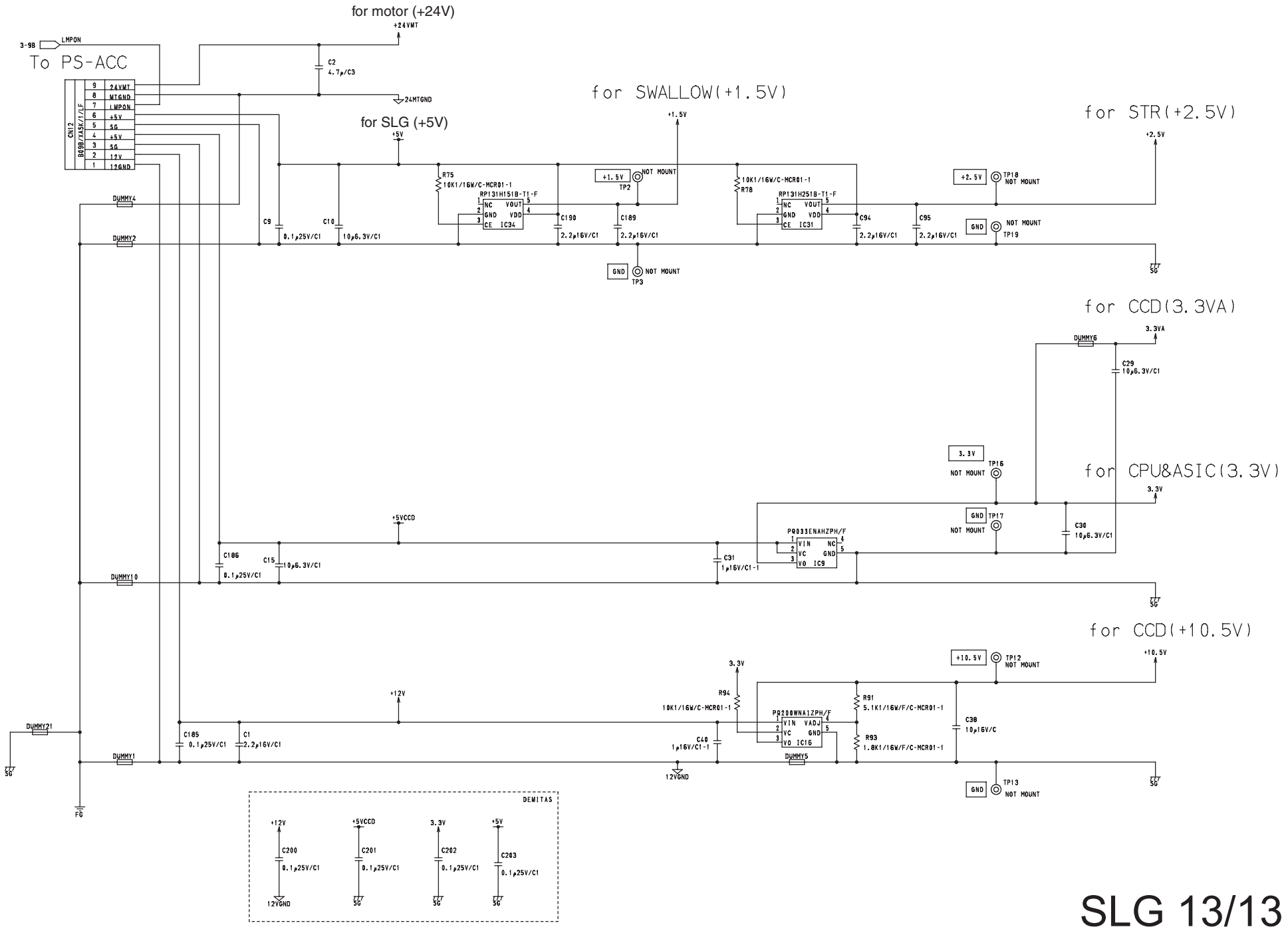




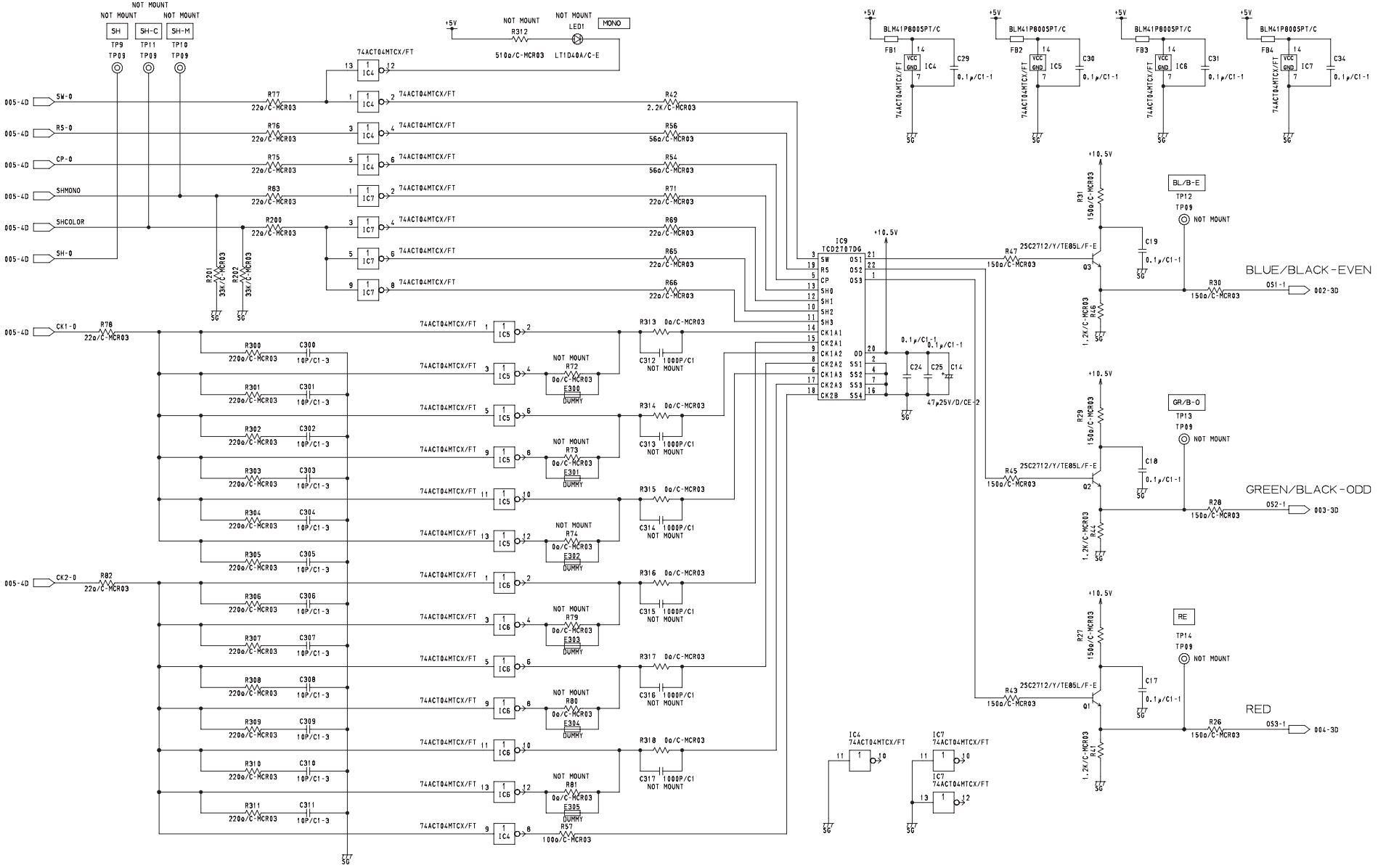

SLG 11/13



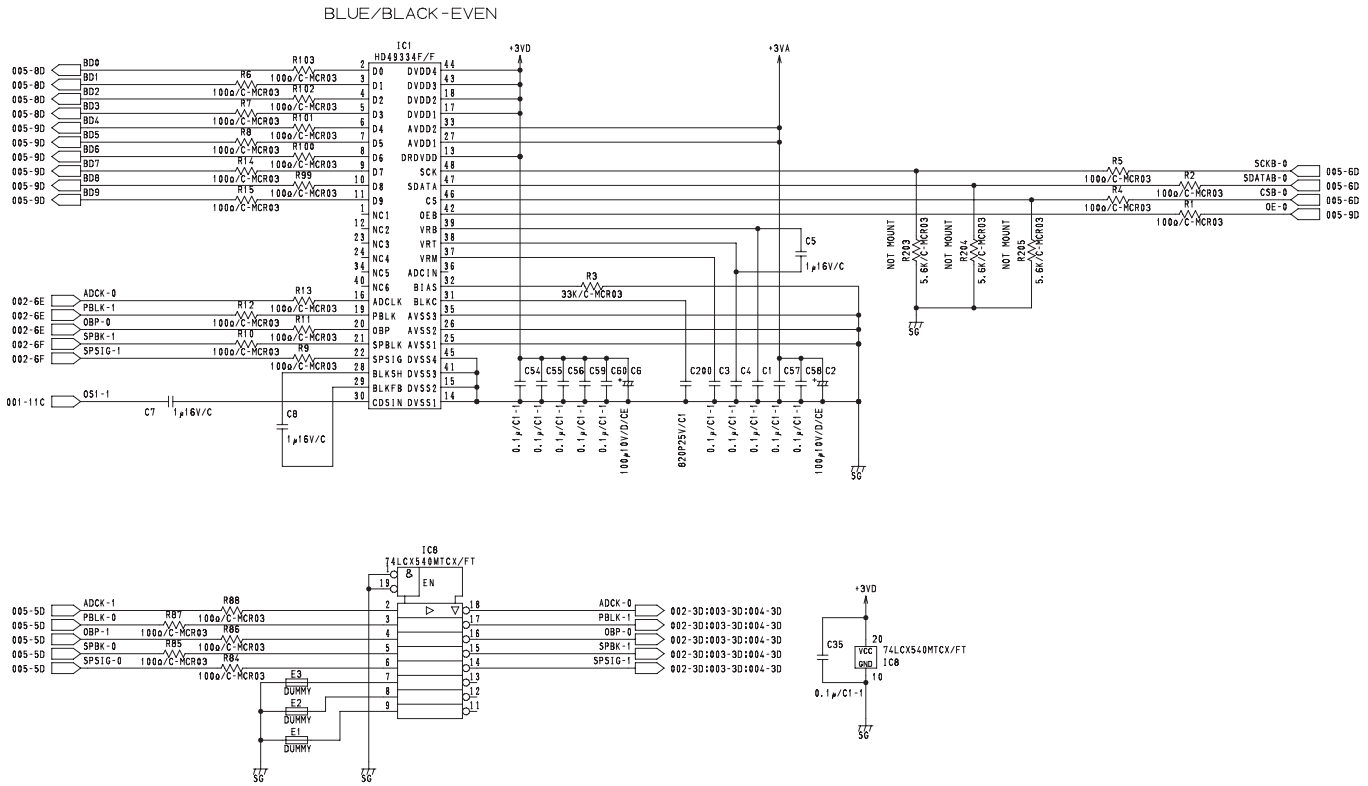

SLG 12/13



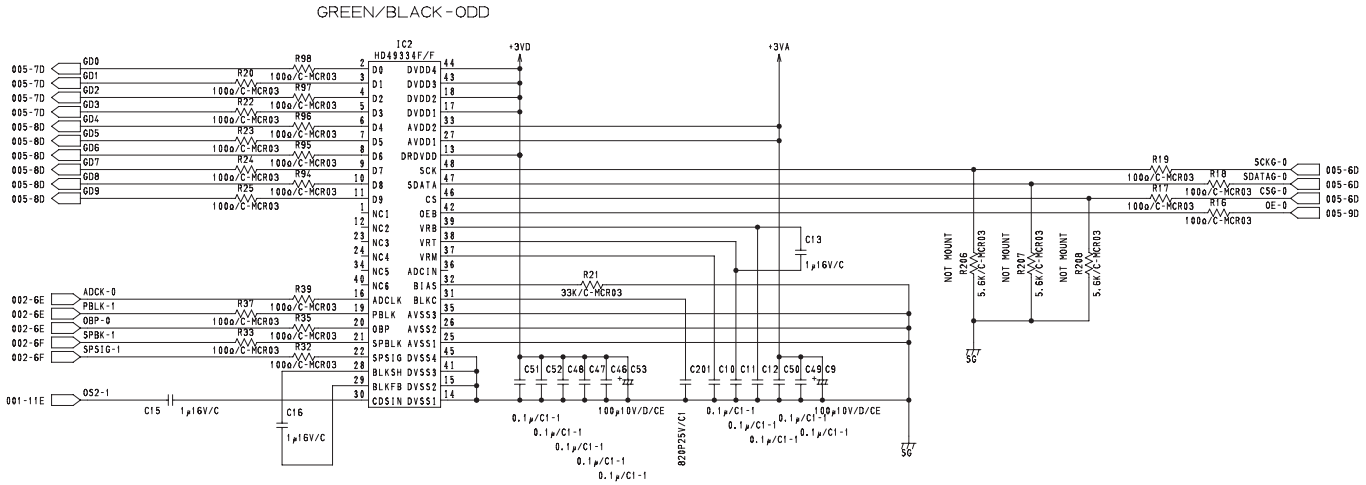

# SLG 13/13



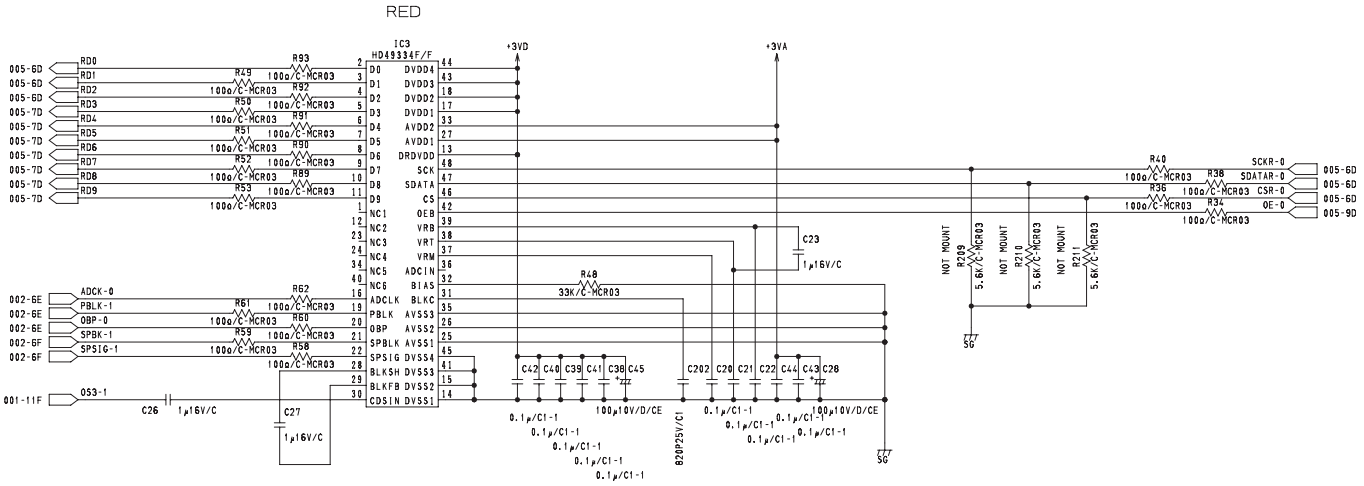

CCD 1/5



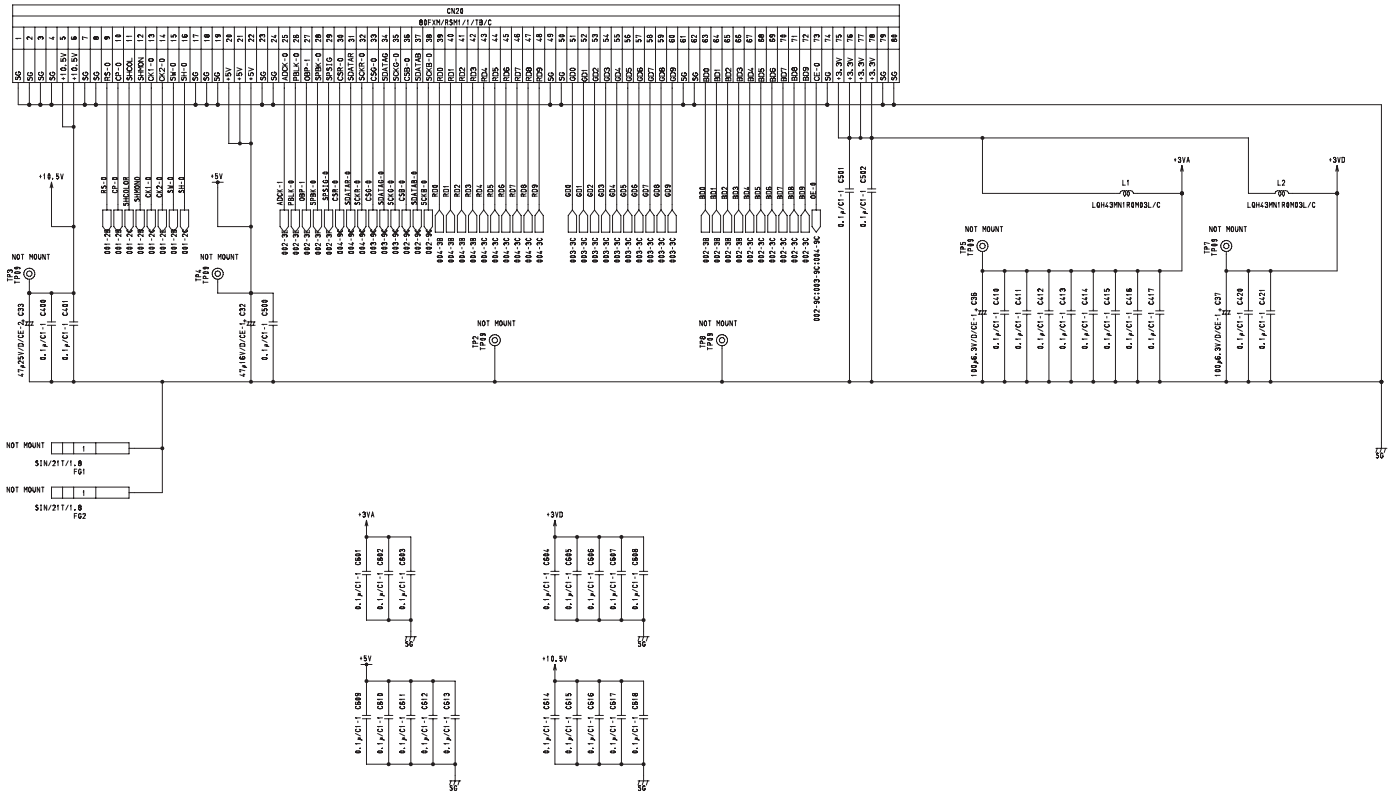

CCD 2/5



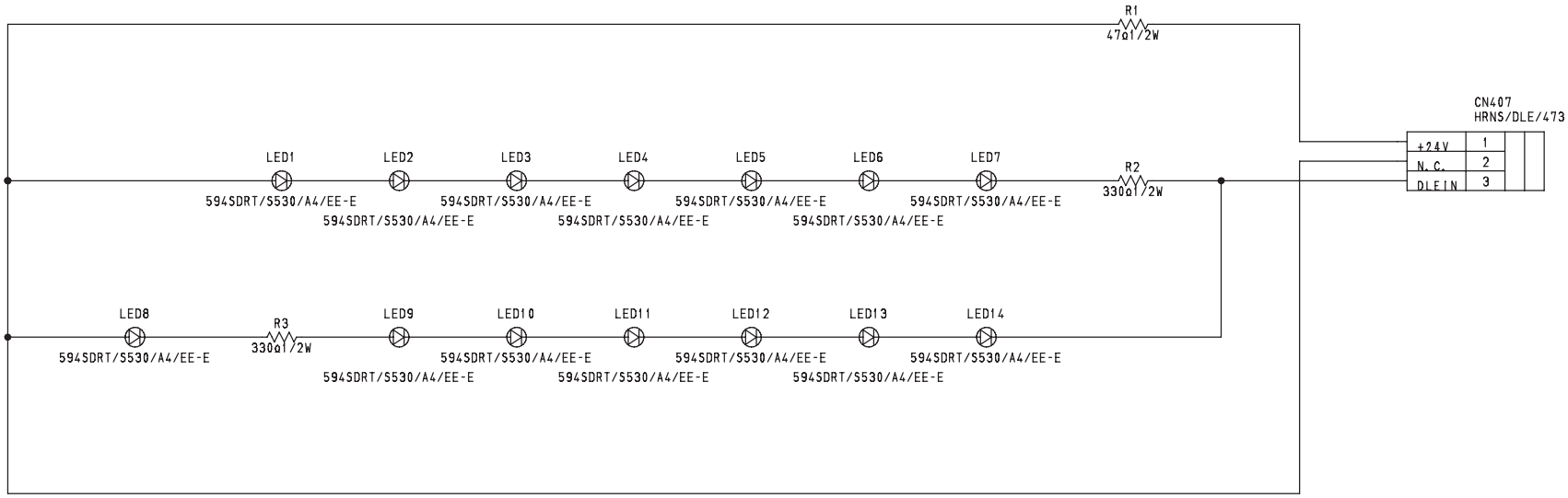

CCD 3/5



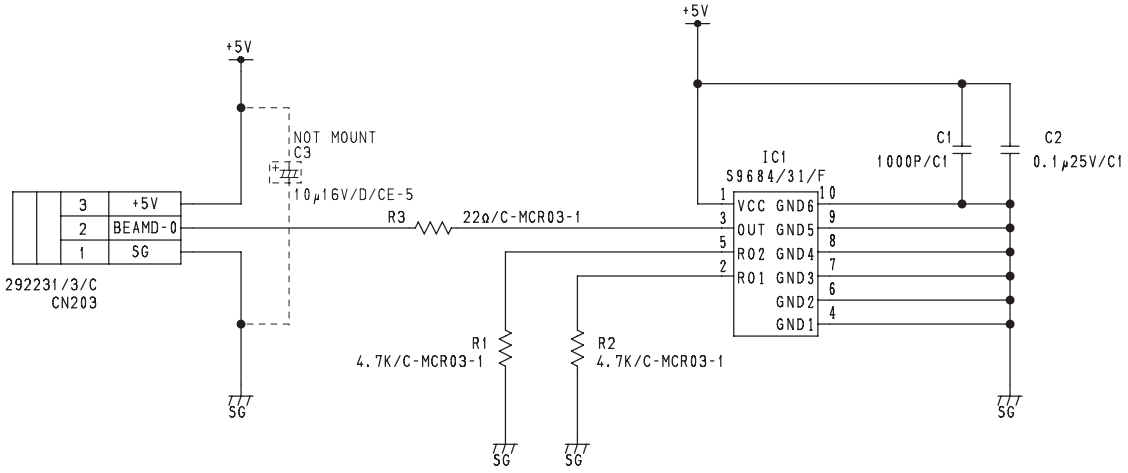

CCD 4/5



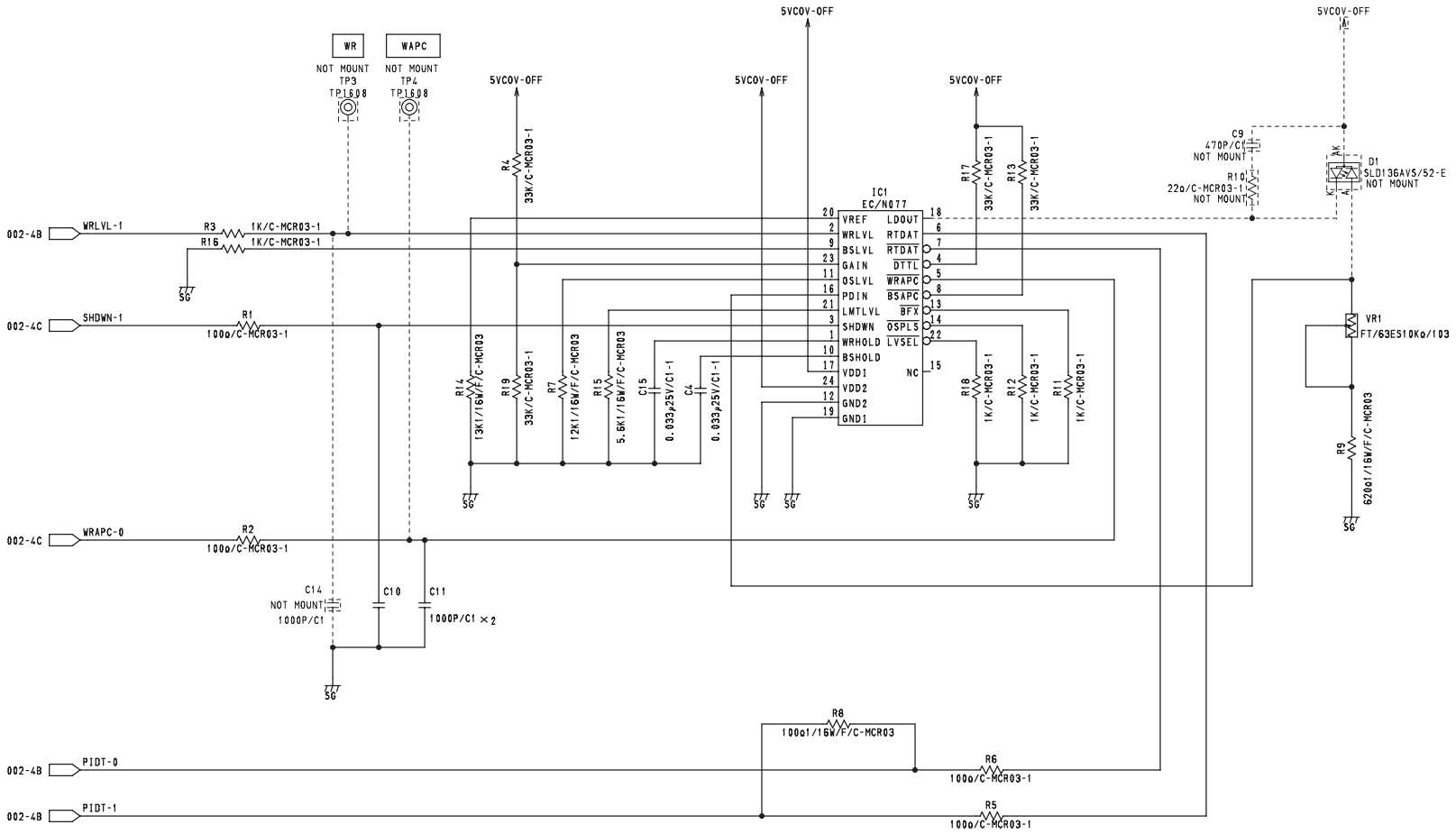

CCD 5/5



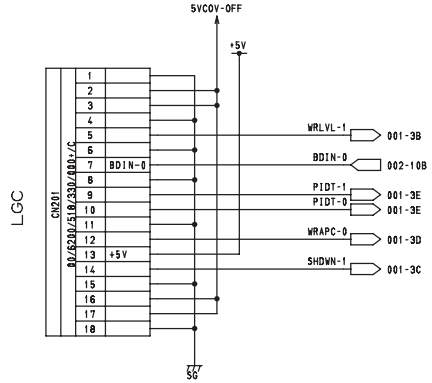

LED 1/1

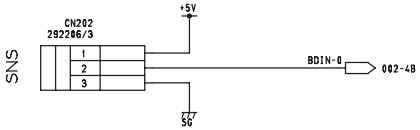


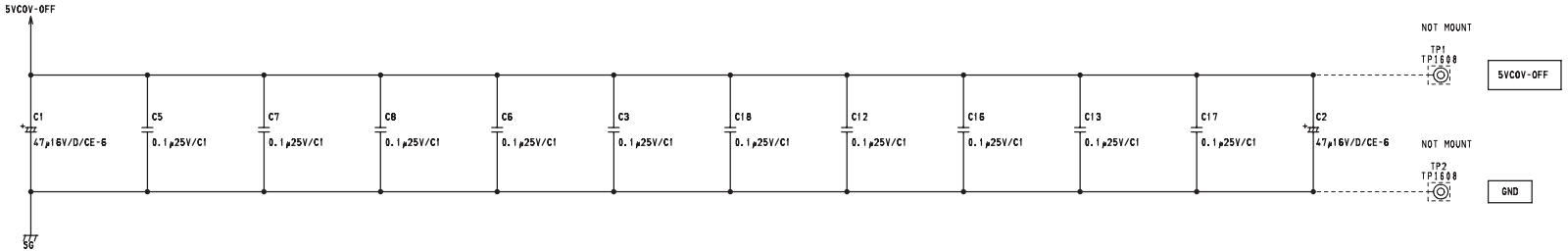

SNS 1/1

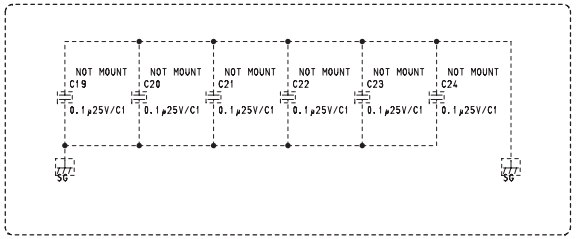



LDR 1/2

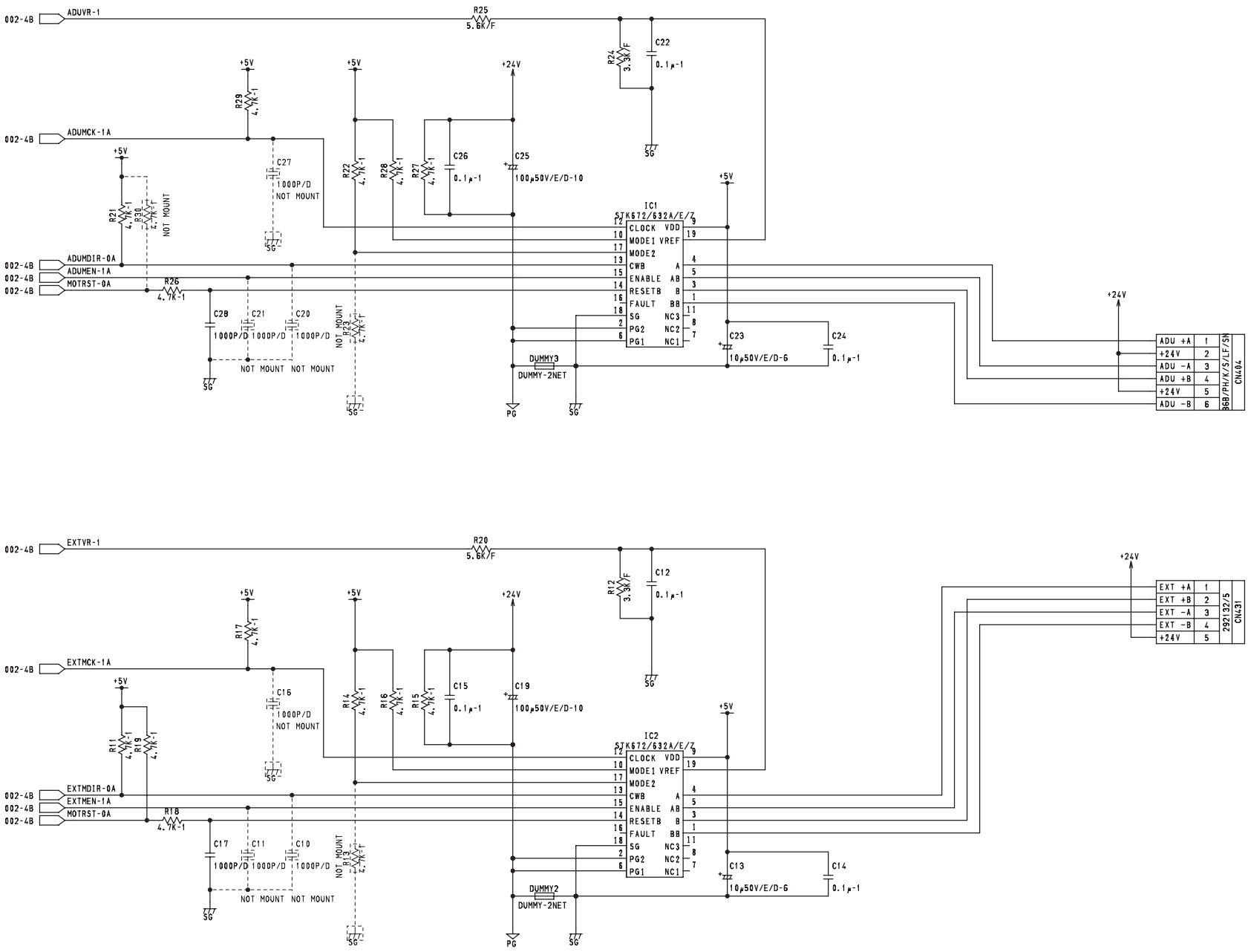


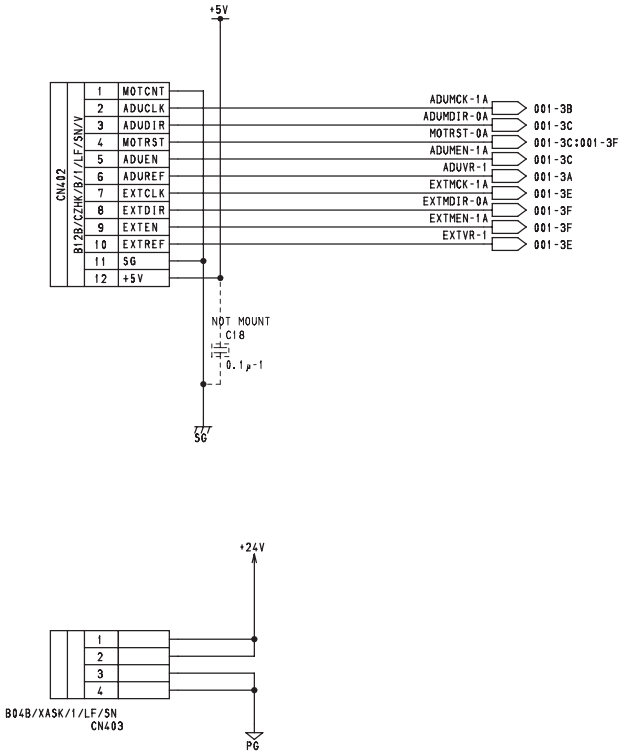



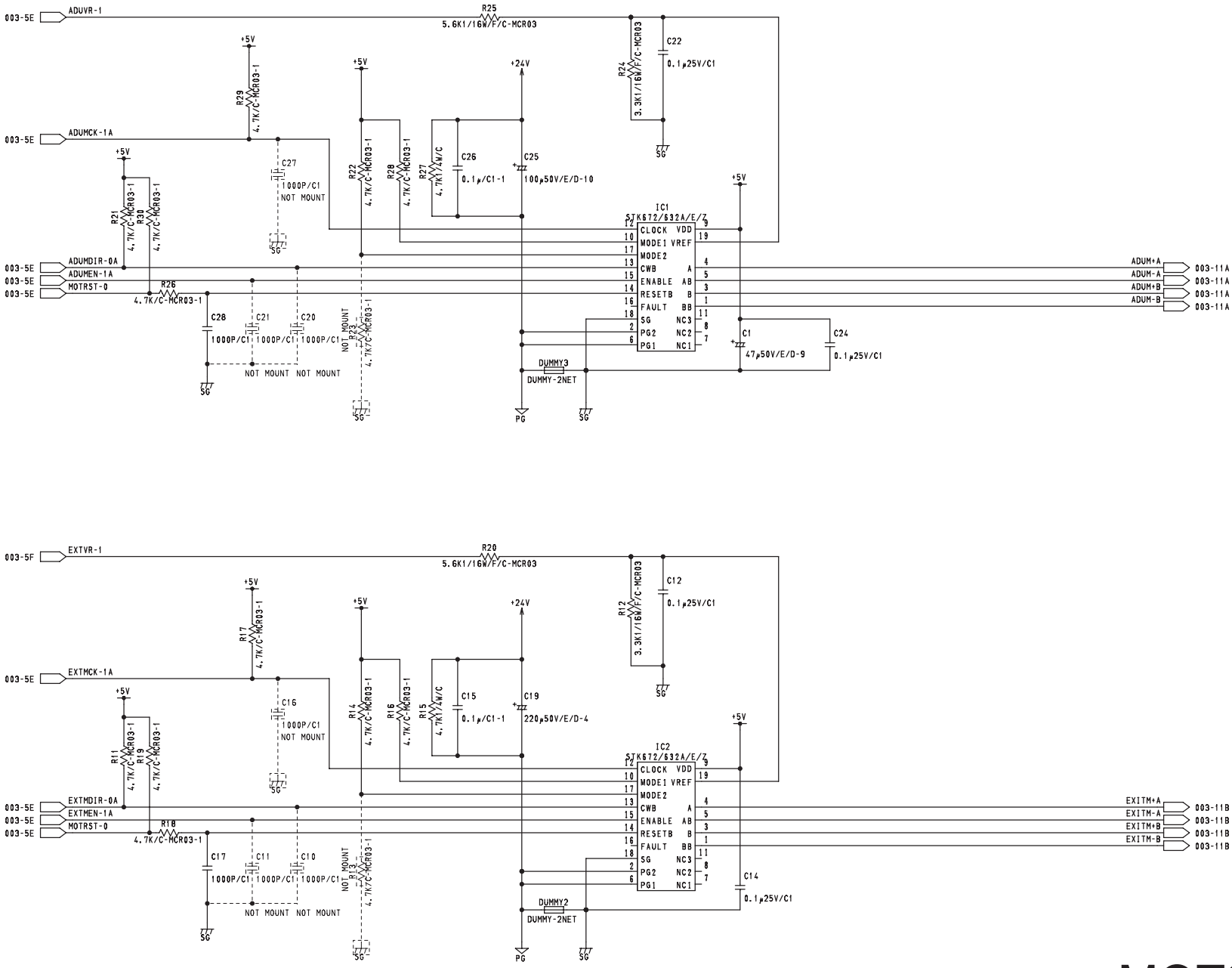

LDR 2/2



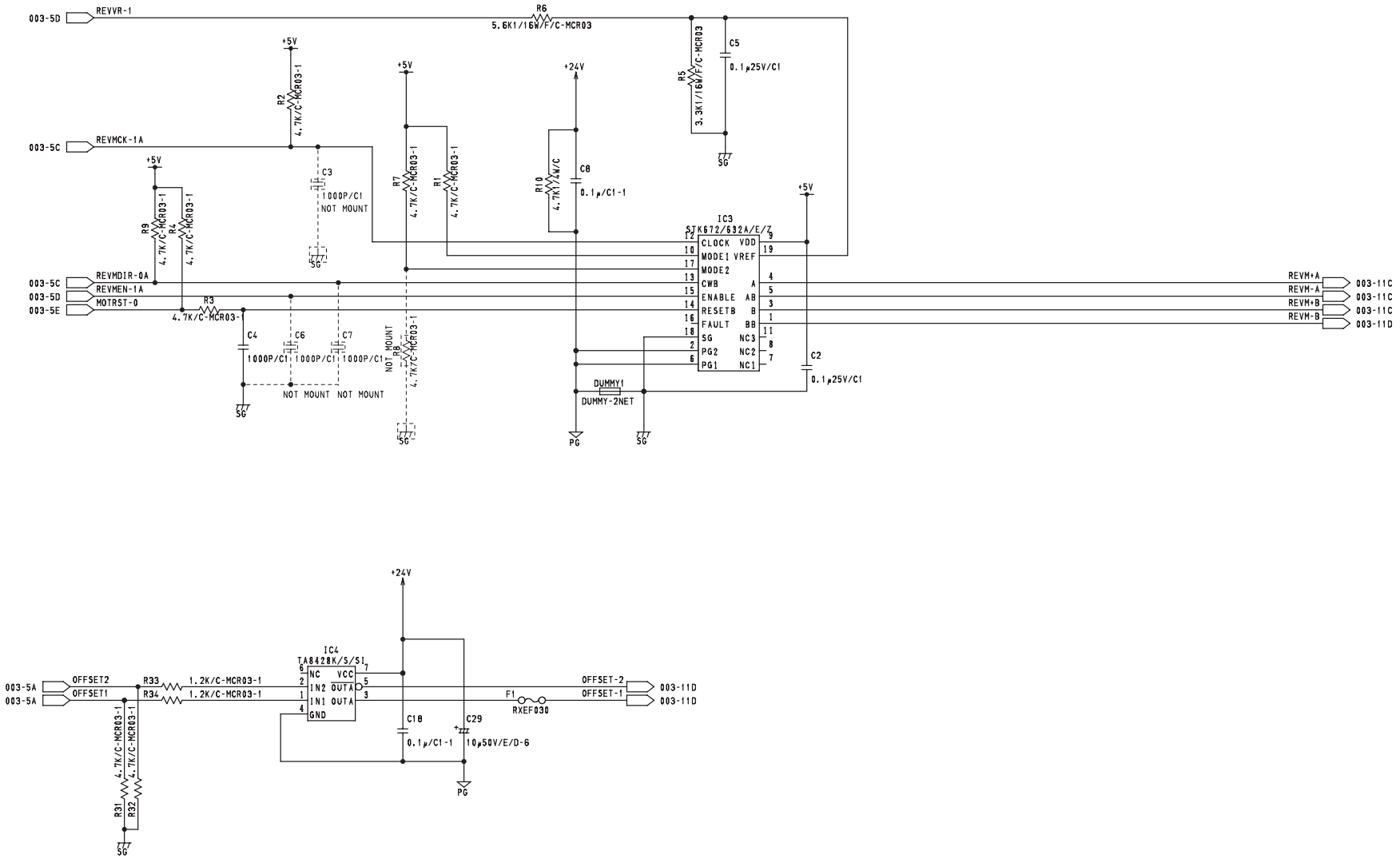

MOT 1/2



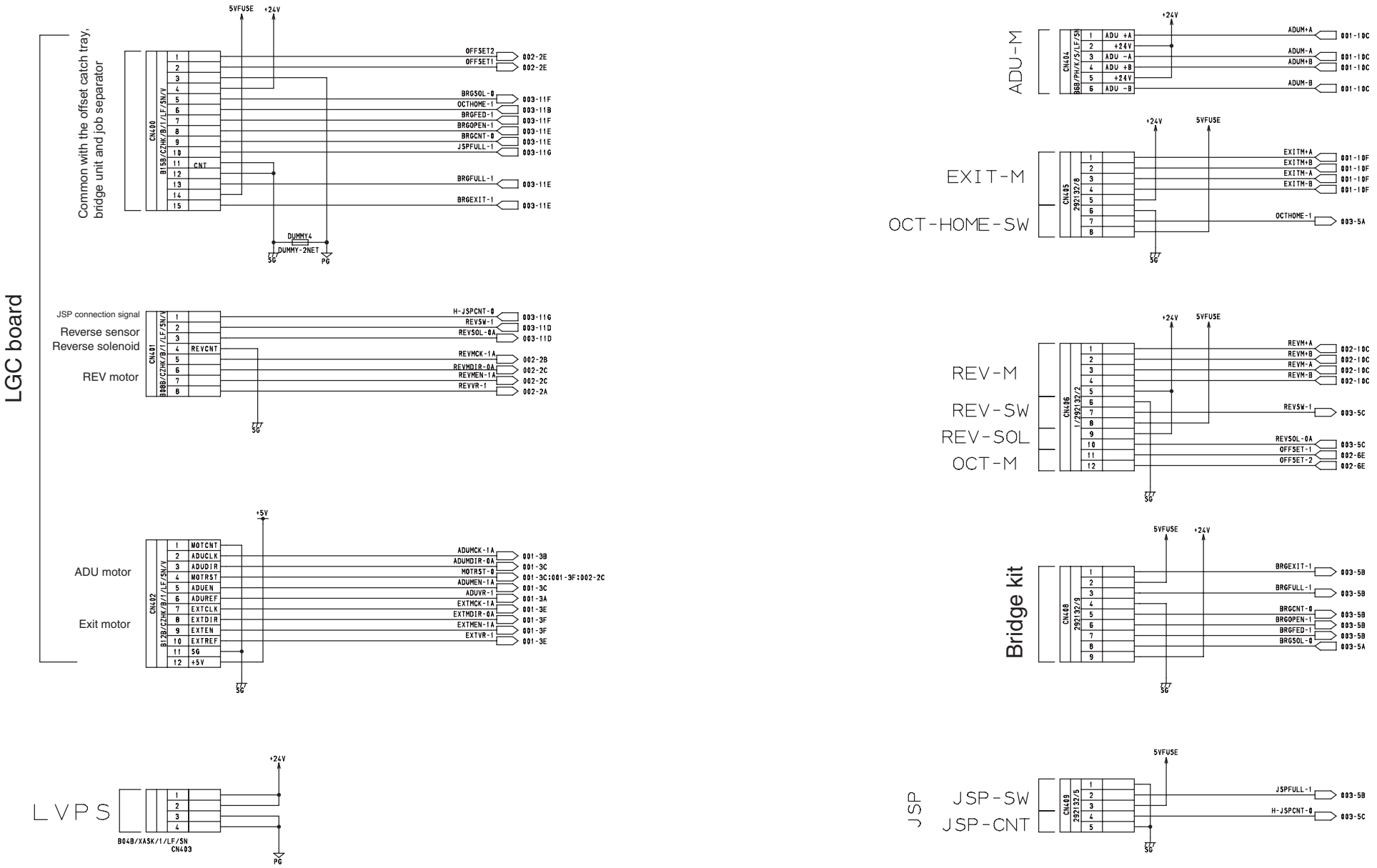

MOT 2/2



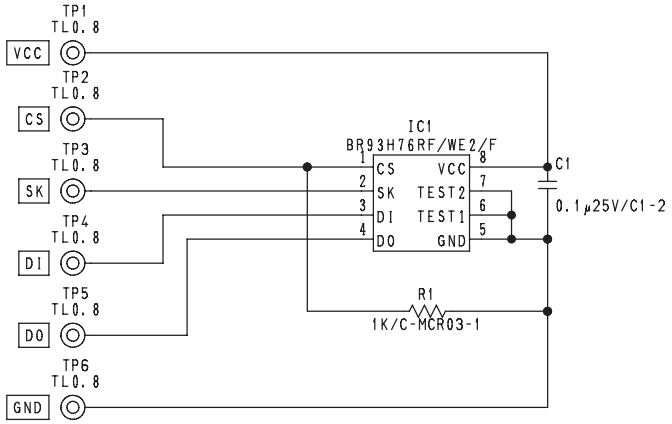

MOT2 1/3



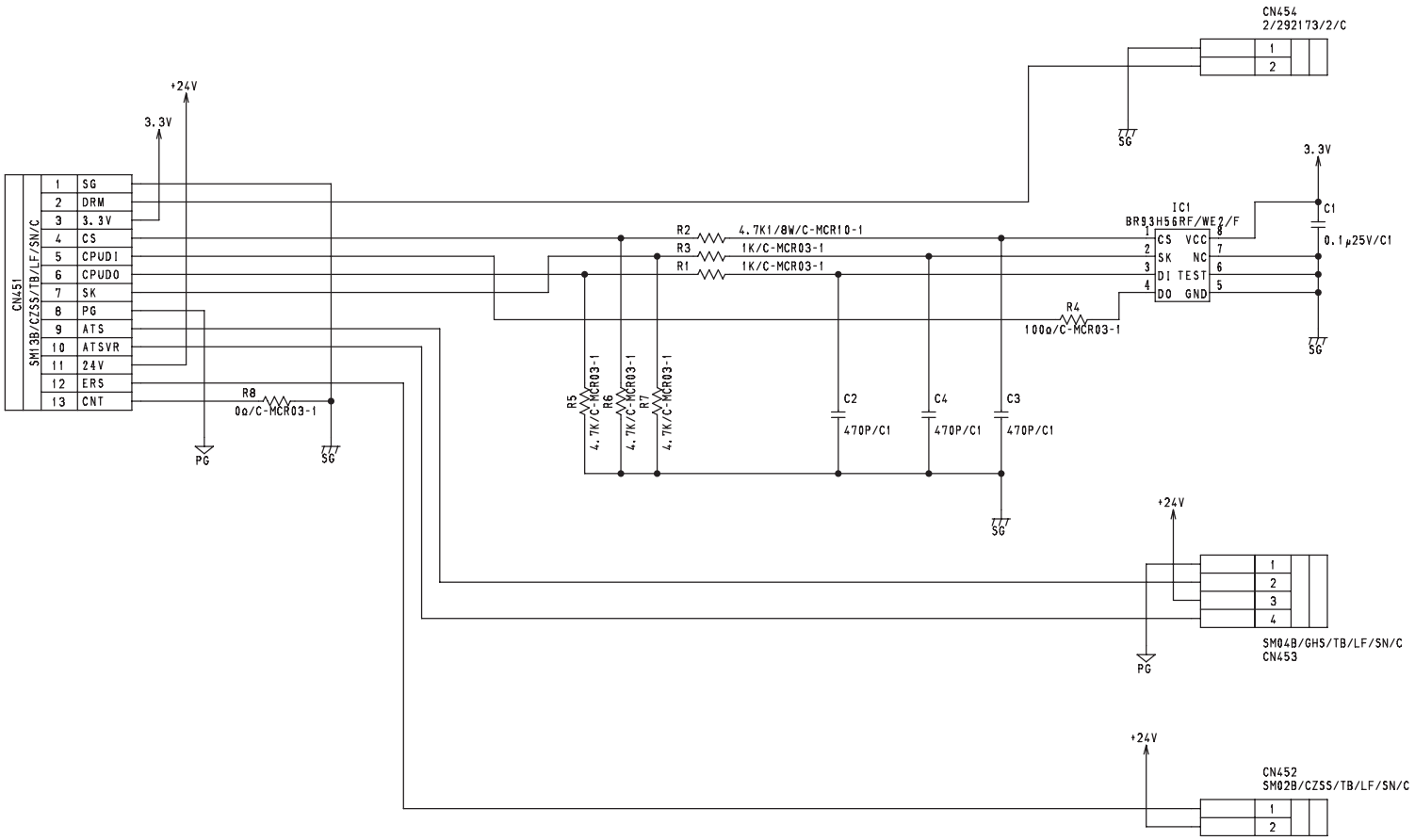

MOT2 2/3



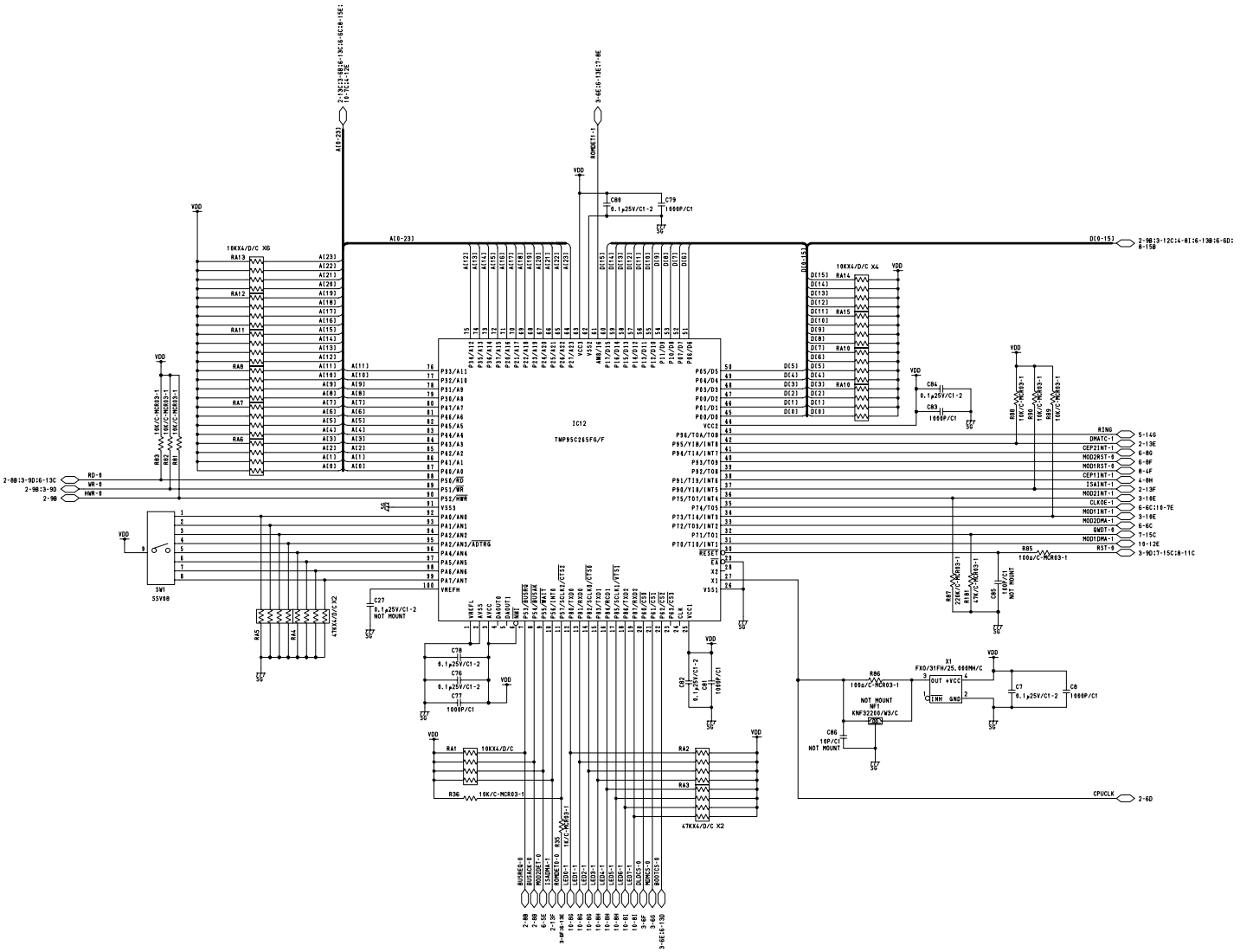

# MOT2 3/3



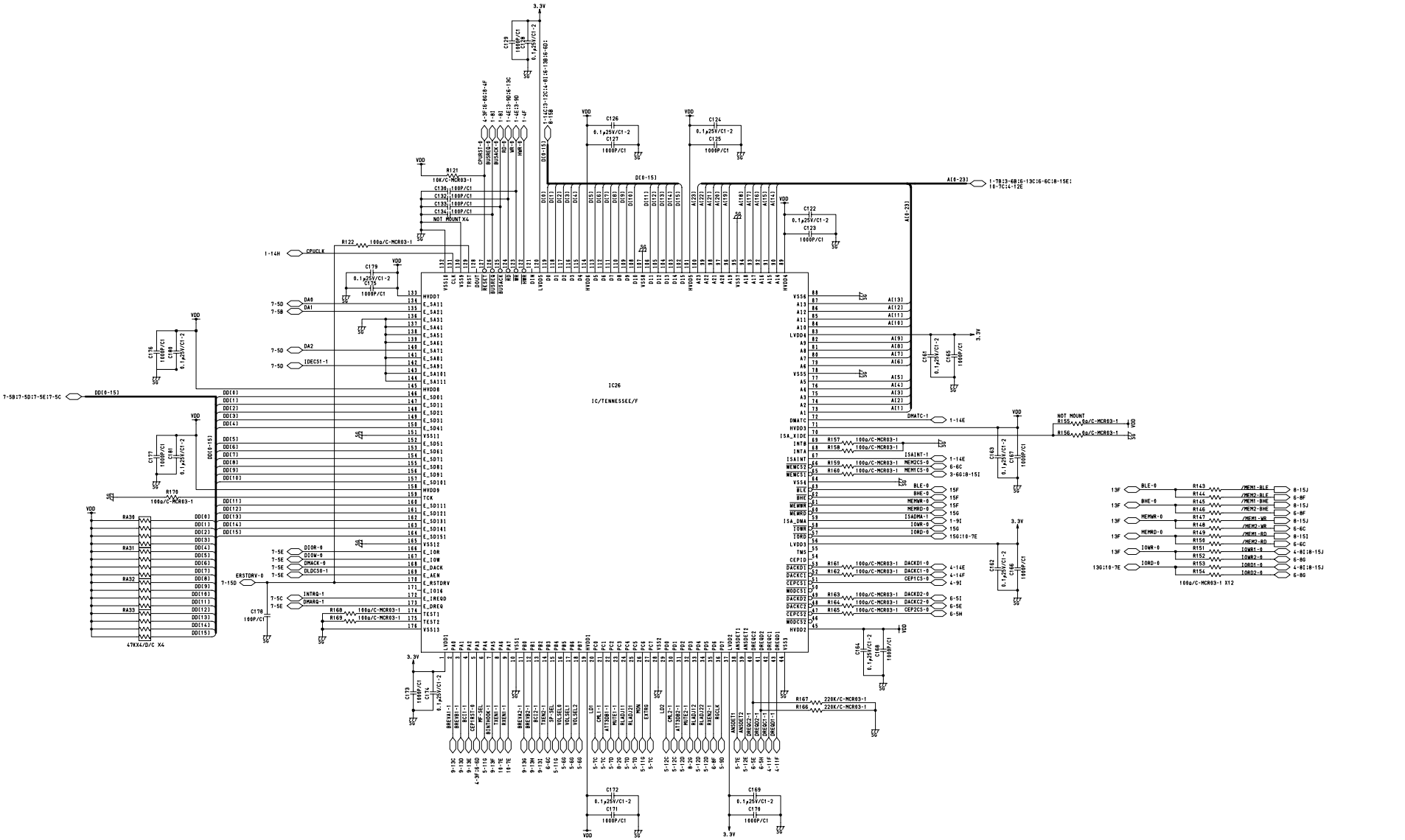

CTRG 1/1



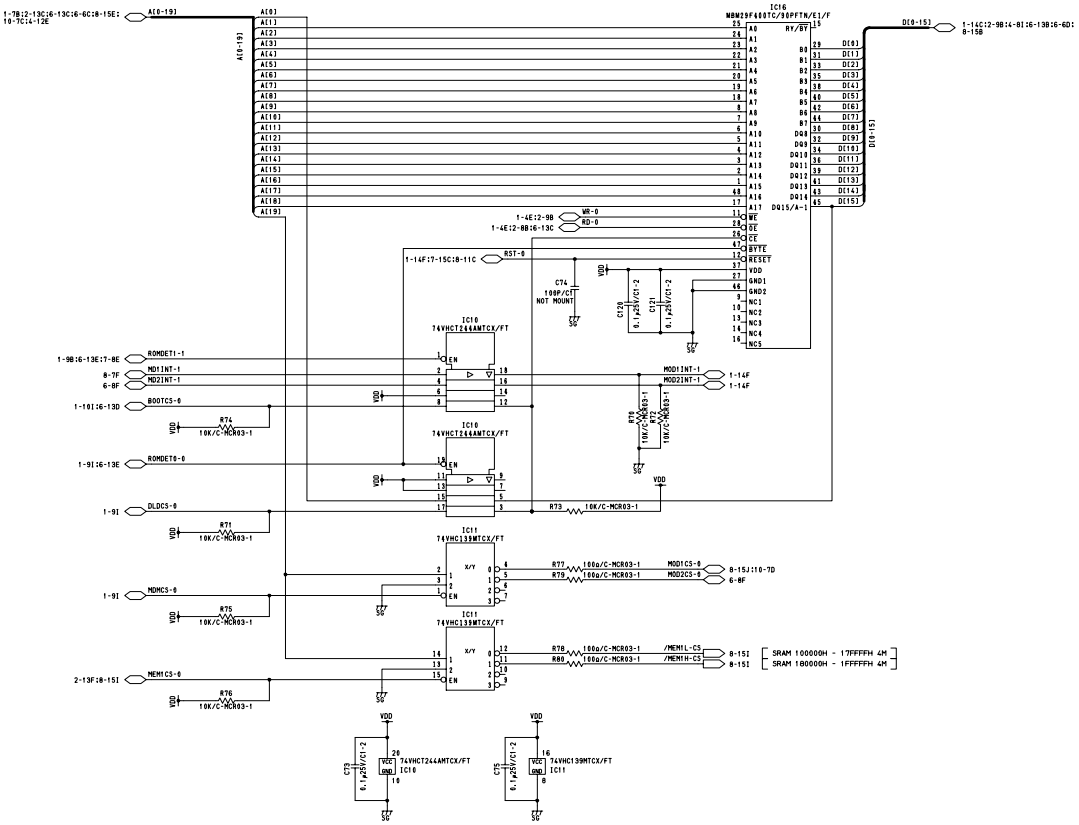

EPU 1/1



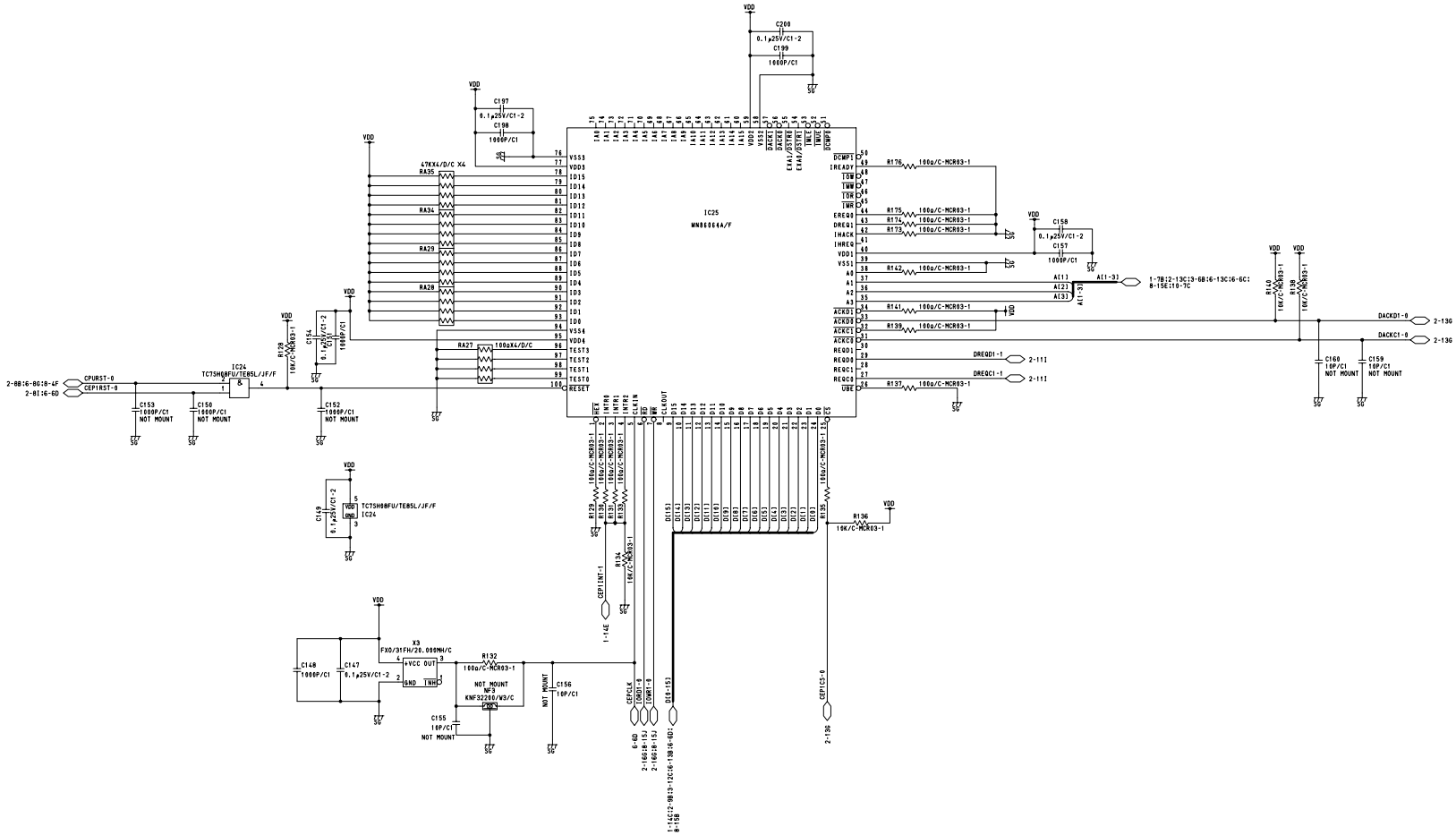

FAX 1/10



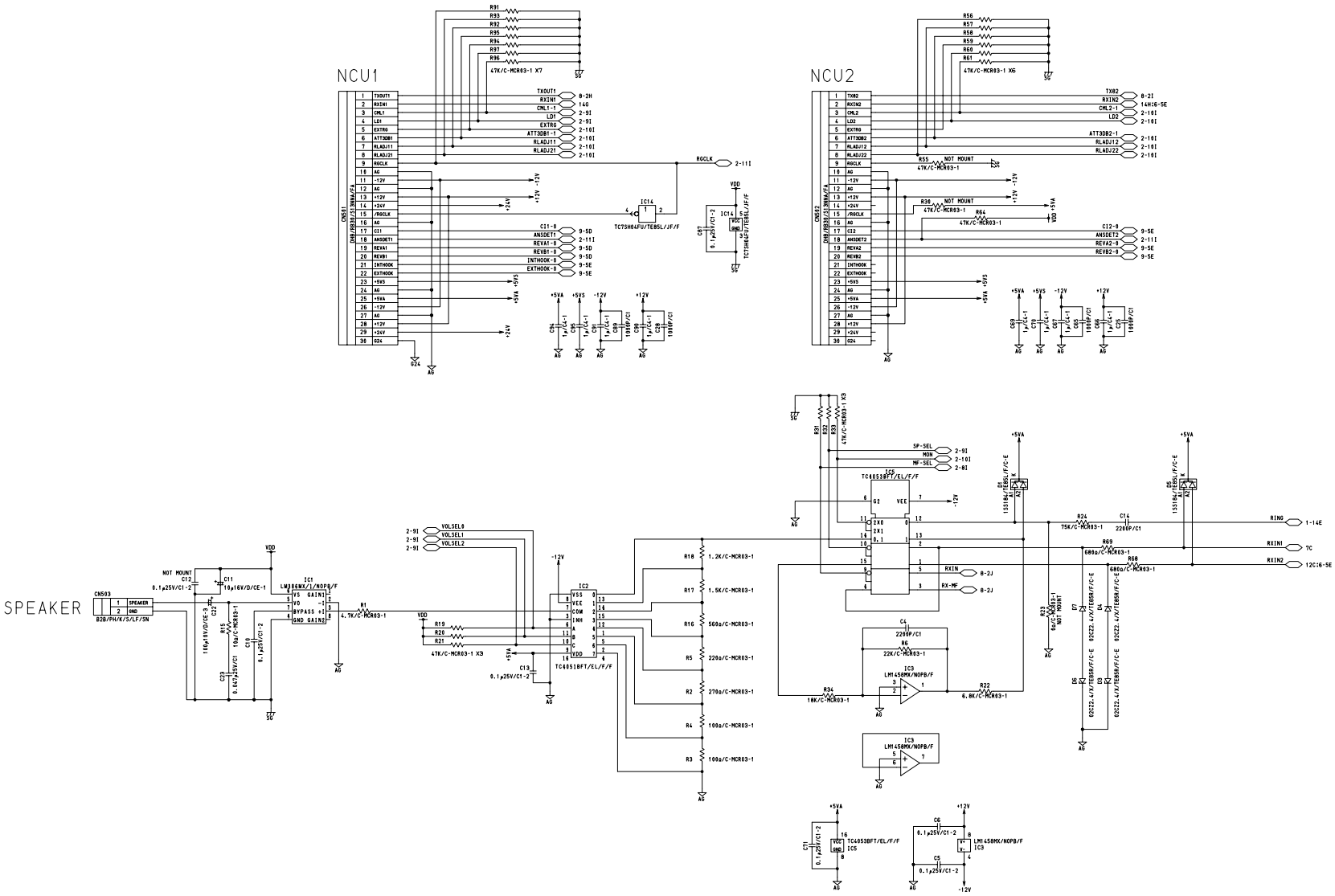

FAX 2/10



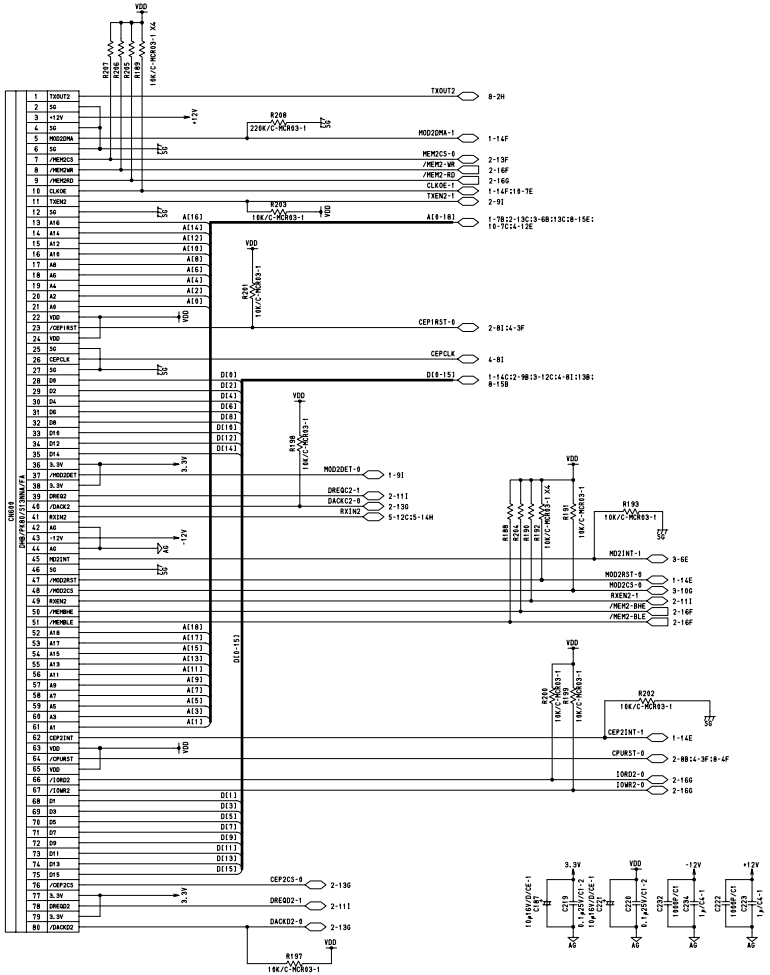
FAX 3/10



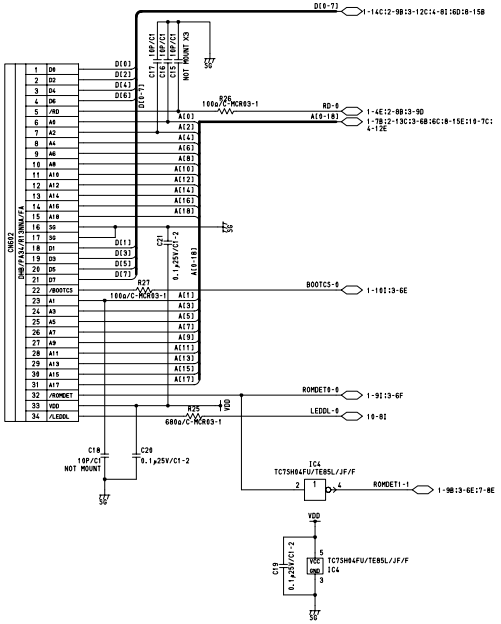

FAX 4/10



MODEM I/F

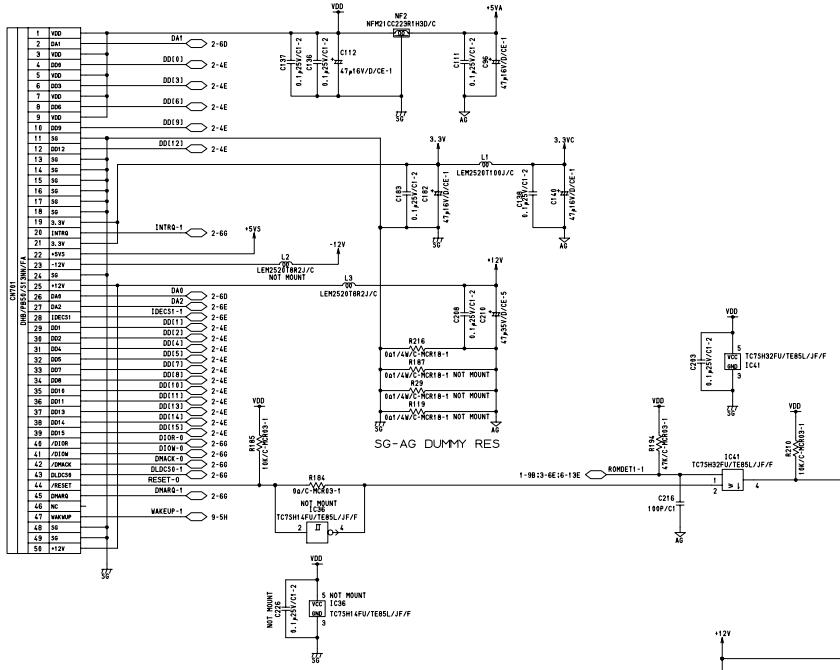


DOWN LOAD

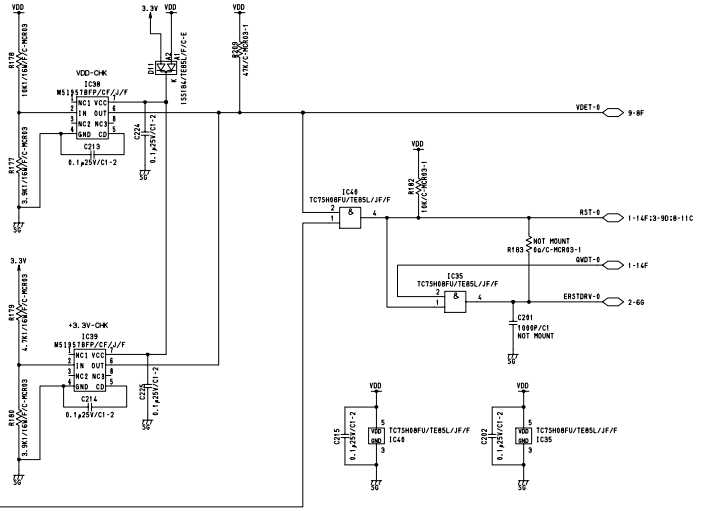


FAX 6/10

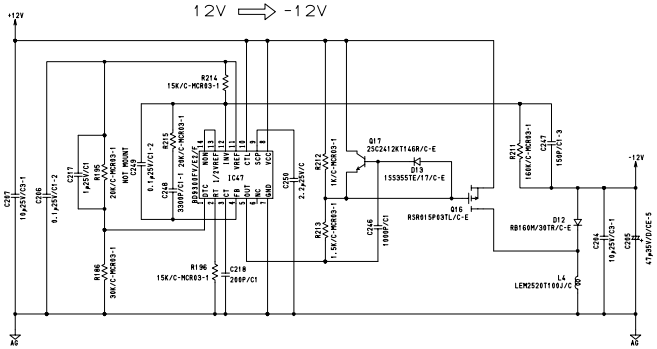
SYS BOARD I/F (IDE)



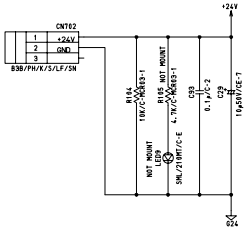
H/W RESET

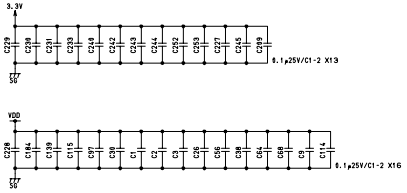


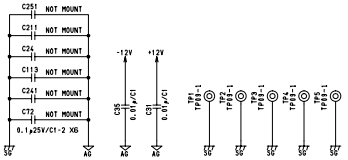
12V ⟹ -12V



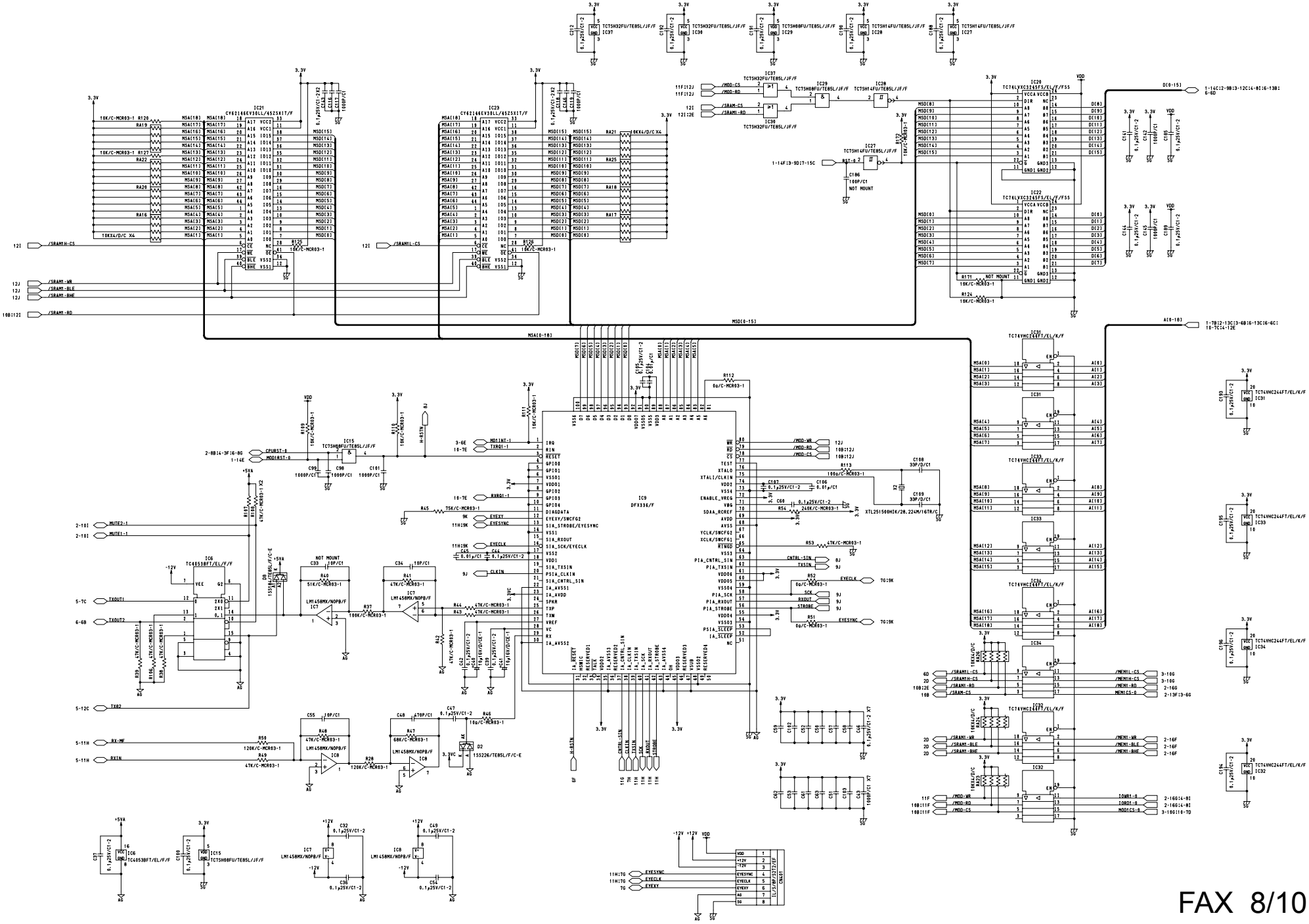
+24V POWER



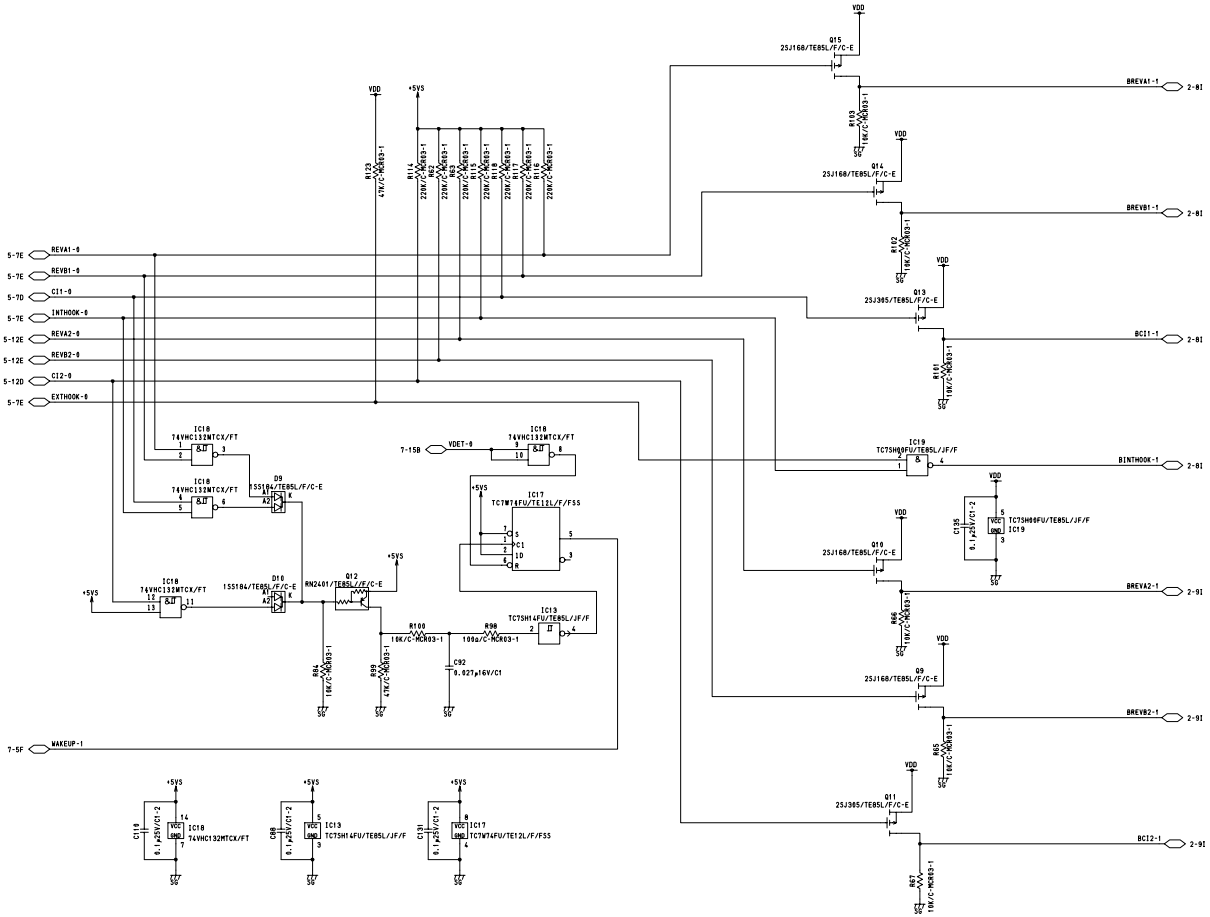




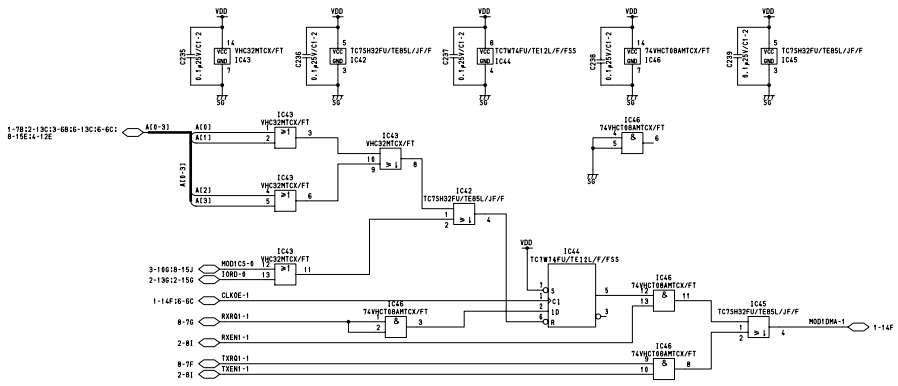
FAX 7/10

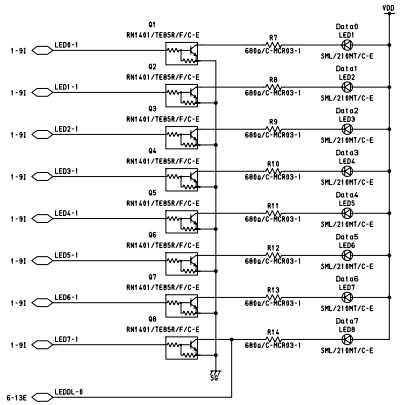


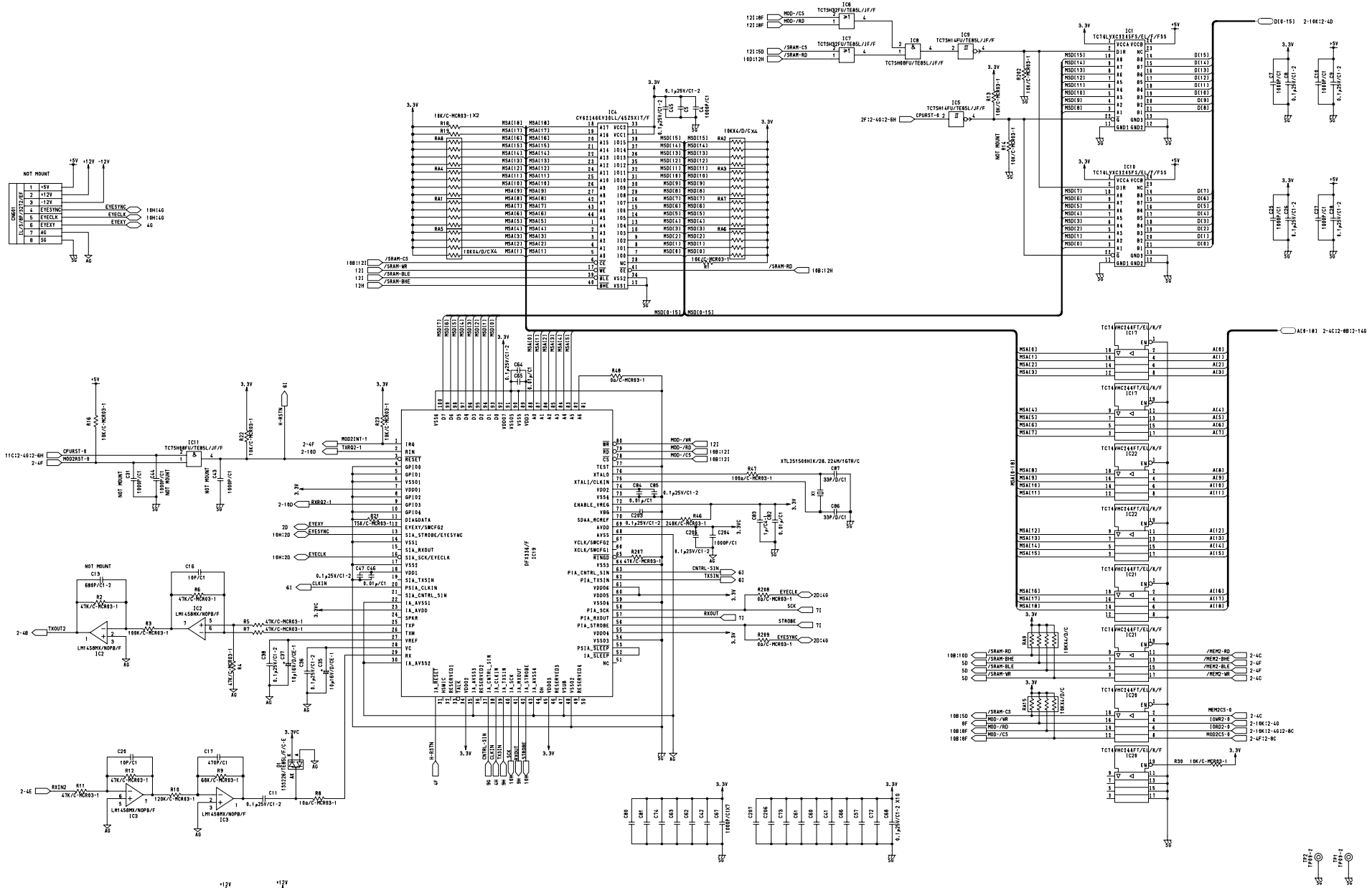
FAX 8/10




FAX 9/10

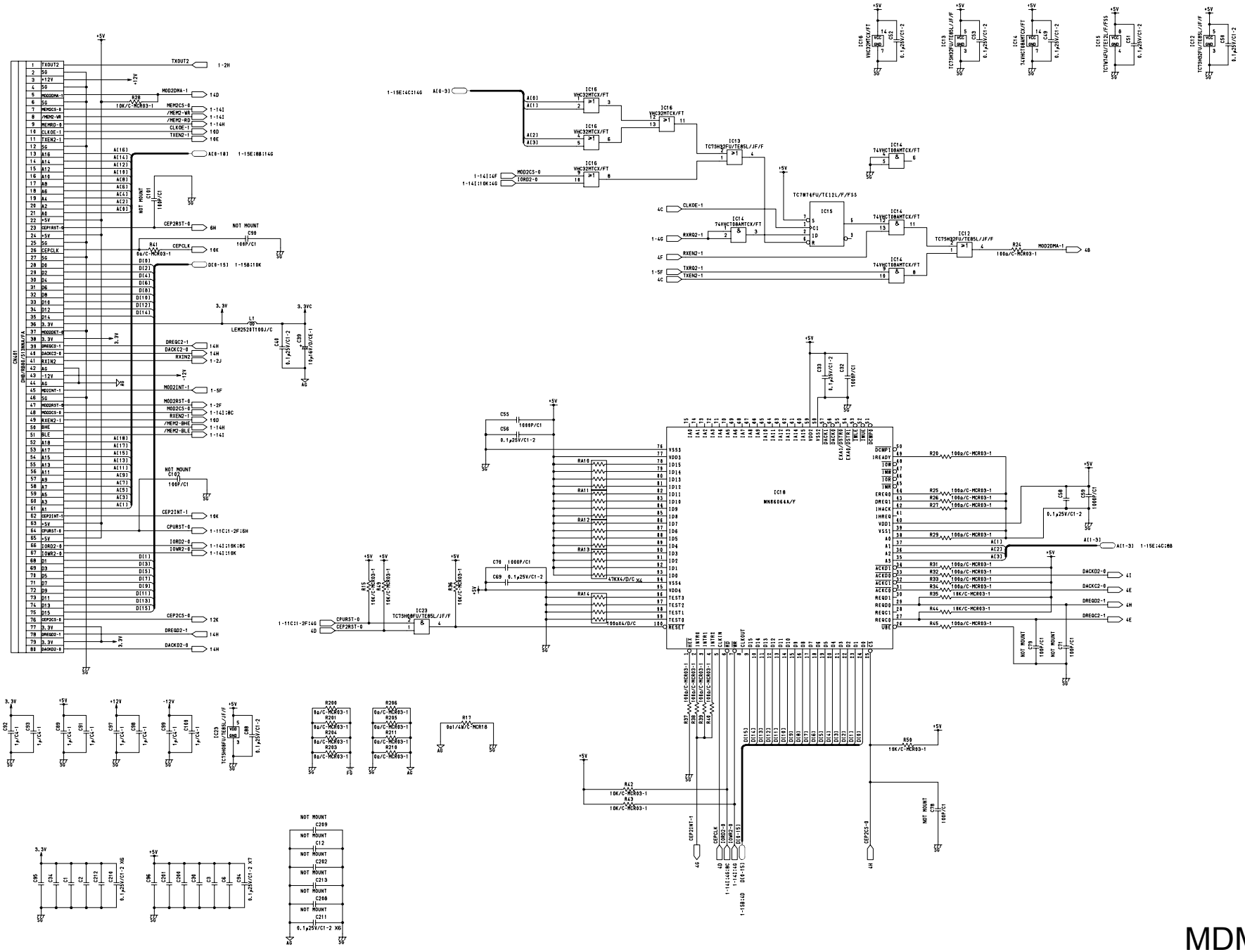




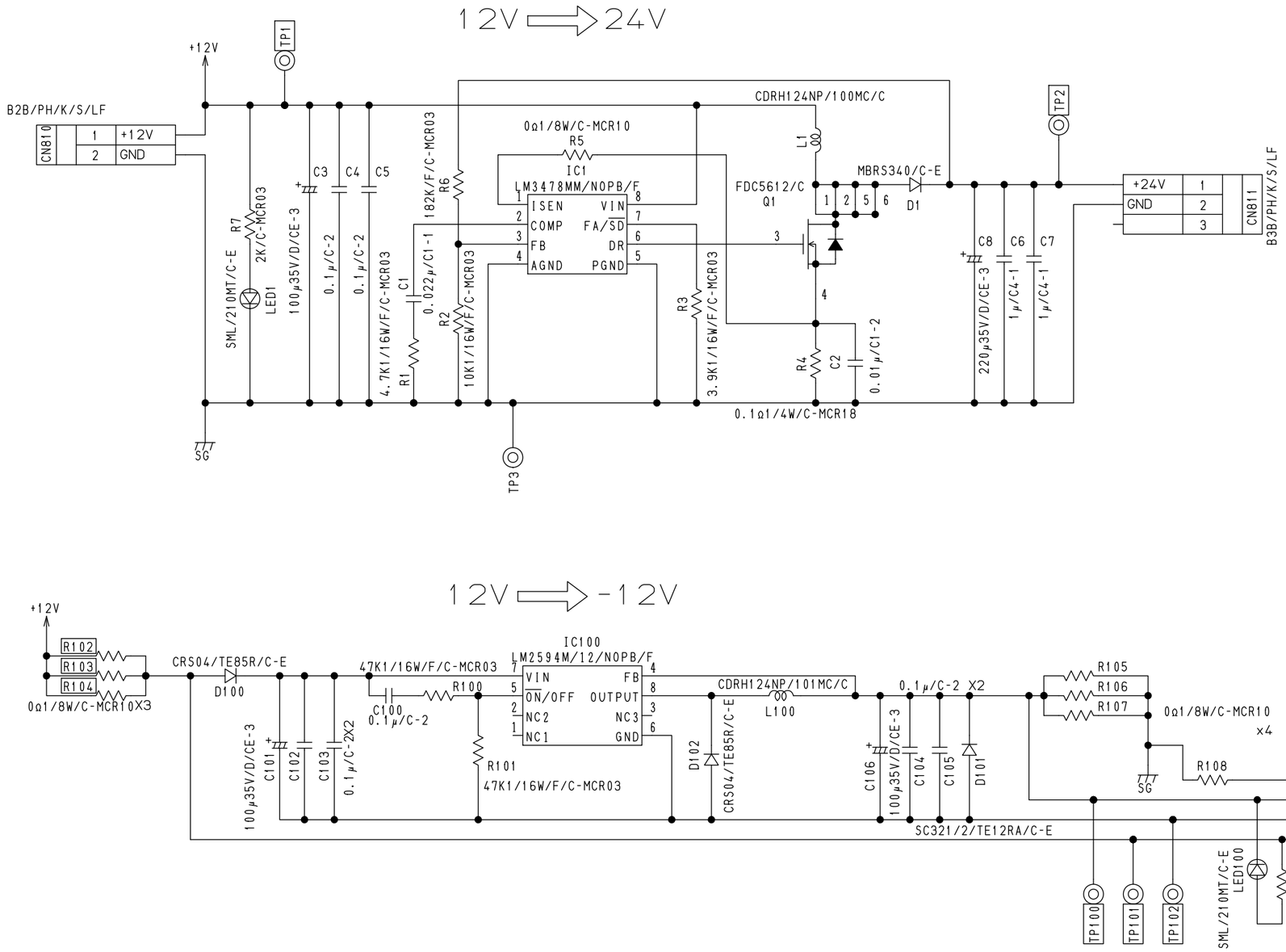


MDM 1/2

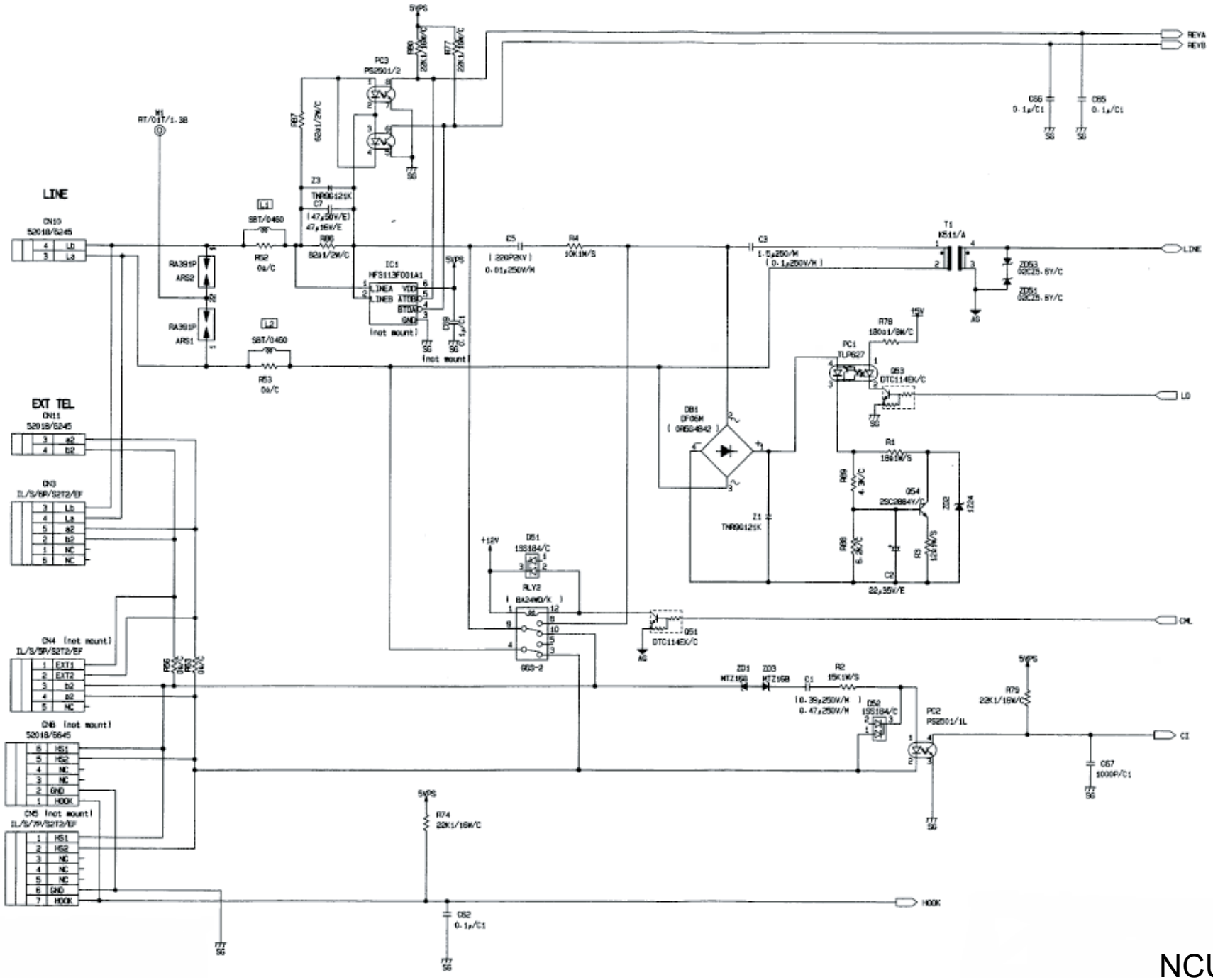
FAX I/F



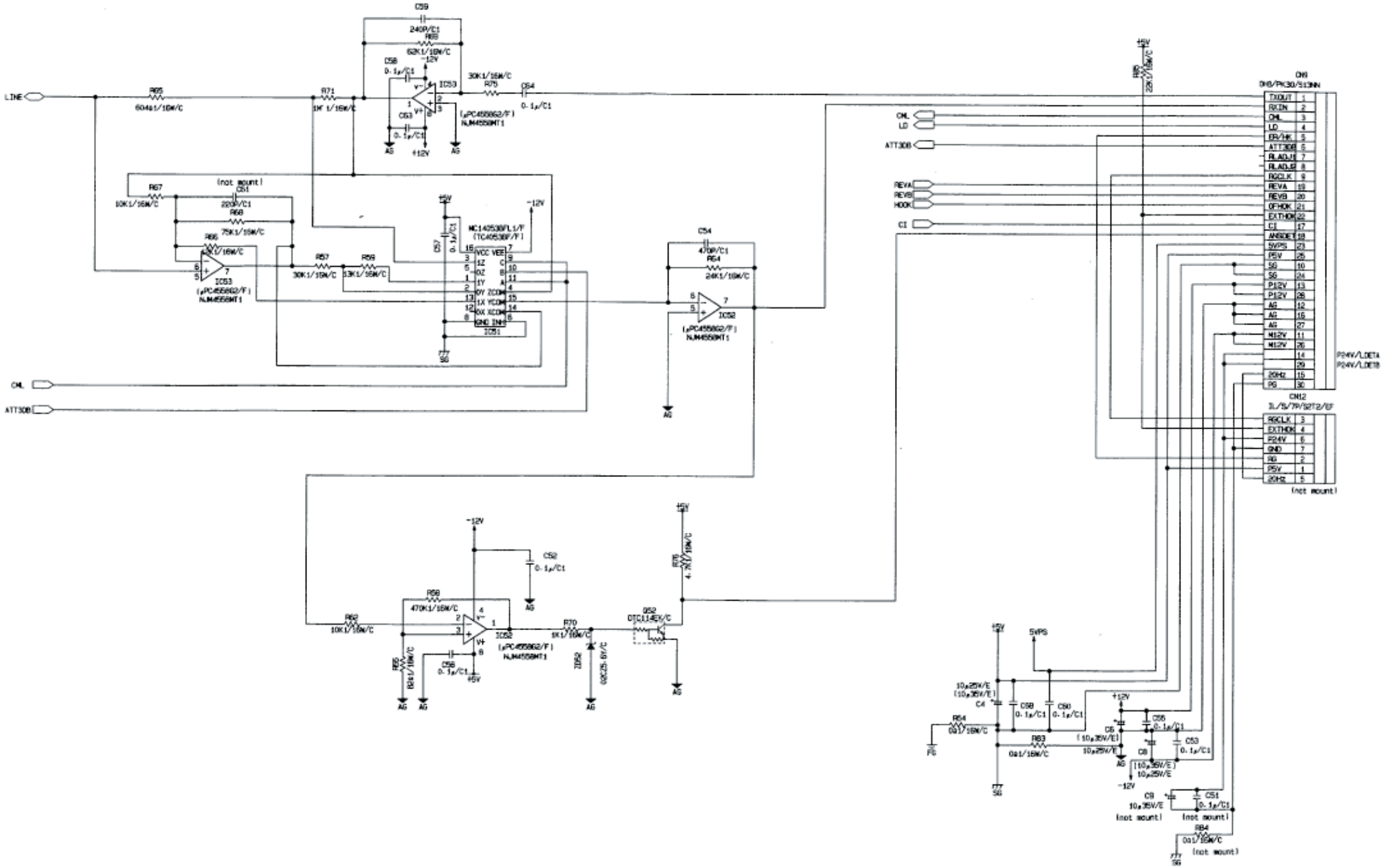
MDM 2/2



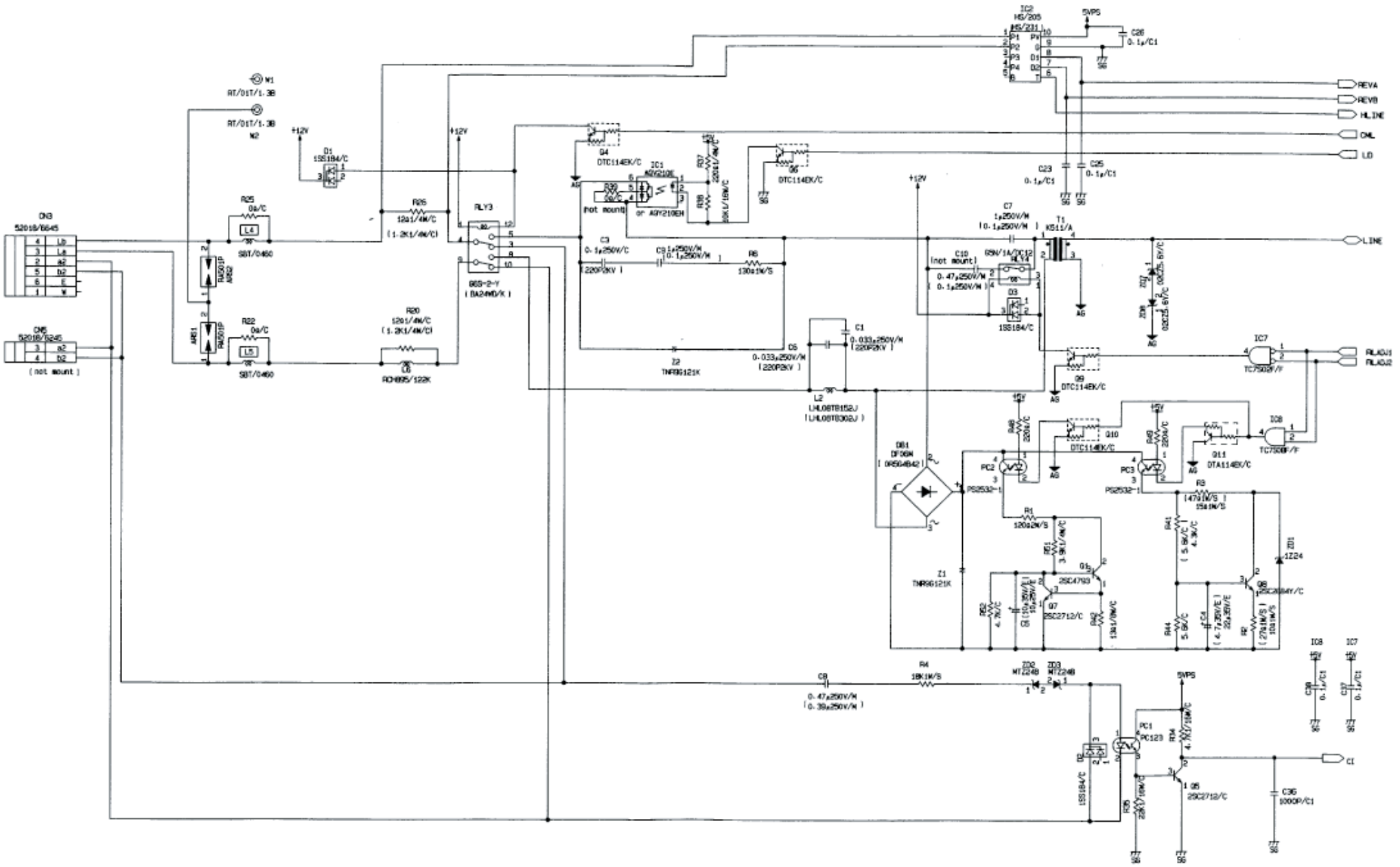

FAX POW 1/1

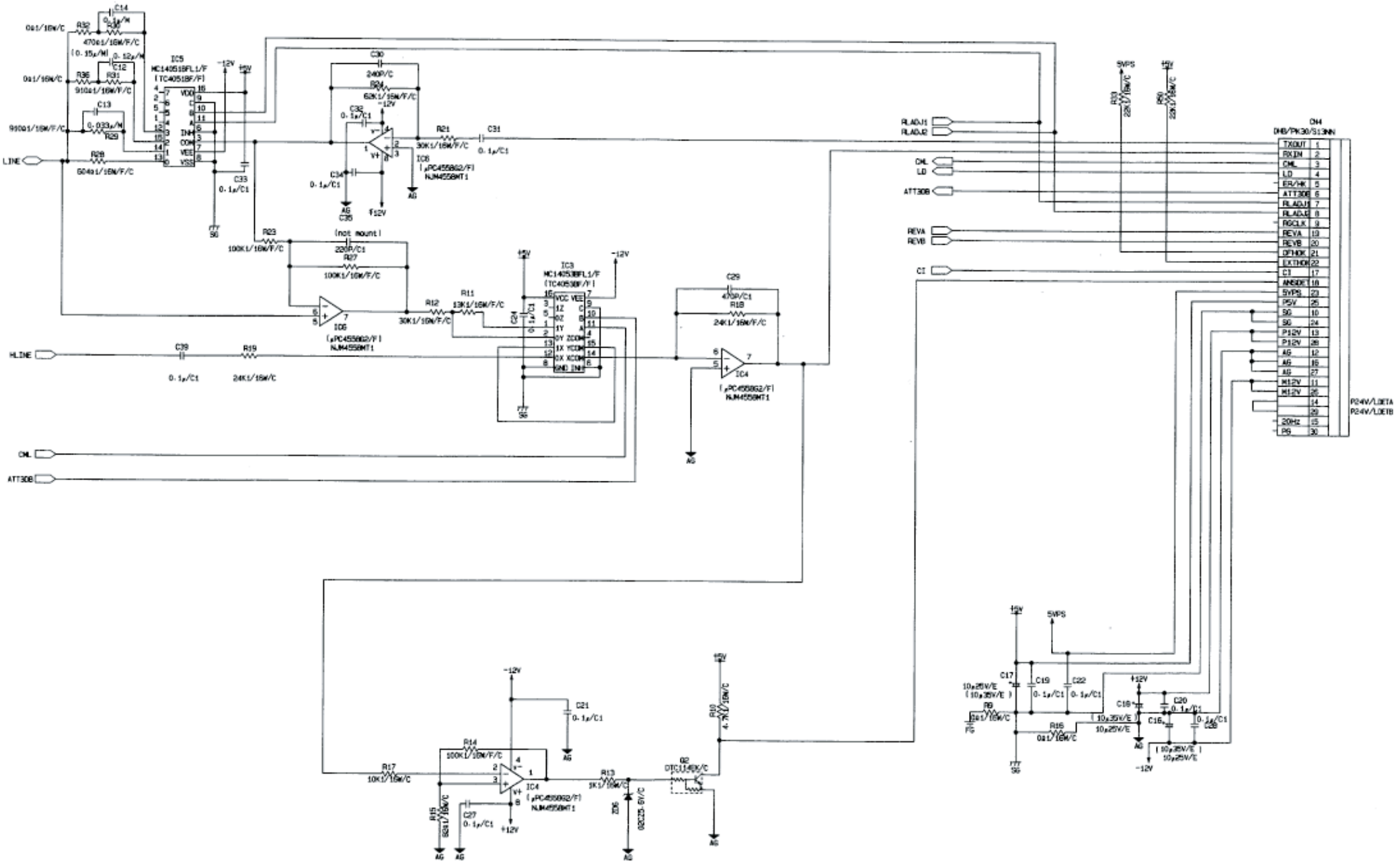



NCU-US 1/2

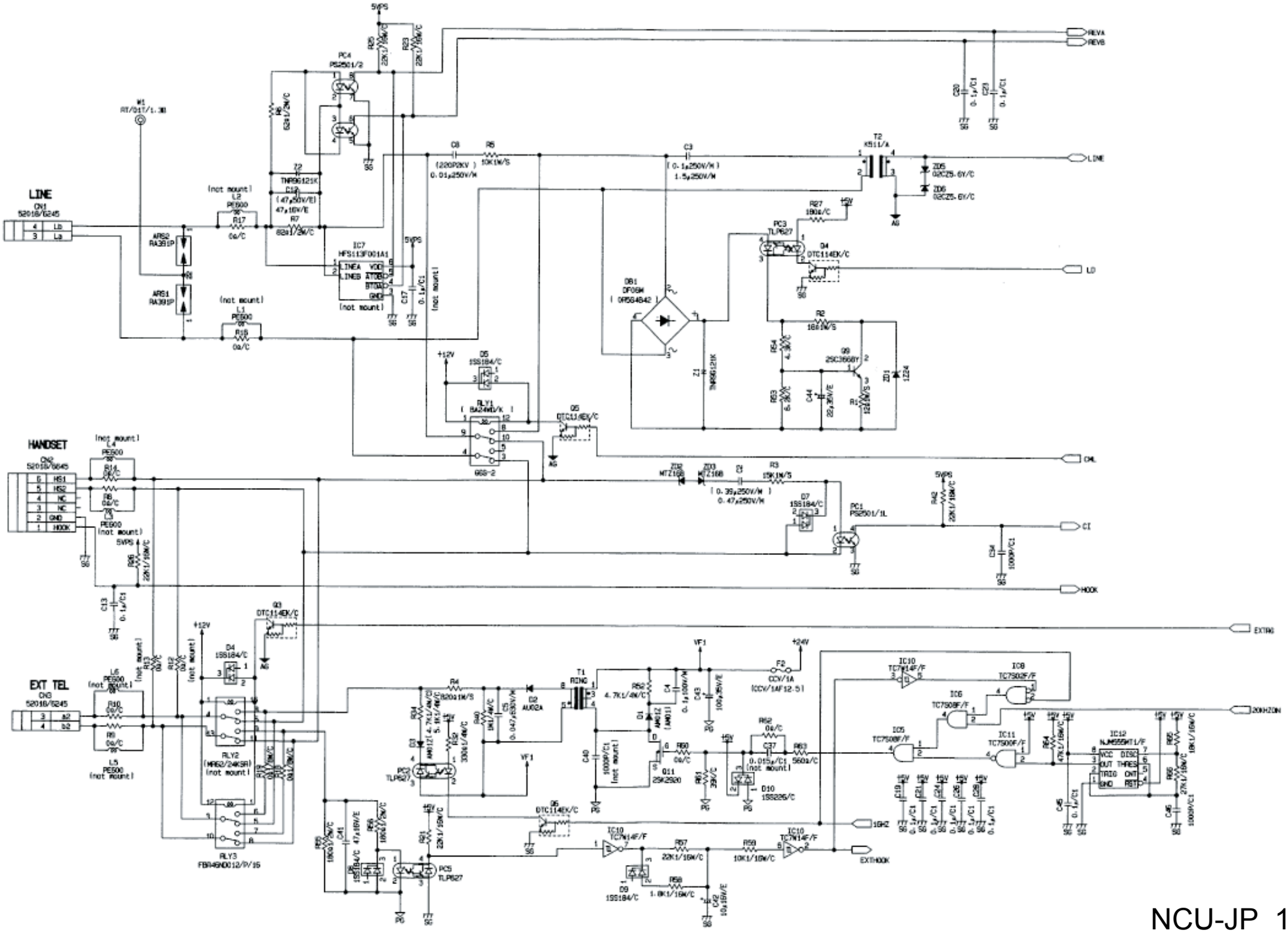


NCU-US 2/2

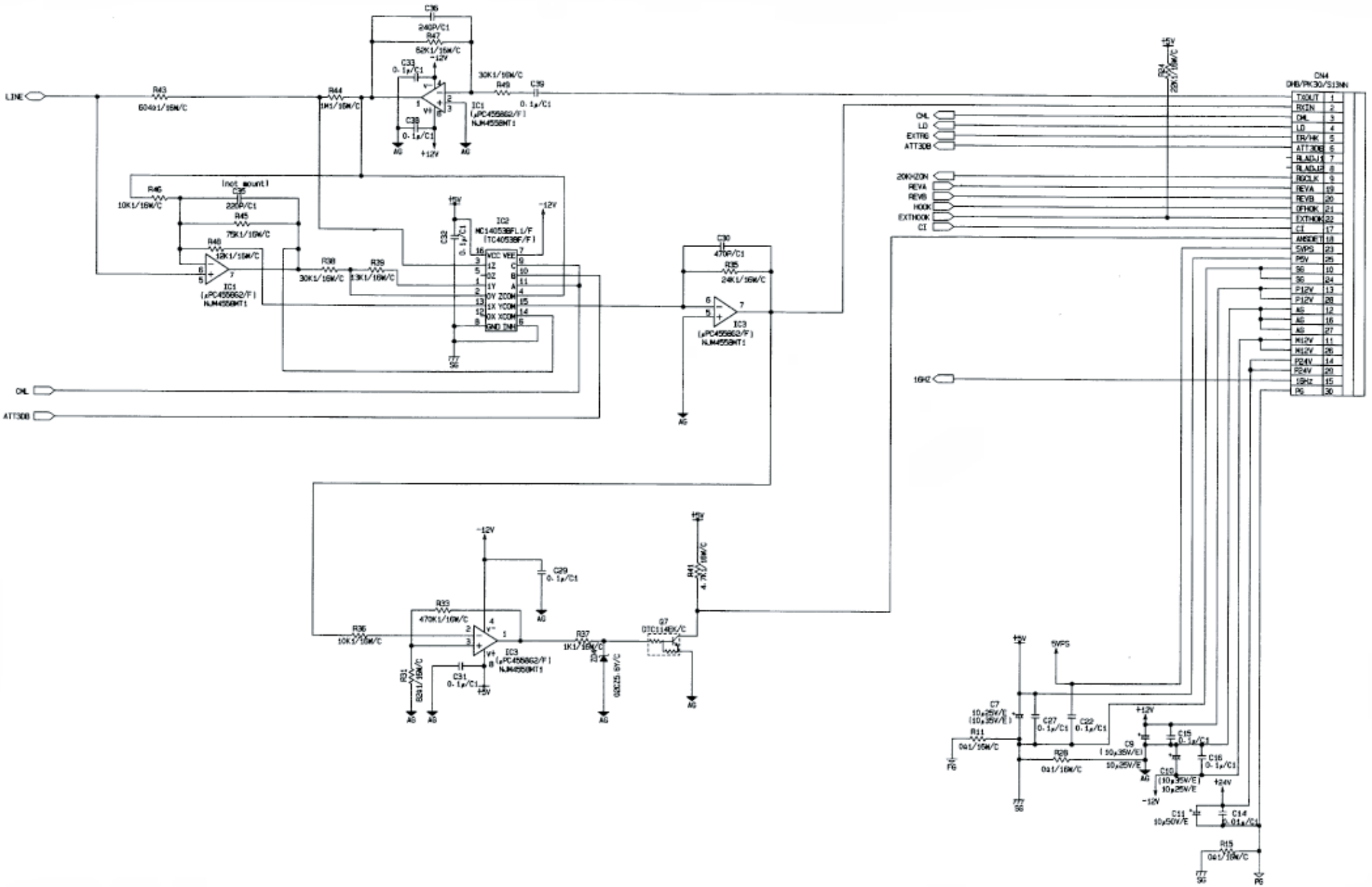




NCU-EU 2/2




NCU-JP 1/2




NCU-JP 2/2