

TOSHIBA

PC BOARD REPAIR MANUAL

MULTIFUNCTIONAL DIGITAL SYSTEMS

e-STUDIO202L/232/282



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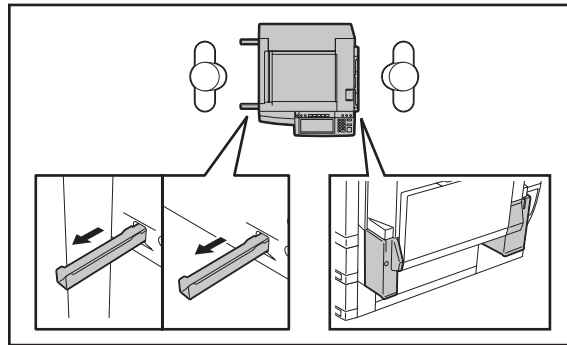
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GENERAL PRECAUTIONS REGARDING THE SERVICE FOR e-STUDIO202L/232/282 SERIES

The installation and service should be done by a qualified service technician.

1) Transportation/Installation

- When transporting/installing the equipment, employ two persons and be sure to hold the positions as shown in the figure.
The equipment is quite heavy and weighs approximately 75 kg (165.34 lb.) therefore pay full attention when handling it.



- Be sure not to hold the movable parts or units (e.g. the control panel, ADU or RADF) when transporting the equipment.
- Be sure to use a dedicated outlet with AC 110 V / 13.2 A, 115 V or 127 V / 12 A, 220-240 V or 240 V / 8 A for its power source.
- The equipment must be grounded for safety.
- Select a suitable place for installation. Avoid excessive heat, high humidity, dust, vibration and direct sunlight.
- Provide proper ventilation since the equipment emits a slight amount of ozone.
- To insure adequate working space for the copying operation, keep a minimum clearance of 80 cm (32") on the left, 80 cm (32") on the right and 10 cm (4") on the rear.
- The equipment shall be installed near the socket outlet and shall be accessible.
- Be sure to fix and plug in the power cable securely after the installation so that no one trips over it.

2) General Precautions at Service

- Be sure to turn the power OFF and unplug the power cable during service (except for the service should be done with the power turned ON).
- Unplug the power cable and clean the area around the prongs of the plug and socket outlet once a year or more. A fire may occur when dust lies on this area.
- When the parts are disassembled, reassembly is the reverse of disassembly unless otherwise noted in this manual or other related documents. Be careful not to install small parts such as screws, washers, pins, E-rings, star washers in the wrong places.
- Basically, the equipment should not be operated with any parts removed or disassembled.
- The PC board must be stored in an anti-electrostatic bag and handled carefully using a wristband since the ICs on it may be damaged due to static electricity.

Caution: Before using the wristband, unplug the power cable of the equipment and make sure that there are no charged objects which are not insulated in the vicinity.

- Avoid expose to laser beam during service. This equipment uses a laser diode. Be sure not to expose your eyes to the laser beam. Do not insert reflecting parts or tools such as a screwdriver on the laser beam path. Remove all reflecting metals such as watches, rings, etc. before starting service.
- Be sure not to touch high-temperature sections such as the exposure lamp, fuser unit, damp heater and areas around them.
- Be sure not to touch high-voltage sections such as the chargers, developer, high-voltage transformer, exposure lamp control inverter, inverter for the LCD backlight and power supply unit. Especially, the board of these components should not be touched since the electric charge may remain in the capacitors, etc. on them even after the power is turned OFF.
- Make sure that the equipment will not operate before touching potentially dangerous places (e.g. rotating/operating sections such as gears, belts pulleys, fans and laser beam exit of the laser optical unit).
- Be careful when removing the covers since there might be the parts with very sharp edges underneath.
- When servicing the equipment with the power turned ON, be sure not to touch live sections and rotating/operating sections. Avoid exposing your eyes to laser beam.
- Use designated jigs and tools.
- Use recommended measuring instruments or equivalents.
- Return the equipment to the original state and check the operation when the service is finished.

3) Important Service Parts for Safety

- The breaker, door switch, fuse, thermostat, thermofuse, thermistor, IC-RAMs including lithium batteries, etc. are particularly important for safety. Be sure to handle/install them properly. If these parts are short-circuited and their functions become ineffective, they may result in fatal accidents such as burnout. Do not allow a short-circuit or do not use the parts not recommended by Toshiba TEC Corporation.

4) Cautionary Labels

- During servicing, be sure to check the rating plate and cautionary labels such as "Unplug the power cable during service", "CAUTION. HOT", "CAUTION. HIGH VOLTAGE", "CAUTION. LASER BEAM", etc. to see if there is any dirt on their surface and if they are properly stuck to the equipment.

5) **Disposal of the Equipment, Supplies, Packing Materials, Used Batteries and IC-RAMs**

- Regarding the recovery and disposal of the equipment, supplies, packing materials, used batteries and IC-RAMs including lithium batteries, follow the relevant local regulations or rules.

Caution:

Dispose of used batteries and IC-RAMs including lithium batteries according to this manual.

Attention:

Se débarrasser de batteries et IC-RAMs usés y compris les batteries en lithium selon ce manuel.

Vorsicht:

Entsorgung der gebrauchten Batterien und IC-RAMs (inclusive der Lithium-Batterie) nach diesem Handbuch.

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1. SYSTEM BLOCK DIAGRAM

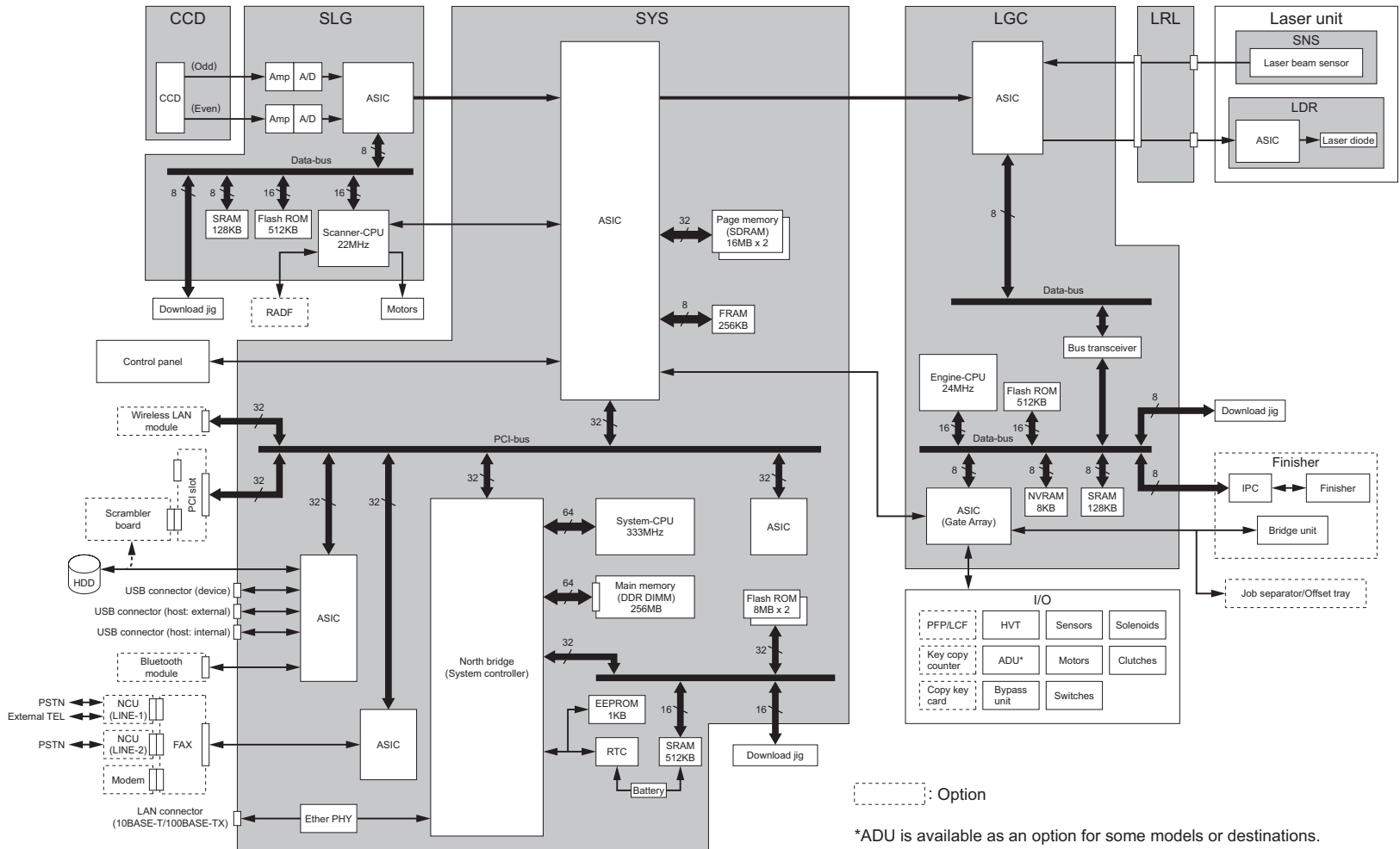


Fig. 1-1

2. GENERAL DESCRIPTION OF MAIN IC

2.1 Scanner CPU (TMP95C063F)

2.1.1 Outline and features

The TMP95C063F is developed as a high-speed, advanced 16-bit microcontroller for a range of mid to large-scale equipment.

This device is presented in a 144-pin plastic flat package. Its features are as follows.

- 1) Original high-speed 16-bit CPU (900H_CPU)
 - Instruction mnemonics upwardly compatible with TLCS-90/900
 - 16-Mbyte linear address space
 - General-purpose registers using register bank system
 - 16-bit multiplication/division instructions, bit transfer/arithmetic instructions
 - Micro DMA: 4 channels (640 ns/2 bytes at 25 MHz)
- 2) Minimum instruction execution time: 160 ns (at 25 MHz)
- 3) Internal RAM: No
Internal ROM: No
- 4) External memory expansion
 - Expandable up to 16 Mbytes (common to programs and data)
 - External data bus width selection pin (AM8/16)
 - Can use both 8- and 16-bit external buses
... Dynamic data bus sizing
- 5) Internal DRAM controller: 2 channels
 - $\overline{2CAS}/\overline{2WE}$ selectable
- 6) 8-bit timer: 8 channels
- 7) 16-bit timer: 2 channels
- 8) Pattern generator: 4 bits, 2 channels
- 9) General-purpose serial interface: 2 channels
 - Baud rate generated by external clock
- 10) 10-bit A/D converter: 8 channels
- 11) 8-bit D/A converter: 2 channels
- 12) Watchdog timer
- 13) Chip selector, wait controller: 4 blocks
- 14) Interrupt function:
 - CPU interrupts: 2 (software interrupt instructions, illegal instructions)
 - Internal interrupts: 22 (7 priority levels available)
 - External interrupts: 11 (7 priority levels available)
- 15) Input/output ports
 - 91 pins
- 16) Standby function
 - 3 HALT modes (RUN, IDLE, STOP)

2.1.2 Functions

The Scanner CPU interfaces with the System CPU and RADF, and controls the whole system of the scanning section such as the scan motor, APS sensor, exposure lamp and such. The Scanner CPU also sets the parameter of each image processing ASIC. These control programs of the Scanner CPU are stored in the Flash ROM on the SLG board. These programs can be updated by downloading the new programs with the download jig, PC which is serially connected and so on.

2.1.3 Pin assignment

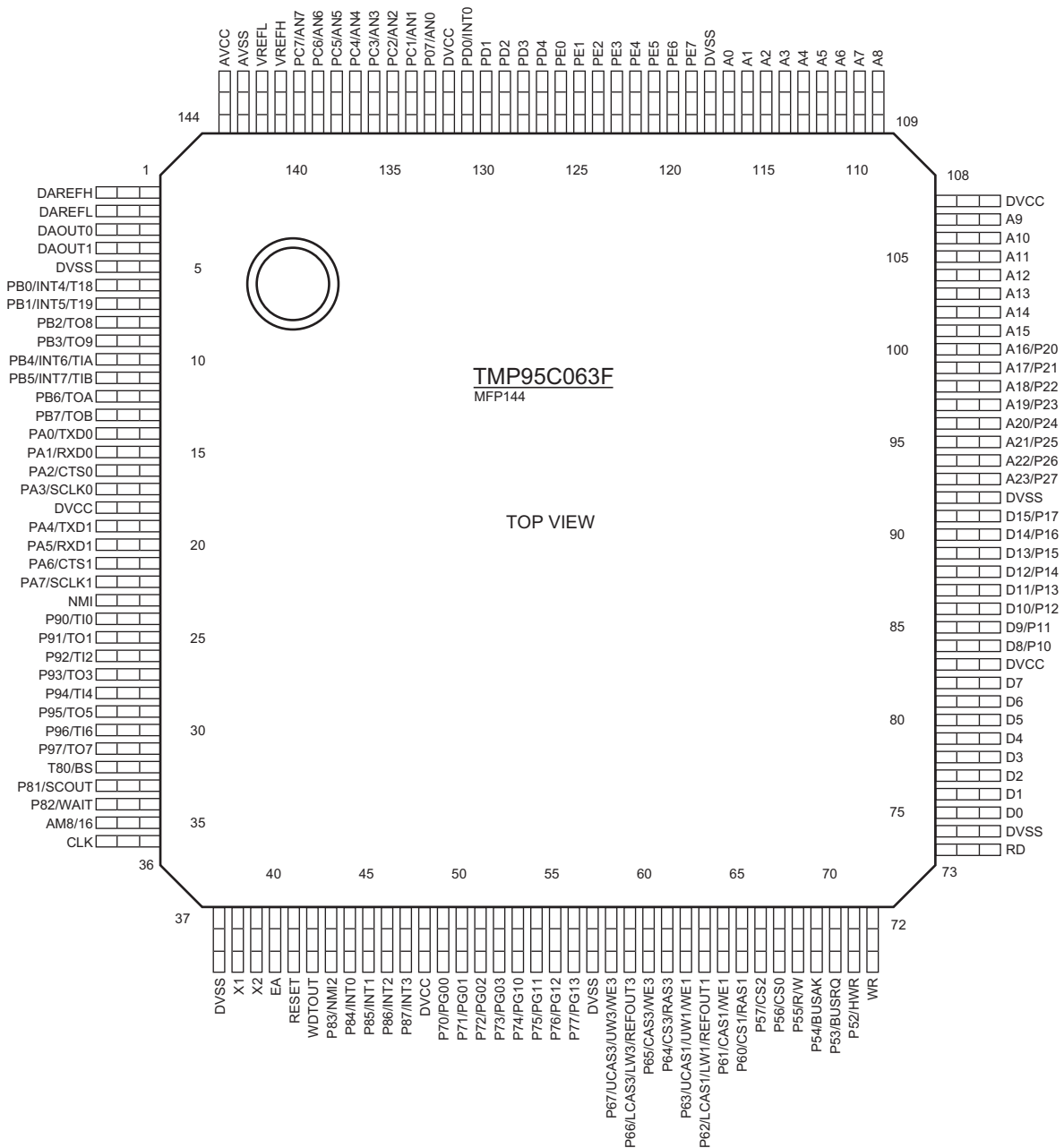


Fig. 2-1

2.1.4 Signals

Pin No.	Port name	Signal name	I/O	Function
1	DAREFH	DAREFH	I	Reference voltage (H) for D/A converter (+5V)
2	DAREFL	DAREFL	I	Reference voltage (L) for D/A converter (Signal ground)
3	DAOUT0	MOTREF	O	Reference voltage for scan motor
4	DAOUT1	-	-	Not used (Open)
5	DVSS1	SG	-	Signal ground
6	PB0/INT4/TI8	DFSCST	I	RADF scanning start signal
7	PB1/INT5/TI9	-	-	Not used (Open)
8	PB2/TO8	DFRAK	I	RADF acknowledge signal: SLG board <- RADF
9	PB3/TO9	EEMCLK	O	EEPROM clock
10	PB4/INT6/TIA	DFRRQ	I	RADF request signal: SLG board <- RADF
11	PB5/INT7/TIB	-	-	Not used (Open)
12	PB6/TOA	PNCNT	I	Debug panel connection signal (L: connected) (for debug)
13	PB7/TOB	SSW	I	Debug panel SW status signal (for debug)
14	PA0/TXD0	SRXD	O	Reception data: SLG board -> SYS board
15	PA1/RXD0	STXDA	I	Transmission data: SLG board <- SYS board
16	PA2/ $\overline{\text{CTS0}}$	SRTSA	I	Transmission request signal: SLG board <- SYS board
17	PA3/SCLK0	SCTS	O	Transmission clear signal: SLG board -> SYS board
18	DVCC1	DVCC	-	+5V
19	PA4/TXD1	DFTXD	O	Transmission data: SLG board -> RADF
20	PA5/RXD1	DFRXD	I	Reception data: SLG <- RADF
21	PA6/ $\overline{\text{CTS1}}$	DFAK	O	Acknowledge signal: SLG board -> RADF
22	PA7/SCLK1	DFRQ	O	Request signal: SLG -> RADF
23	$\overline{\text{NMI}}$	/NMI	I	Non-maskable Interrupt signal (Pull-up: +5V)
24	P90/TI0	EEMCS	O	EEPROM chip select signal
25	P91/TO1	MOTCLK	O	Scan motor drive clock
26	P92/TI2	-	-	Not used (Open)
27	P93/TO3	LED	O	Download jig LED drive signal
28	P94/TI4	EEMDTIN	I	EEPROM read data
29	P95/TO5	EEMDTOUT	O	EEPROM write data
30	P96/TI6	3BAPS1	O	Not used
31	P97/TO7	3BAPS2	O	Not used

Pin No.	Port name	Signal name	I/O	Function
32	P80/BS	3BAPS3	O	Not used
33	P81/SCOUT	-	-	Not used (Open)
34	P82/ $\overline{\text{WAIT}}$	-	-	Not used (Open)
35	AM8/ $\overline{\text{16}}$	WORD	I	Bus width selection signal (H: 8-bit fixed, L: 8/16-bit coexisting)
36	CLK	-	-	Not used (Open)
37	DVSS2	SG	-	Signal ground
38	X1	X1	I	Clock input (22MHz)
39	X2	X2	O	Clock output (22MHz)
40	$\overline{\text{EA}}$	/EA	I	Pull-down: signal ground
41	$\overline{\text{RESET}}$	MRST	I	Reset signal (Low-active)
42	$\overline{\text{WDTOUT}}$	WDTOUT	O	Watchdog output signal (H: CPU is normal, L: CPU is out of control)
43	P83/ $\overline{\text{NMI2}}$	-	-	Not used (Open)
44	P84/INT0	-	-	Not used (Open)
45	P85/INT1	-	-	Not used (Open)
46	P86/INT2	DFCOPY	-	Not used (Open)
47	P87/INT3	VSYNC	-	Not used (Open)
48	DVCC2	+5V	-	+5V
49	P70/PG00	DEBUG0	O	Debug signal [0]
50	P71/PG01	DEBUG1	O	Debug signal [1]
51	P72/PG02	DEBUG2	O	Debug signal [2]
52	P73/PG03	DEBUG3	O	Debug signal [3]
53	P74/PG10	DEBUG4	O	Debug signal [4]
54	P75/PG11	DEBUG5	O	Debug signal [5]
55	P76/PG12	DEBUG6	O	Debug signal [6]
56	P77/PG13	DEBUG7	O	Debug signal [7]
57	DVSS3	SG	-	Signal ground
58	P67/ $\overline{\text{UCAS3}}/\overline{\text{UW3}}/\overline{\text{WE3}}$	-	-	Not used (Open)
59	P66/ $\overline{\text{LCAS3}}/\overline{\text{LW3}}/\overline{\text{REFOUT3}}$	FANON	O	Not used
60	P65/ $\overline{\text{CAS3}}/\overline{\text{WE3}}$	FANCHG	O	Not used
61	P64/ $\overline{\text{CS3}}/\overline{\text{RAS3}}$	CS3	O	Chip select signal [3] (Low-active) * For Flash (When PC download mode)
62	P63/ $\overline{\text{UCAS}}/\overline{\text{UW1}}/\overline{\text{WE}}$	-	-	Not used (Open)
63	P62/ $\overline{\text{LCAS}}/\overline{\text{LW1}}/\overline{\text{REFOUT1}}$	LMPON	O	Exposure lamp ON signal (L: ON)


Pin No.	Port name	Signal name	I/O	Function
64	P61/ $\overline{\text{CAS1/WE1}}$	CCDPSOFF	-	Not used (Open)
65	P60/ $\overline{\text{CS1/RAS1}}$	CS1	O	Chip select signal [1] (Low-active) * For SRAM
66	P57/ $\overline{\text{CS2}}$	CS2	O	Chip select signal [2] (Low-active) * For Flash ROM
67	P56/ $\overline{\text{CS0}}$	CS0	O	Chip select signal [0] (Low-active) * For ASIC
68	P55/ $\overline{\text{R/W}}$	ASICWR	O	ASIC data bus input/output switching signal (H: input, L: output)
69	P54/ $\overline{\text{BUSAK}}$	PGNCNT	I	Not used
70	P53/ $\overline{\text{BUSRQ}}$	TSTSEL	I	Not used
71	P52/ $\overline{\text{HWR}}$	-	-	Not used (Open)
72	$\overline{\text{WR}}$	MWR	O	Write signal (Low-active)
73	$\overline{\text{RD}}$	MRD	O	Read signal (Low-active)
74	DVSS4	SG	-	Signal ground
75	D0	MDT[0]	I/O	Data bus [0]
76	D1	MDT[1]	I/O	Data bus [1]
77	D2	MDT[2]	I/O	Data bus [2]
78	D3	MDT[3]	I/O	Data bus [3]
79	D4	MDT[4]	I/O	Data bus [4]
80	D5	MDT[5]	I/O	Data bus [5]
81	D6	MDT[6]	I/O	Data bus [6]
82	D7	MDT[7]	I/O	Data bus [7]
83	DVCC3	+5V	-	+5V
84	D8/P10	MDT[8]	I/O	Data bus [8]
85	D9/P11	MDT[9]	I/O	Data bus [9]
86	D10/P12	MDT[10]	I/O	Data bus [10]
87	D11/P13	MDT[11]	I/O	Data bus [11]
88	D12/P14	MDT[12]	I/O	Data bus [12]
89	D13/P15	MDT[13]	I/O	Data bus [13]
90	D14/P16	MDT[14]	I/O	Data bus [14]
91	D15/P17	MDT[15]	I/O	Data bus [15]
92	DVSS5	SG	-	Signal ground
93	A23/P27	DWNLD	O	PC download enable signal (Low-active)
94	A22/P26	5VSWON	O	5VSW power supply signal (Low-active)
95	A21/P25	PNGT	O	Debug panel control signals ON/OFF signal (for debug)
96	A20/P24	-	-	Not used (Open)

Pin No.	Port name	Signal name	I/O	Function
97	A19/P23	SLEEP	O	ASIC sleep mode control signal (H: sleep mode)
98	A18/P22	MAD[18]	O	Address bus [18]
99	A17/P21	MAD[17]	O	Address bus [17]
100	A16/P20	MAD[16]	O	Address bus [16]
101	A15	MAD[15]	O	Address bus [15]
102	A14	MAD[14]	O	Address bus [14]
103	A13	MAD[13]	O	Address bus [13]
104	A12	MAD[12]	O	Address bus [12]
105	A11	MAD[11]	O	Address bus [11]
106	A10	MAD[10]	O	Address bus [10]
107	A9	MAD[9]	O	Address bus [9]
108	DVCC4	+5V	-	+5V
109	A8	MAD[8]	O	Address bus [8]
110	A7	MAD[7]	O	Address bus [7]
111	A6	MAD[6]	O	Address bus [6]
112	A5	MAD[5]	O	Address bus [5]
113	A4	MAD[4]	O	Address bus [4]
114	A3	MAD[3]	O	Address bus [3]
115	A2	MAD[2]	O	Address bus [2]
116	A1	MAD[1]	O	Address bus [1]
117	A0	MAD[0]	O	Address bus [0]
118	DVSS6	SG	-	Signal ground
119	PE7	PSYNC	O	Not used
120	PE6	APSON	O	APS sensor power supply control signal (H: supply, L: cut off)
121	PE5	-	-	Not used (Open)
122	PE4	MOTMD3	O	Scan motor control data [3]
123	PE3	MOTMD2	O	Scan motor control data [2]
124	PE2	MOTMD1	O	Scan motor control data [1]
125	PE1	MOTDIR	O	Scan motor rotational direction switch signal (H: CCW, L: CW)
126	PE0	MOTEN	O	Scan motor hold ON/OFF signal (H: ON, L: OFF)
127	PD4	ROMDT	I	Download jig connection signal (L: connected)
128	PD3	DFCNT	I	RADF connection signal (L: connected)
129	PD2	APS3	I	APS-3 sensor output signal (Low-active)
130	PD1	APS2	I	APS-2 sensor output signal (Low-active)

Pin No.	Port name	Signal name	I/O	Function
131	PD0/INT8	APS1	I	APS-1 sensor output signal (Low-active)
132	DVCC5	+5V	-	+5V
133	PC0/AN0	TSTMEM	I	Not used
134	PC1/AN1	3BAPSIN	I	Not used
135	PC2/AN2	+24VCHK	I	+24V voltage check
136	PC3/AN3	-	-	Signal ground
137	PC4/AN4	HOME	I	Carriage home position sensor detect signal (H: home position)
138	PC5/AN5	PLTN	I	Platen sensor detect signal (H: closed L: open)
139	PC6/AN6	APSC	I	APS-C sensor output signal (Low-active)
140	PC7/AN7	APSR	I	APS-R sensor output signal (Low-active)
141	VREFH	VREFH	I	Reference voltage (H) for A/D converter (+5V)
142	VREFL	VREFL	I	Reference voltage (L) for A/D converter (Signal ground)
143	AVSS	AVSS	I	A/D converter ground (Signal ground)
144	AVCC	AVCC	I	A/D converter power supply (+5V)

2.2 Engine CPU (TMP95C063F)


2.2.1 Outline and features

The Engine CPU employs the same elemental devices as those of the Scanner CPU. Refer to the following pages for the outline and features of these elemental devices.  P. 2-1 "2.1.1 Outline and features"

2.2.2 Functions

The Engine CPU interfaces with the System CPU, gate array, laser unit and finisher controller PC board (IPC board), and controls the whole system of the printer engine section. These control programs of the Engine CPU are stored in the Flash ROM on the LGC board. These programs can be updated by downloading the new programs with the download jig, PC which is serially connected and so on. The adjustment/setting value related with the control of engine section is stored in the removable NVRAM on the LGC board in order to prevent a data loss and simplify the data transfer process at the board replacement.

2.2.3 Pin assignment

The Engine CPU employs the same elemental devices as those of the Scanner CPU. Refer to the following pages for the pin assignment of these elemental devices.  P. 2-2 "2.1.3 Pin assignment"

2.2.4 Signals

Pin No.	Port name	Signal name	I/O	Function
1	DAREFH	DAREFH	I	Reference voltage (H) for D/A converter (+5V)
2	DAREFL	DAREFL	I	Reference voltage (L) for D/A converter (Signal ground)
3	DAOUT0	ADUVR-1	O	Reference voltage for ADU motor current restriction
4	DAOUT1	ATSVR-1	O	Reference voltage for Auto-toner sensor
5	DVSS1	SG	-	Signal ground
6	PB0/INT4/TI8	HTRSTOP-1	I	Fuser unit abnormality control signal (H: heater abnormal, L: normal)
7	PB1/INT5/TI9	OVERHEAT-1	I	Fuser unit overheating detection signal (H: overheated, L: normal)
8	PB2/TO8	PLLENM-0	O	Phase locked loop control enable signal for main clock (H: enable)
9	PB3/TO9	PLLENP-0	O	Phase locked loop control enable signal for printer clock (H: enable)
10	PB4/INT6/TIA	SCOUT-1	I	Timer clock input * From pin33
11	PB5/INT7/TIB	HVSDWN-1A	I	High-voltage transformer leakage detection signal (H: high-voltage transformer abnormal, L: normal)
12	PB6/TOA	POMCK-0	O	Polygonal motor reference clock
13	PB7/TOB	PS12NG-1	I	+12V supervisory signal (H: +12V abnormal L: normal)
14	PA0/TXD0	-	O	Not used
15	PA1/RXD0	-	O	Not used
16	PA2/ $\overline{\text{CTS0}}$	-	O	Not used
17	PA3/SCLK0	-	I	Not used
18	DVCC1	DVCC	-	+5V
19	PA4/TXD1	-	O	Not used
20	PA5/RXD1	-	O	Not used
21	PA6/ $\overline{\text{CTS1}}$	LED-1	O	Download jig LED drive signal (L: LED ON)
22	PA7/SCLK1	FMBSY-0	I	Flash ROM status signal (H: ready, L: busy)
23	$\overline{\text{NMI}}$	/NMI	I	Non-maskable Interrupt signal (Pull-up: +5V)
24	P90/TI0	-	I	Not used
25	P91/TO1	-	I	Not used
26	P92/TI2	-	I	Not used
27	P93/TO3	YDRV-0	O	Not used
28	P94/TI4	SCOUT-1	I	Timer clock input * From pin33

Pin No.	Port name	Signal name	I/O	Function
29	P95/TO5	-	-	Not used
30	P96/TO6	-	-	-
31	P97/TO7	-	-	-
32	P80/BS	PS5SNG-1	I	+5VSW supervisory signal (H: +5VSW abnormal, L: normal)
33	P81/SCOUT	SCOUT	O	Timer clock output * To pins10 and 28
34	P82/ $\overline{\text{WAIT}}$	YFAN2L-0	O	Not used
35	AM8/ $\overline{\text{16}}$	ROMDT-1	I	Bus width selection signal (H: 8-bit fixed, L: 8/16-bit coexisting)
36	CLK	-	-	Not used (Open)
37	DVSS2	SG	-	Signal ground
38	X1	X1	I	Clock input (24MHz)
39	X2	X2	O	Clock output (24MHz)
40	$\overline{\text{EA}}$	/EA	I	Pull-down: signal ground
41	$\overline{\text{RESET}}$	CPURST-0	I	Reset signal (Low-active)
42	$\overline{\text{WDTOU}}$	WDT-0	O	Watchdog output signal (H: CPU is normal, L: CPU is out of control)
43	P83/ $\overline{\text{NMI2}}$	YFAN2H-0	O	Not used
44	P84/INT0	STINT-1	I	Transmission interrupt signal: LGC board -> SYS board
45	P85/INT1	HSCTCP-1A	I	H-sync counter coincidence status signal (H: coincided, L: not coincided)
46	P86/INT2	CMINT-1	I	Reception interrupt signal: LGC board <- SYS board
47	P87/INT3	PDWN-1	I	Switching regulator power down signal (H: regulator ON or OFF, L: normal)
48	DVCC2	+5V	-	+5V
49	P70/PG00	ADUM1A-0	O	ADU motor drive signal [phase-A] (Low-active)
50	P71/PG01	ADUM1B-0	O	ADU motor drive signal [phase-B] (Low-active)
51	P72/PG02	ADUM1C-0	O	ADU motor drive signal [phase-C] (Low-active)
52	P73/PG03	ADUM1D-0	O	ADU motor drive signal [phase-D] (Low-active)
53	P74/PG10	EXTMA-0	O	Exit motor drive signal [phase-A] (Low-active)
54	P75/PG11	EXTMB-0	O	Exit motor drive signal [phase-B] (Low-active)
55	P76/PG12	EXTMC-0	O	Exit motor drive signal [phase-C] (Low-active)
56	P77/PG13	EXTMD-0	O	Exit motor drive signal [phase-D] (Low-active)
57	DVSS3	SG	-	Signal ground
58	P67/ $\overline{\text{UCAS3/UW3/WE3}}$	PWRFNL-0	O	Internal cooling fan-2 low speed drive signal

Pin No.	Port name	Signal name	I/O	Function
59	P66/ $\overline{\text{LCAS3/LW3}}$ / REFOUT3	PWRFNH-0	O	Internal cooling fan-2 high speed drive signal PWRFNH-0 PWRFNL-0 Status L L High speed drive L H High speed drive H L Low speed drive H H Stop
60	P65/ $\overline{\text{CAS3/WE3}}$	RSTSW1-0	O	Main switch reset signal (H: normal L: reset (power is turn OFF))
61	P64/ $\overline{\text{CS3/RAS3}}$	CS3-0	O	Chip select signal [3] (Low-active) * For SRAM
62	P63/ $\overline{\text{UCAS/UW1/WE}}$	ERSLP-0	O	Discharger LED drive signal (L: ON)
63	P62/ $\overline{\text{LCAS/LW1/REFOUT1}}$	CLNFNL-0	O	Internal cooling fan-1 low speed drive signal
64	P61/ $\overline{\text{CAS1/WE1}}$	CLNFNH-0	O	Internal cooling fan-1 high speed drive signal CLNFNH-0 CLNFNL-0 Status L L High speed drive L H High speed drive H L Low speed drive H H Stop
65	P60/ $\overline{\text{CS1/RAS1}}$	CS1-0	O	Chip select signal [1] (Low-active) * For Gate Array (EC/N075: IC24)
66	P57/ $\overline{\text{CS2}}$	CS2-0	O	Chip select signal [2] (Low-active) * For Flash ROM
67	P56/ $\overline{\text{CS0}}$	CS0-0	O	Chip select signal [0] (Low-active) * For ASIC
68	P55/ $\overline{\text{R/W}}$	RW-0	O	Read/write signal (H: read, L: write) * For IPC bus direction
69	P54/ $\overline{\text{BUSAK}}$	POMON-0	O	Polygonal motor drive signal (H: OFF, L: ON)
70	P53/ $\overline{\text{BUSRQ}}$	POMPL-0	I	Polygonal motor phase locked loop control signal (H: stop or error, L: uniform speed driving)
71	P52/ $\overline{\text{HWR}}$	POMDT-0	I	Download jig connection signal (L: connected)
72	$\overline{\text{WR}}$	WR-0	O	Write signal (Low-active)
73	$\overline{\text{RD}}$	RD-0	O	Read signal (Low-active)
74	DVSS4	SG	-	Signal ground
75	D0	D[0]	I/O	Data bus [0]
76	D1	D[1]	I/O	Data bus [1]
77	D2	D[2]	I/O	Data bus [2]
78	D3	D[3]	I/O	Data bus [3]
79	D4	D[4]	I/O	Data bus [4]
80	D5	D[5]	I/O	Data bus [5]
81	D6	D[6]	I/O	Data bus [6]
82	D7	D[7]	I/O	Data bus [7]
83	DVCC3	+5V	-	+5V

Pin No.	Port name	Signal name	I/O	Function
84	D8/P10	D[8]	I/O	Data bus [8]
85	D9/P11	D[9]	I/O	Data bus [9]
86	D10/P12	D[10]	I/O	Data bus [10]
87	D11/P13	D[11]	I/O	Data bus [11]
88	D12/P14	D[12]	I/O	Data bus [12]
89	D13/P15	D[13]	I/O	Data bus [13]
90	D14/P16	D[14]	I/O	Data bus [14]
91	D15/P17	D[15]	I/O	Data bus [15]
92	DVSS5	SG	-	Signal ground
93	A23/P27	A[23]	O	Address bus [23] * For generation of Flash ROM chip select signal
94	A22/P26	A[22]	O	Address bus [22] * For generation of Flash ROM chip select signal
95	A21/P25	-	-	Not used (Open)
96	A20/P24	-	-	Not used (Open)
97	A19/P23	WDE-0	O	Watchdog enable signal (H: enable)
98	A18/P22	A[18]	O	Address bus [18]
99	A17/P21	A[17]	O	Address bus [17]
100	A16/P20	A[16]	O	Address bus [16]
101	A15	A[15]	O	Address bus [15]
102	A14	A[14]	O	Address bus [14]
103	A13	A[13]	O	Address bus [13]
104	A12	A[12]	O	Address bus [12]
105	A11	A[11]	O	Address bus [11]
106	A10	A[10]	O	Address bus [10]
107	A9	A[9]	O	Address bus [9]
108	DVCC4	+5V	-	+5V
109	A8	A[8]	O	Address bus [8]
110	A7	A[7]	O	Address bus [7]
111	A6	A[6]	O	Address bus [6]
112	A5	A[5]	O	Address bus [5]
113	A4	A[4]	O	Address bus [4]
114	A3	A[3]	O	Address bus [3]
115	A2	A[2]	O	Address bus [2]
116	A1	A[1]	O	Address bus [1]
117	A0	A[0]	O	Address bus [0]

Pin No.	Port name	Signal name	I/O	Function
118	DVSS6	SG	-	Signal ground
119	PE7	LDOFF-0	O	Enforced laser OFF signal (H: normal, L: laser turn OFF)
120	PE6	LE-0	O	Laser enable signal (H: laser turn ON disable, L: laser turn ON enable)
121	PE5	GCCTCP-1A	I	Pixel counter coincidence status signal (H: coincided, L: not coincided)
122	PE4	EWSCN-0	I	Not used
123	PE3	BUSEN-1	O	Not used
124	PE2	CSCHG-0	O	Chip select circuit switch signal (H: ASIC selected, L: normal)
125	PE1	FCOVSW-1	I	Front cover opening/closing switch detection signal (H: opened, L: closed)
126	PE0	PSTPSW-1	I	Registration sensor detection signal (H: paper transport, L: none)
127	PD4	MVDEN-0	O	Paper transport signal (H: standby, L: paper transport)
128	PD3	PVDEN-0A	I	VDEN signal (H: standby, L: printing)
129	PD2	ERR1-1A	I	H-Sync/PWM calibration error detection signal (H: error)
130	PD1	LDON-0	O	Laser ON signal (H: OFF, L: ON)
131	PD0/INT8	CSTCSW-1	I	Side cover opening/closing sensor detection signal (H: opened, L: closed)
132	DVCC5	+5V	-	+5V
133	PC0/AN0	HMS-1	I	Temperature/humidity sensor detection signal (Analog signal) * humidity detection
134	PC1/AN1	TEMP-1	I	Temperature/humidity sensor detection signal (Analog signal) * temperature detection
135	PC2/AN2	DRTH-1	I	Drum thermistor detection signal (Analog signal)
136	PC3/AN3	FCOV2-1	I	Cover opening/closing status detection signal (Analog signal) * +24V(+24VD2) supply status detection
137	PC4/AN4	MTH--1A	I	Center thermistor detection signal (Analog signal)
138	PC5/AN5	STH--1A	I	Side thermistor detection signal (Analog signal)
139	PC6/AN6	ETH--1A	I	Edge thermistor detection signal (Analog signal)
140	PC7/AN7	ATS-1	I	Auto-toner sensor detection signal (Analog signal)
141	VREFH	VREFH	I	Reference voltage (H) for A/D converter (+5V)

Pin No.	Port name	Signal name	I/O	Function
142	VREFL	VREFL	I	Reference voltage (L) for A/D converter (Signal ground)
143	AVSS	AVSS	I	A/D converter ground (Signal ground)
144	AVCC	AVCC	I	A/D converter power supply (+5V)

2.3 Gate Array (EC/N075)

2.3.1 Functions

The gate array is controlled by command from the Engine CPU and the logic circuit inside the gate array. The primary functions of the gate array are as follows.

- I/O control of each electrical part (motor, sensor, switch, electromagnetic spring clutch, solenoid, etc.)
- Interface to control the bypass unit and ADU
- Interface to control the high-voltage transformer
- Interface to control the PFP, LCF and finisher
- Interface to control the NVRAM on the LGC board
(An erroneous data loss is prevented with a key circuit provided when the CPU is running away.)

2.3.2 Pin assignment

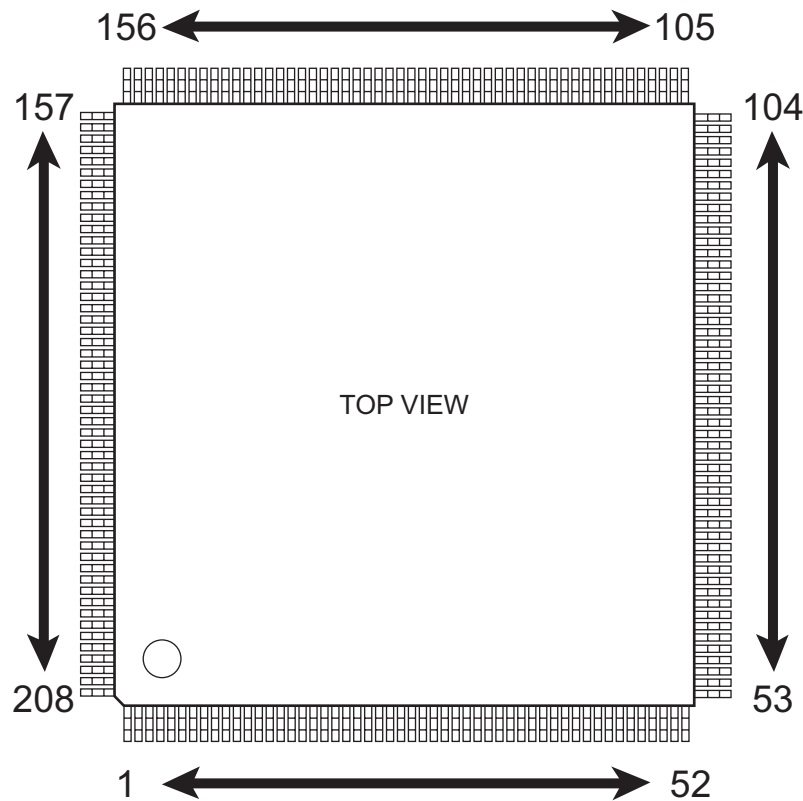




Fig. 2-2

2.3.3 Signals








Pin No.	Port name	Signal name	I/O	Function															
1	LVDD1	+3.3V	-	+3.3V															
2	PA4	-	O	Upper transport clutch drive request signal (H: OFF, L: ON) * To pin202															
3	PA5	1STCLL-0	O	Middle transport clutch drive signal (H: OFF, L: ON) * It is also a middle transport clutch drive request signal (To pin203)															
4	PA6	CLTRM-0	O	Tray-up motor control signal [1]															
5	PA7	CLTRM-1	O	Tray-up motor control signal [2] <table border="1"> <thead> <tr> <th>CLTRM-1</th> <th>CLTRM-0</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>OFF</td> </tr> <tr> <td>L</td> <td>H</td> <td>CCW</td> </tr> <tr> <td>H</td> <td>L</td> <td>CW</td> </tr> <tr> <td>H</td> <td>H</td> <td>Break</td> </tr> </tbody> </table>	CLTRM-1	CLTRM-0	Status	L	L	OFF	L	H	CCW	H	L	CW	H	H	Break
CLTRM-1	CLTRM-0	Status																	
L	L	OFF																	
L	H	CCW																	
H	L	CW																	
H	H	Break																	
6	HVSS1	SG	-	Signal ground															
7	PB0	ATSCNT-1	I	Auto-toner sensor connection signal (L: connected)															
8	PB1	HTBOXSW-1	I	Not used															
9	PB2	TNFULL-1	I	Auger lock switch detection signal (H: full of recycled toner, L: normal)															
10	PB3	TNRSW-1	I	Toner cartridge installation switch detection signal (H: cartridge absence, L: cartridge presence)															
11	HVSS2	SG	-	Signal ground															
12	PB4	MAMPL-1	I	Main motor phase locked loop control signal (H: stop or error, L: uniform speed driving)															
13	PB5	1STFED-1	I	1st transport sensor detection signal (H: paper transport L: none)															
14	PB6	2NDFED-1	I	2nd transport sensor detection signal (H: paper transport L: none)															
15	PB7	SDCSW-1	I	Transfer cover opening/closing switch detection signal (H: opened, L: closed)															
16	HVDD	+5V	-	+5V															
17	PC0	TNRM-0	O	Toner motor control signal [1]															
18	PC1	TNRM-1	O	Toner motor control signal [2] <table border="1"> <thead> <tr> <th>TNRM-1</th> <th>TNRM-0</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>OFF</td> </tr> <tr> <td>L</td> <td>H</td> <td>CCW</td> </tr> <tr> <td>H</td> <td>L</td> <td>CW</td> </tr> <tr> <td>H</td> <td>H</td> <td>Break</td> </tr> </tbody> </table>	TNRM-1	TNRM-0	Status	L	L	OFF	L	H	CCW	H	L	CW	H	H	Break
TNRM-1	TNRM-0	Status																	
L	L	OFF																	
L	H	CCW																	
H	L	CW																	
H	H	Break																	
19	PC2	RGTCCL-0	O	Registration roller clutch drive signal (H: OFF, L: ON)															
20	PC3	MAMON-0	O	Main motor ON signal (H: OFF, L: ON)															
21	HVSS3	SG	-	Signal ground															
22	PC4	MAMBK-0	O	Main motor brake signal (L: brake)															











Pin No.	Port name	Signal name	I/O	Function
23	PC5	MAMCW-1	O	Main motor rotational direction switch signal (H: CCW, L: CW)
24	PC6	CLKB-1	O	PFP/LCF signal output switch signal [1] (Up-edge trigger) *  P. 2-25 "[2] Description of signals DRV [0]-[7]"
25	PC7	CLKC-1	O	PFP/LCF signal output switch signal [2] (Up-edge trigger) *  P. 2-25 "[2] Description of signals DRV [0]-[7]"
26	LVSS1	SG	-	Signal ground
27	LVDD2	+3.3V	-	+3.3V
28	HVDD2	+5V	-	+5V
29	A0	A[0]	I	Address bus [0]
30	A1	A[1]	I	Address bus [1]
31	A2	A[2]	I	Address bus [2]
32	A3	A[3]	I	Address bus [3]
33	A4	A[4]	I	Address bus [4]
34	A5	A[5]	I	Address bus [5]
35	HVSS4	SG	-	Signal ground
36	A6	A[6]	I	Address bus [6]
37	A7	A[7]	I	Address bus [7]
38	A12	A[12]	I	Address bus [12]
39	A13	A[13]	I	Address bus [13]
40	A14	A[14]	I	Address bus [14]
41	HVDD3	+5V	-	+5V
42	D0	D[0]	I/O	Data bus [0]
43	D1	D[1]	I/O	Data bus [1]
44	D2	D[2]	I/O	Data bus [2]
45	D3	D[3]	I/O	Data bus [3]
46	HVSS5	SG	-	Signal ground
47	D4	D[4]	I/O	Data bus [4]
48	D5	D[5]	I/O	Data bus [5]
49	D6	D[6]	I/O	Data bus [6]
50	D7	D[7]	I/O	Data bus [7]
51	HVSS6	SG	-	Signal ground
52	LVSS2	SG	-	Signal ground
53	LVDD3	+3.3V	-	+3.3V
54	RD	RD-0	I	Read signal (Low-active)

Pin No.	Port name	Signal name	I/O	Function
55	WR	WR-0	I	Write signal (Low-active)
56	CS	CS1-0	I	Chip select signal [1] (Low-active) * For Gate Array (EC/N075: IC24)
57	HVSS7	SG	-	Signal ground
58	CTS	-	-	Pull-up: +5V
59	RXD	-	-	Pull-up: +5V
60	CBSY	CBSY-0	I	System interface command busy signal
61	CMD	CMD-0	I	System interface received data signal
62	SACK	SACK-0	I	System interface status acknowledge signal
63	SERR	SERR-0	I	System interface status error signal
64	HVDD4	+5V	-	+5V
65	RXDINT	-	-	Not used (Open)
66	TXDINT	-	-	Not used (Open)
67	CMDINT	CMINT-1	O	System interface reception interrupt signal
68	STSINT	STINT-1	O	System interface transmission interrupt signal
69	RTS	-	-	Not used (Open)
70	HVSS8	SG	-	Signal ground
71	TXD	-	-	Not used (Open)
72	SBSY	SBSY-0	O	System interface status busy signal
73	STS	STS	O	System interface transmitted data signal
74	CACK	CACK-0	O	System interface command acknowledge signal
75	CERR	CERR-0	O	System interface command error signal
76	HVSS9	SG	-	Signal ground
77	SCLK	-	-	Pull-up: +5V
78	HVDD5	+5V	-	+5V
79	RESET	GARST-0	I	Reset signal (Low-active)
80	HVSS10	SG	-	Signal ground
81	CNTRST	-	-	Pull-up: +5V
82	TESTSW	-	-	Pull-down: signal ground
83	TSTEN	-	-	Pull-down: signal ground
84	LVSS3	SG	-	Signal ground
85	PD0	TSIZE0-1	O	Paper size signal [0] for copy key card
86	PD1	TSIZE1-1	O	Paper size signal [1] for copy key card
87	PD2	TSIZE2-1	O	Paper size signal [2] for copy key card
88	PD3	TSIZE3-1	O	Paper size signal [3] for copy key card
89	LVDD4	+3.3V	-	+3.3V

Pin No.	Port name	Signal name	I/O	Function
90	PD4	FLCTR-0	O	Back-side printing count signal for copy key card
91	PD5	MNCTR-0	O	Mono color printing count signal for copy key card
92	PD6	BKCTR-0	O	Black printing count signal for copy key card
93	PD7	EXTCTR-0	O	Paper exit signal for coin controller
94	HVSS11	SG	-	Signal ground
95	PE0	MCRUN-0	O	Equipment operation status signal for copy key card
96	PE1	CTRON-0	O	Total count signal for copy key card
97	PE2	KCTRON-0	O	ON signal for key copy counter
98	PE3	HVTM-0	O	Charger/grid bias ON signal (L: ON)
99	HVSS12	SG	-	Signal ground
100	PE4	HVTT-0	O	Transfer bias ON signal (L: ON)
101	PE5	HVTAC-0	O	Developer AC bias ON signal (L: ON)
102	PE6	HVTSP-0	O	Separation bias ON signal (L: ON)
103	PE7	HVTGB-0	O	Transfer guide bias ON signal (L: ON)
104	HVDD6	+5V	-	+5V
105	HVSS13	SG	-	Signal ground
106	OSC1	OSC1	I	Clock input (8.334MHz)
107	HVDD7	+5V	-	+5V
108	OSC2	OSC2	O	Clock output (8.334MHz)
109	HVSS14	SG	-	Signal ground
110	DICH1	DADAT1-1	O	D/A converter serial data
111	LDCH1	DALTH1-1	O	D/A converter latch signal
112	CLKCH1	DACLK1-1	O	D/A converter serial data transfer clock
113	DICH2	-	-	Not used (Open)
114	LDCH2	-	-	Not used (Open)
115	CLKCH2	-	-	Not used (Open)
116	HVDD8	+5V	-	+5V
117	PF0	YSNR1-1	I	Not used
118	PF1	CTRCNT2-0	I	Copy enable signal for copy key card / coin controller
119	PF2	CKCTR0-0	I	Not used
120	PF3	KCTRC-0	I	Key copy counter connection signal (L: connected)
121	LVSS4	SG	-	Signal ground
122	PF4	YSNR2-1	I	Not used
123	PF5	IPCSW-0	I	IPC board (finisher controller) connection signal (L: connected)

Pin No.	Port name	Signal name	I/O	Function
124	PF6	EXTSW-1	I	Exit sensor detection signal (H: paper transport L: none)
125	PF7	FUSCNT-1	I	Fuser unit connection signal (L: connected)
126	HVSS15	SG	-	Signal ground
127	PG0	VCMFNH-0	O	Exhaust fan high speed drive signal
128	PG1	VCMFNL-0	O	Exhaust fan low speed drive signal VCMFNH-0 VCMFNL-0 Status L L High speed drive L H High speed drive H L Low speed drive H H Stop
129	PG2	HTRMODE-1	O	Fuser unit operation mode signal (H: warming-up, L: normal)
130	PG3	GASOL-0	O	Gate solenoid drive signal for option (H: OFF, L: ON) • Bridge unit (H: to finisher, L: to inner receiving tray) • Job separator (H: to upper tray, L: to lower tray) • Offset tray (H: to ADU pass, L: to OCT pass)
131	LVDD5	+3.3V	-	+3.3V
132	PG4	OFFSET1	O	OCT motor control signal [1] * For offset tray
133	PG5	OFFSET2	O	OCT motor control signal [2] * For offset tray OFFSET1 OFFSET2 L L OFF L H Paper exit to front side H L Paper exit to rear side H H Break
134	PG6	YFAN1H-0	O	Not used
135	PG7	YFAN1L-0	O	Not used
136	HVSS16	SG	-	Signal ground
137	PH0	SFBCL1-0	O	Bypass feed clutch drive signal (H: OFF, L: ON)
138	PH1	SFBCL2-0	O	Bypass pickup solenoid drive signal (H: OFF, L: ON (pickup))
139	PH2	ADUCL-0	O	ADU clutch drive signal (H: OFF, L: ON)
140	PH3	HTR1ON-0	O	Center heater lamp control signal (H: OFF, L: ON)
141	HVDD9	+5V	-	+5V
142	PH4	HTR2ON-0	O	Side heater lamp control signal (H: OFF, L: ON)
143	PH5	2NDCL-0	O	Lower transport clutch drive signal (H: OFF, L: ON)
144	PH6	CURGC-0	O	Upper drawer feed clutch drive signal (H: OFF, L: ON)
145	PH7	CLRGC-0	O	Lower drawer feed clutch drive signal (H: OFF, L: ON)
146	HVSS17	SG	-	Signal ground
147	PI0	SFBCNT-1	I	Bypass unit connection signal (L: connected)

Pin No.	Port name	Signal name	I/O	Function
148	PI1	SFBEMP-1	I	Bypass paper sensor detection signal (H: paper absence L: paper presence)
149	PI2	SFBTRY-1	I	Not used
150	PI3	LCCNT-0	I	PFP/LCF connection signal (L: connected)
151	HVSS18	SG	-	Signal ground
152	PI4	SIZE[0]	I	Paper/drawer detection sensor/switch detection signal [0] *  P. 2-24 "[1] Description of signals SIZE [0]-[3]"
153	PI5	SIZE[1]	I	Paper/drawer detection sensor/switch detection signal [1] *  P. 2-24 "[1] Description of signals SIZE [0]-[3]"
154	PI6	SIZE[2]	I	Paper/drawer detection sensor/switch detection signal [2] *  P. 2-24 "[1] Description of signals SIZE [0]-[3]"
155	PI7	SIZE[3]	I	Paper/drawer detection sensor/switch detection signal [3] *  P. 2-24 "[1] Description of signals SIZE [0]-[3]"
156	HVSS19	SG	-	Signal ground
157	HVDD10	+5V	-	+5V
158	DCCLK1	MAMCK-1	O	Main motor reference clock
159	DCCLK2	HVCLK-1	O	Not used (Open)
160	DCCLK3	-	-	Not used (Open)
161	DCCLK4	-	-	Not used (Open)
162	HVSS20	SG	-	Signal ground
163	SM_A	-	-	Not used (Open)
164	SM_B	-	-	Not used (Open)
165	SM_NA	-	-	Not used (Open)
166	SM_NB	-	-	Not used (Open)
167	HVSS21	SG	-	Signal ground
168	SMCLK	-	-	Pull-up: +5V
169	HVDD11	+5V	-	+5V
170	PJ0	DRV[0]	O	PFP/LCF output signal [0] *  P. 2-25 "[2] Description of signals DRV [0]-[7]"
171	PJ1	DRV[1]	O	PFP/LCF output signal [1] *  P. 2-25 "[2] Description of signals DRV [0]-[7]"
172	PJ2	DRV[2]	O	PFP/LCF output signal [2] *  P. 2-25 "[2] Description of signals DRV [0]-[7]"

Pin No.	Port name	Signal name	I/O	Function
173	PJ3	DRV[3]	O	PFP/LCF output signal [3] *  P. 2-25 "[2] Description of signals DRV [0]-[7]"
174	HVSS22	SG	-	Signal ground
175	PJ4	DRV[4]	O	PFP/LCF output signal [4] *  P. 2-25 "[2] Description of signals DRV [0]-[7]"
176	PJ5	DRV[5]	O	PFP/LCF output signal [5] *  P. 2-25 "[2] Description of signals DRV [0]-[7]"
177	PJ6	DRV[6]	O	PFP/LCF output signal [6] *  P. 2-25 "[2] Description of signals DRV [0]-[7]"
178	PJ7	DRV[7]	O	PFP/LCF output signal [7] *  P. 2-25 "[2] Description of signals DRV [0]-[7]"
179	HVSS23	SG	-	Signal ground
180	MWR	WRRAM-0	O	Write enable signal for NVRAM (Low-active)
181	SMINT	-	-	Not used (Open)
182	LVDD6	+3.3V	-	+3.3V
183	CS0	-	-	Not used (Open)
184	CS1	CSRAM-0	O	Chip select signal [1] (Low-active) * For NVRAM
185	CS2	-	-	Not used (Open)
186	CS3	CSIPC-0	O	Chip select signal [3] (Low-active) * For IPC board (finisher controller)
187	CS4	-	-	Not used (Open)
188	CS5	-	-	Not used (Open)
189	HVSS24	SG	-	Signal ground
190	PK0	RETS[0]	I	Paper feeding section / PFP / LCF input signal [0] *  P. 2-27 "[3] Description of signals RETS [0]-[7]"
191	PK1	RETS[1]	I	Paper feeding section / PFP / LCF input signal [1] *  P. 2-27 "[3] Description of signals RETS [0]-[7]"
192	PK2	RETS[2]	I	Paper feeding section / PFP / LCF input signal [2] *  P. 2-27 "[3] Description of signals RETS [0]-[7]"
193	PK3	RETS[3]	I	Paper feeding section / PFP / LCF input signal [3] *  P. 2-27 "[3] Description of signals RETS [0]-[7]"
194	LVSS5	SG	-	Signal ground
195	PK4	RETS[4]	I	Paper feeding section / PFP / LCF input signal [4] *  P. 2-27 "[3] Description of signals RETS [0]-[7]"

Pin No.	Port name	Signal name	I/O	Function									
196	PK5	RETS[5]	I	Paper feeding section / PFP / LCF input signal [5] * P. 2-27 "[3] Description of signals RETS [0]-[7]"									
197	PK6	RETS[6]	I	Paper feeding section / PFP / LCF input signal [6] * P. 2-27 "[3] Description of signals RETS [0]-[7]"									
198	PK7	RETS[7]	I	Paper feeding section / PFP / LCF input signal [7] * P. 2-27 "[3] Description of signals RETS [0]-[7]"									
199	HVDD12	+5V	-	+5V									
200	MULTD0	-	-	Pull-up: +5V									
201	MULTD1	-	I	Upper transport clutch drive request signal input * From pin2									
202	MULTA	1STCLL-0	I	Middle transport clutch drive request signal input * From pin3									
203	MULTY	1STCLH-0	O	Upper transport clutch drive signal (H: OFF, L: ON) * The drive conditions of the upper transport clutch are as follows. <table border="0"> <tr> <td>Pin201</td> <td>Pin202</td> <td>Upper transport clutch</td> </tr> <tr> <td>L</td> <td>L</td> <td>OFF</td> </tr> <tr> <td>L</td> <td>H</td> <td>ON</td> </tr> </table>	Pin201	Pin202	Upper transport clutch	L	L	OFF	L	H	ON
Pin201	Pin202	Upper transport clutch											
L	L	OFF											
L	H	ON											
204	PA0	SCSWA-0	O	Paper feeding section bus buffer enable signal [A] (Low-active) * For bypass unit and bridge unit / job separator / offset tray section * P. 2-24 "[1] Description of signals SIZE [0]-[3]" P. 2-27 "[3] Description of signals RETS [0]-[7]"									
205	PA1	SCSWB-0	O	Paper feeding section bus buffer enable signal [B] (Low-active) * For PFP/LCF section * P. 2-24 "[1] Description of signals SIZE [0]-[3]" P. 2-27 "[3] Description of signals RETS [0]-[7]"									
206	PA2	SCSWC-0	O	Paper feeding section bus buffer enable signal [C] (Low-active) * For PFP/LCF section * P. 2-24 "[1] Description of signals SIZE [0]-[3]" P. 2-27 "[3] Description of signals RETS [0]-[7]"									
207	PA3	SCSWD-0	O	Paper feeding section bus buffer enable signal [D] (Low-active) * For ADU and upper/lower drawer section * P. 2-24 "[1] Description of signals SIZE [0]-[3]" P. 2-27 "[3] Description of signals RETS [0]-[7]"									
208	LVSS6	SG	-	Signal ground									

[1] Description of signals SIZE [0]-[3]

The following functions are assigned to the signals SIZE [0]-[3] depending on each status of SCSWA-D-0 signals.

[1-1] When SCSWA-0 = Low:

Signal name	Function
SIZE[0]	Bypass unit slide guide width detection signal [0] (Low-active)
SIZE[1]	Bypass unit slide guide width detection signal [1] (Low-active)
SIZE[2]	Bypass unit slide guide width detection signal [2] (Low-active)
SIZE[3]	Not used

[1-2] When SCSWB-0 = Low:

Signal name	Function
SIZE[0]	PFP upper drawer detection switch detection signal (H: drawer opened, L: drawer closed)
SIZE[1]	Not used
SIZE[2]	Not used
SIZE[3]	Not used

[1-3] When SCSWC-0 = Low:

Signal name	Function
SIZE[0]	PFP lower drawer detection switch detection signal (H: drawer opened, L: drawer closed)
SIZE[1]	Not used
SIZE[2]	Not used
SIZE[3]	Not used

[1-4] When SCSWD-0 = Low:

Signal name	Function
SIZE[0]	ADU entrance sensor detection signal (H: paper transport, L: none)
SIZE[1]	ADU exit sensor detection signal (H: paper transport, L: none)
SIZE[2]	ADU opening/closing switch detection signal (H: ADU opened L: ADU closed)
SIZE[3]	ADU connection signal (L: connected)

[2] Description of signals DRV [0]-[7]

The following functions are assigned to the signals DRV [0]-[7] depending on the installation status of the PFP and LCF. These signals are latched by the up-edge trigger of the CLKB-1 or CLKC-1 signal.

[2-1] When CLKB-1 = Up-edge trigger and PFP is installed:

Signal name	Function
DRV[0]	PFP motor drive signal [A]
DRV[1]	PFP motor drive signal [B] DRV[1] DRV[0] Status L L Break L H ON H L Not used H H OFF
DRV[2]	Not used
DRV[3]	Not used
DRV[4]	PFP upper drawer feed clutch drive signal (H: OFF, L: ON)
DRV[5]	PFP lower drawer feed clutch drive signal (H: OFF, L: ON)
DRV[6]	PFP transport clutch drive signal (H: OFF, L: ON)
DRV[7]	Not used

[2-2] When CLKB-1 = Up-edge trigger and LCF is installed:

Signal name	Function
DRV[0]	LCF transport motor drive signal (H: ON)
DRV[1]	LCF transport motor speed switch signal (H: low speed drive, L: high speed drive)
DRV[2]	LCF transport clutch drive signal (H: OFF, L: ON)
DRV[3]	LCF feed clutch drive signal (H: OFF, L: ON)
DRV[4]	LCF pickup solenoid drive signal (H: OFF, L: ON)
DRV[5]	Not used
DRV[6]	Not used
DRV[7]	Not used

[2-3] When CLKC-1 = Up-edge trigger and PFP is installed:

Signal name	Function
DRV[0]	PFP upper drawer tray-up motor drive signal [A]
DRV[1]	PFP upper drawer tray-up motor drive signal [B] DRV[1] DRV[0] Status L L OFF L H Up H L Down H H Break
DRV[2]	PFP lower drawer tray-up motor drive signal [A]
DRV[3]	PFP lower drawer tray-up motor drive signal [B] DRV[3] DRV[2] Status L L OFF L H Up H L Down H H Break
DRV[4]	Not used
DRV[5]	Not used
DRV[6]	Not used
DRV[7]	Not used

[2-4] When CLKC-1 = Up-edge trigger and LCF is installed:

Signal name	Function
DRV[0]	LCF tray-up motor drive signal [A]
DRV[1]	LCF tray-up motor drive signal [B] DRV[1] DRV[0] Status L L OFF L H Up H L Down H H Break
DRV[2]	LCF end fence motor drive signal [A]
DRV[3]	LCF end fence motor drive signal [B] DRV[3] DRV[2] Status L L OFF L H Transfer H L Reverse H H Break
DRV[4]	LCF end fence solenoid drive signal (H: OFF, L: ON)
DRV[5]	Not used
DRV[6]	Not used
DRV[7]	Not used

[3] Description of signals RETS [0]-[7]

The following functions are assigned to the signals RETS [0]-[7] depending on each status of the signals SCSWA-D-0 and installation status of the PFP and LCF.

[3-1] When SCSWA-0 = Low:

Signal name	Function
RETS[0]	Sensor detection signal for option <ul style="list-style-type: none"> • Bridge unit: paper full detection sensor detection signal (H: normal, L: full) • Job separator: JSP stack sensor (lower) detection signal (H: full, L: normal) • Offset tray: OCT stack sensor detection signal (H: full, L: normal)
RETS[1]	Option detection signal (H: offset tray, L: job separator or bridge unit)
RETS[2]	Cover opening/closing sensor detection signal for option <ul style="list-style-type: none"> • Bridge unit: transport cover opening/closing sensor detection signal (H: opened, L: closed) • Job separator: JSP cover switch detection signal (H: opened, L: closed) • Offset tray: OCT cover switch detection signal (H: opened, L: closed)
RETS[3]	Sensor detection signal for option <ul style="list-style-type: none"> • Bridge unit: bridge unit transport sensor-2 (exit side) detection signal (H: paper transport, L: none) • Job separator: JSP feed sensor detection signal (H: paper transport, L: none)
RETS[4]	Sensor detection signal for option <ul style="list-style-type: none"> • Bridge unit: bridge unit transport sensor-1 (entrance side) detection signal (H: paper transport, L: none) • Offset tray: OCT feed sensor detection signal (H: paper transport, L: none)
RETS[5]	Option detection signal (H: bridge unit, L: job separator or offset tray)
RETS[6]	Sensor detection signal for option <ul style="list-style-type: none"> • Job separator: JSP stack sensor (upper) detection signal (H: full, L: normal) • Offset tray: OCT separate sensor detection signal (H: home position)
RETS[7]	Bridge unit / job separator / offset tray connection signal (L: connected)

* The relations between the connection status of options (Bridge Unit, Job Separator and Offset Tray) and RETS signals ([1], [4] and [7]) are as follows.

RETS[1]	RETS[4]	RETS[7]	Options to connect
L	L	L	Job Separator
L	H	L	Bridge Unit
H	H	L	Offset Tray
-	-	H	None

[3-2] When SCSWB-0 = Low and PFP is installed:

Signal name	Function
RETS[0]	PFP upper drawer tray-up sensor detection signal (H: top position, L: normal)
RETS[1]	PFP upper drawer empty sensor detection signal (H: paper presence, L: paper absence)
RETS[2]	PFP side cover opening/closing switch detection signal (H: opened L: closed)
RETS[3]	PFP connection signal (L: connected)
RETS[4]	PFP upper drawer feed sensor detection signal (H: paper transport, L: none)
RETS[5]	PFP upper drawer paper stock sensor detection signal (H: paper absence L: paper presence)
RETS[6]	Not used
RETS[7]	Not used

[3-3] When SCSWB-0 = Low and LCF is installed:

Signal name	Function
RETS[0]	LCF feeding side paper stock sensor detection signal (H: paper presence L: paper absence)
RETS[1]	Not used
RETS[2]	Not used
RETS[3]	Not used
RETS[4]	Not used
RETS[5]	Not used
RETS[6]	LCF feeding side paper mis-stacking sensor detection signal (H: lever to detect mis-stacking is opened)
RETS[7]	LCF tray bottom sensor detection signal (H: bottom position, L: normal)

[3-4] When SCSWC-0 = Low and PFP is installed:

Signal name	Function
RETS[0]	PFP lower drawer tray-up sensor detection signal (H: top position, L: normal)
RETS[1]	PFP lower drawer empty sensor detection signal (H: paper presence, L: paper absence)
RETS[2]	Not used
RETS[3]	PFP motor phase locked loop control signal (H: stop or error, L: uniform speed driving)
RETS[4]	PFP lower drawer feed sensor detection signal (H: paper transport, L: none)
RETS[5]	PFP lower drawer paper stock sensor detection signal (H: paper absence L: paper presence)
RETS[6]	Not used
RETS[7]	Not used

[3-5] When SCSWC-0 = Low and LCF is installed:

Signal name	Function
RETS[0]	LCF feeding side paper empty sensor detection signal (H: paper presence L: paper absence)
RETS[1]	LCF drawer feed sensor detection signal (H: none, L: paper transport)
RETS[2]	LCF tray-up sensor detection signal (H: top position, L: normal)
RETS[3]	LCF transport motor LD signal (H: stop, L: rotation)
RETS[4]	LCF side cover opening/closing switch detection signal (H: closed L: opened)
RETS[5]	LCF standby side paper empty sensor detection signal (H: paper absence L: paper presence)
RETS[6]	LCF end fence stop position sensor detection signal (H: stop position)
RETS[7]	LCF end fence home position sensor detection signal (H: home position)

[3-6] When SCSWD-0 = Low:

Signal name	Function
RETS[0]	Upper drawer tray-up sensor detection signal (H: top position, L: normal)
RETS[1]	Upper drawer empty sensor detection signal (H: paper presence, L: paper absence)
RETS[2]	Upper drawer paper stock sensor detection signal (H: paper absence, L: paper presence)
RETS[3]	Upper drawer detection switch detection signal (H: drawer opened, L: drawer closed)
RETS[4]	Lower drawer tray-up sensor detection signal (H: top position, L: normal)
RETS[5]	Lower drawer empty sensor detection signal (H: paper presence, L: paper absence)
RETS[6]	Lower drawer paper stock sensor detection signal (H: paper absence, L: paper presence)
RETS[7]	Lower drawer detection switch detection signal (H: drawer opened, L: drawer closed)

3. ELECTRIC CIRCUIT DIAGRAMS

3.1	System control circuit (SYS board)	1/18 to 18/18
3.2	Logic circuit (LGC board)	1/19 to 19/19
3.3	Scanning section control circuit (SLG board)	1/13 to 13/13
3.4	CCD drive circuit (CCD board)	1/2 to 2/2
3.5	Laser control signal relay circuit (LRL board)	1/1
3.6	Laser drive circuit (LDR board)	1/2 to 2/2
3.7	Laser beam detection circuit (SNS board)	1/1
3.8	ADU drive circuit (ADU board)	1/2 to 2/2
3.9	Display circuit (DSP board)	1/1
3.10	Key control circuit (KEY board)	1/1
3.11	Fuse circuit (FUS board)	1/1
3.12	Facsimile circuit (FAX board: GD-1150)	1/14 to 14/14
3.13	Modem circuit (MDM board: GD-1160)	1/4 to 4/4
3.14	Telephone line network control circuit (NCU board: GD-1150/1160) *Only for NA/TW model	1/2 to 2/2
3.15	Telephone line network control circuit (NCU board: GD-1150/1160) *Only for EU/AU/AS/C models	1/2 to 2/2

3.1 System control circuit (SYS board)

SYS board 1/18

Sheet No.	Note
001	INDEX
002	BLANK PAGE
003	CPU -NORTH BRIDGE
004	CPU -NORTH BRIDGE (POWER)
005	CONFIGURATION (NORTH BRIDGE / CPU)
006	RESET / POWER
007	DDR TERMINATION / DDR CLOCK
008	DDR DIMM
009	BOOT ROM ,DownLoad JIG I/F
010	SRAM , DEBUG LED,DEBUG SIO , MPP , FAN
011	ETHERNET
012	PCI(1)-ASIC
013	PCI(1)-PCI1 OPTION SLOT0/1
014	PCI(1)-WIFI SLOT (Mini PCI) , ASIC , FAX I/F
015	PCI(1)-ASIC
016	ASIC , PAGE MEMORY , PANEL I/F
017	, NVRAM , Coin Controller
018	I/F : SLG / LGC

Fig. 3-1

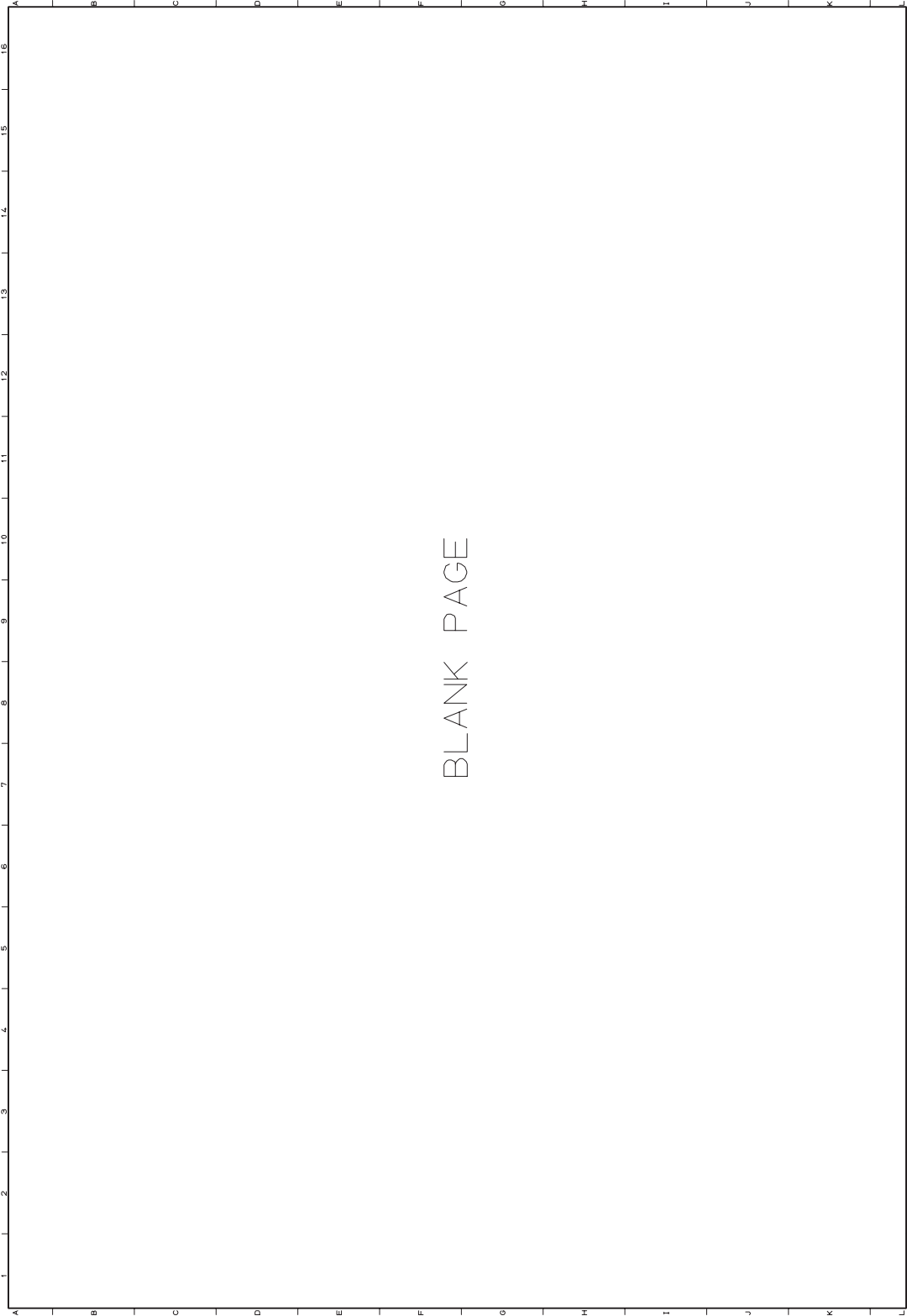


Fig. 3-2

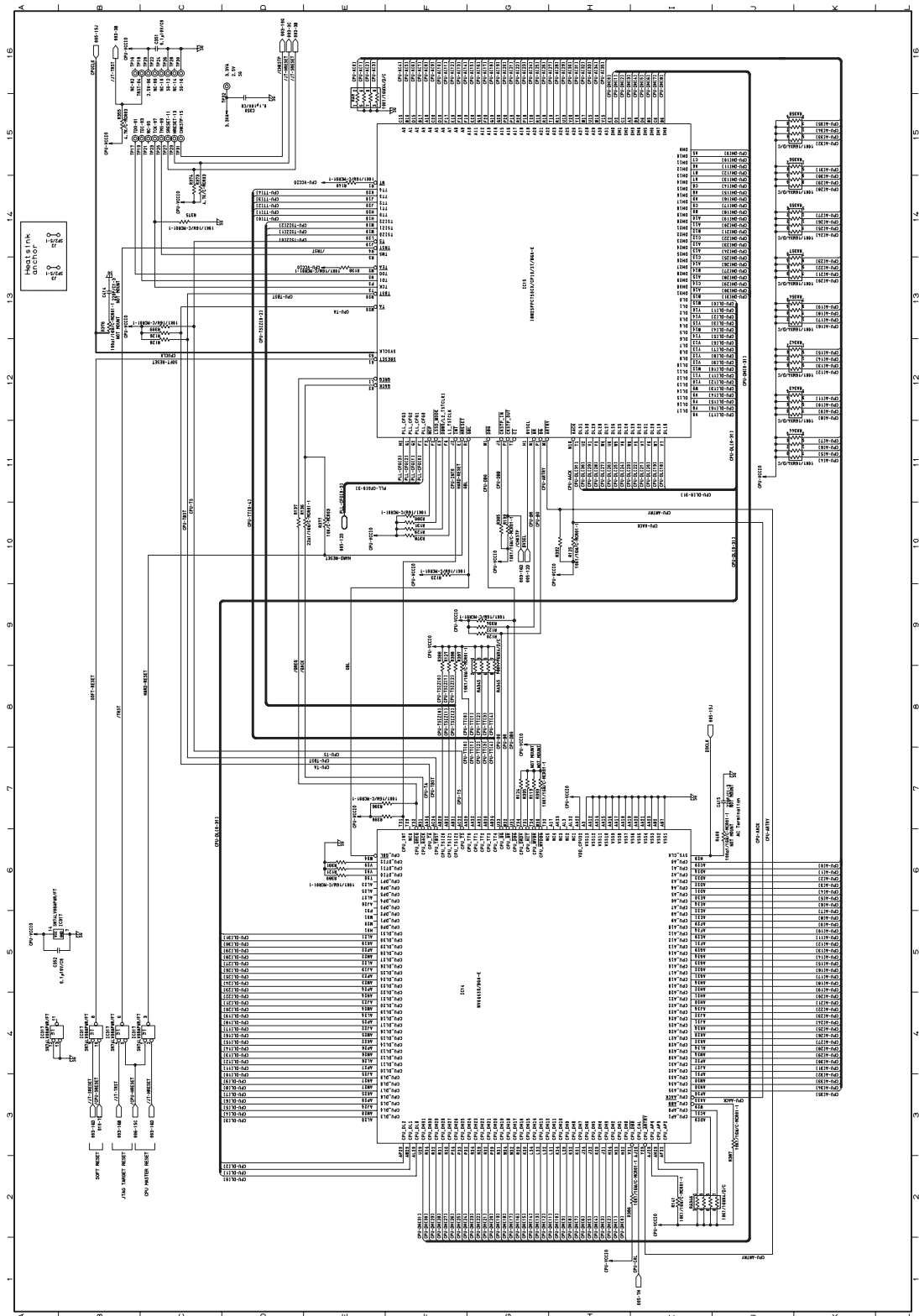


Fig. 3-3

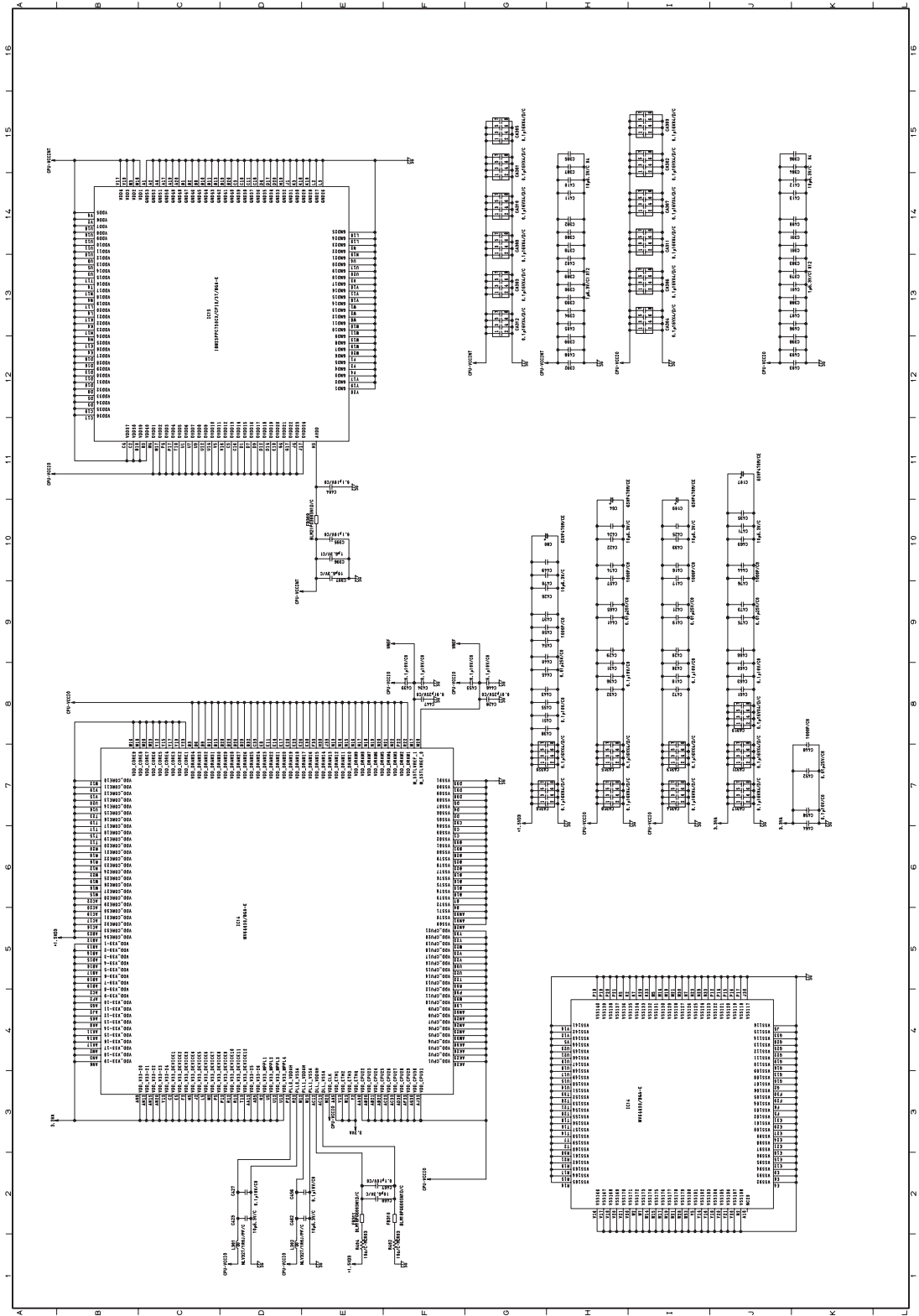
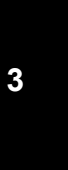


Fig. 3-4



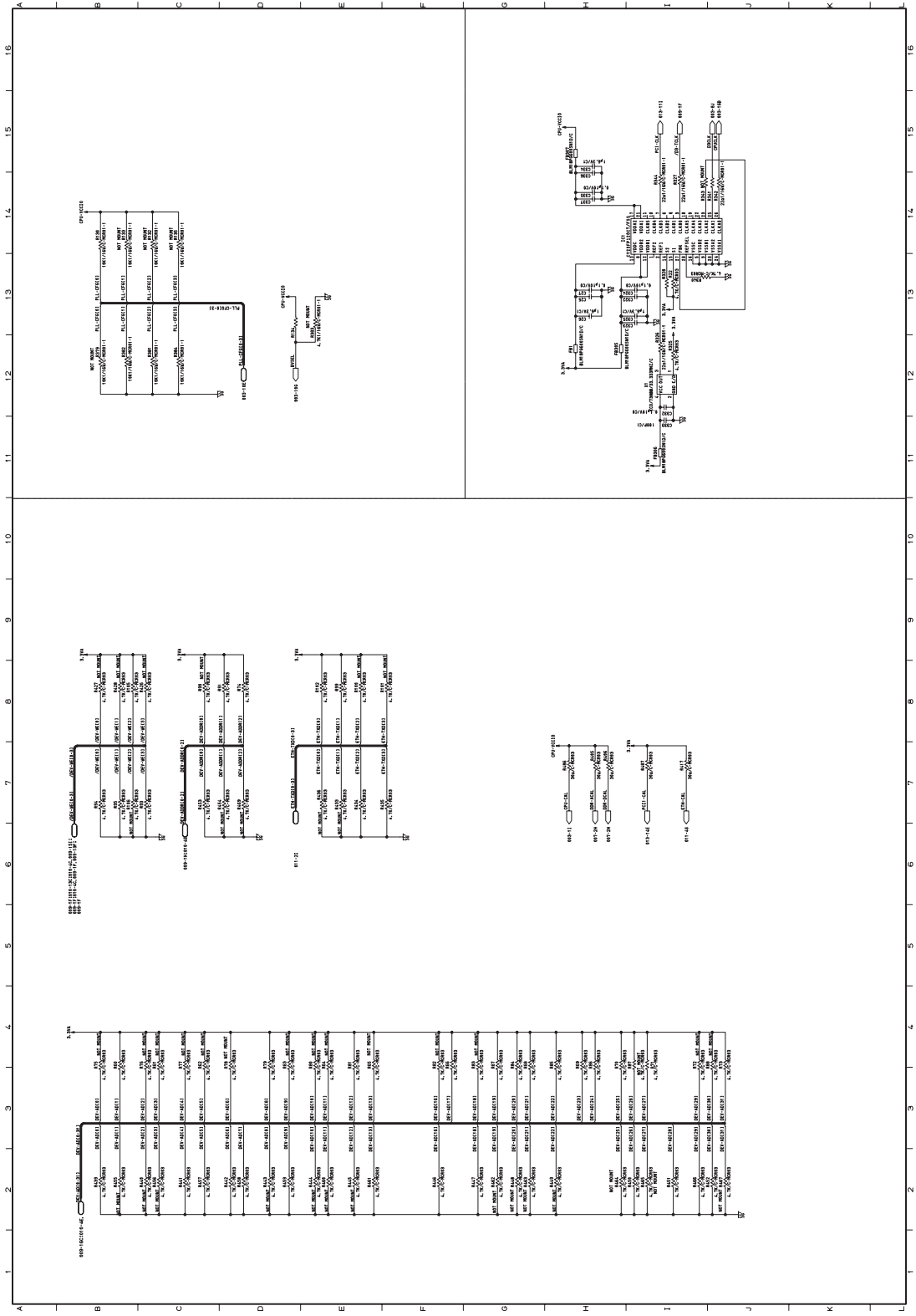


Fig. 3-5

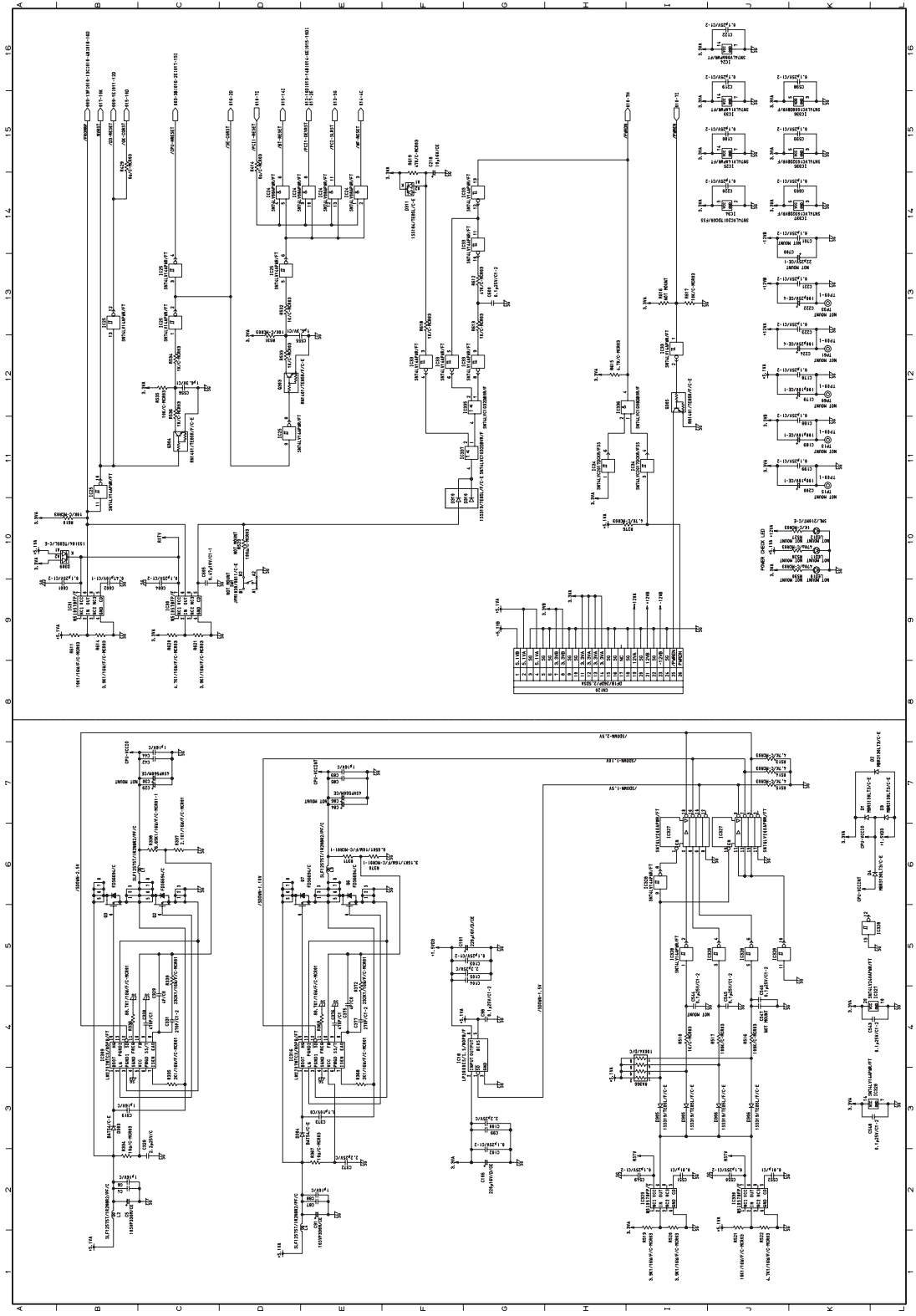


Fig. 3-6



SYS board 7/18

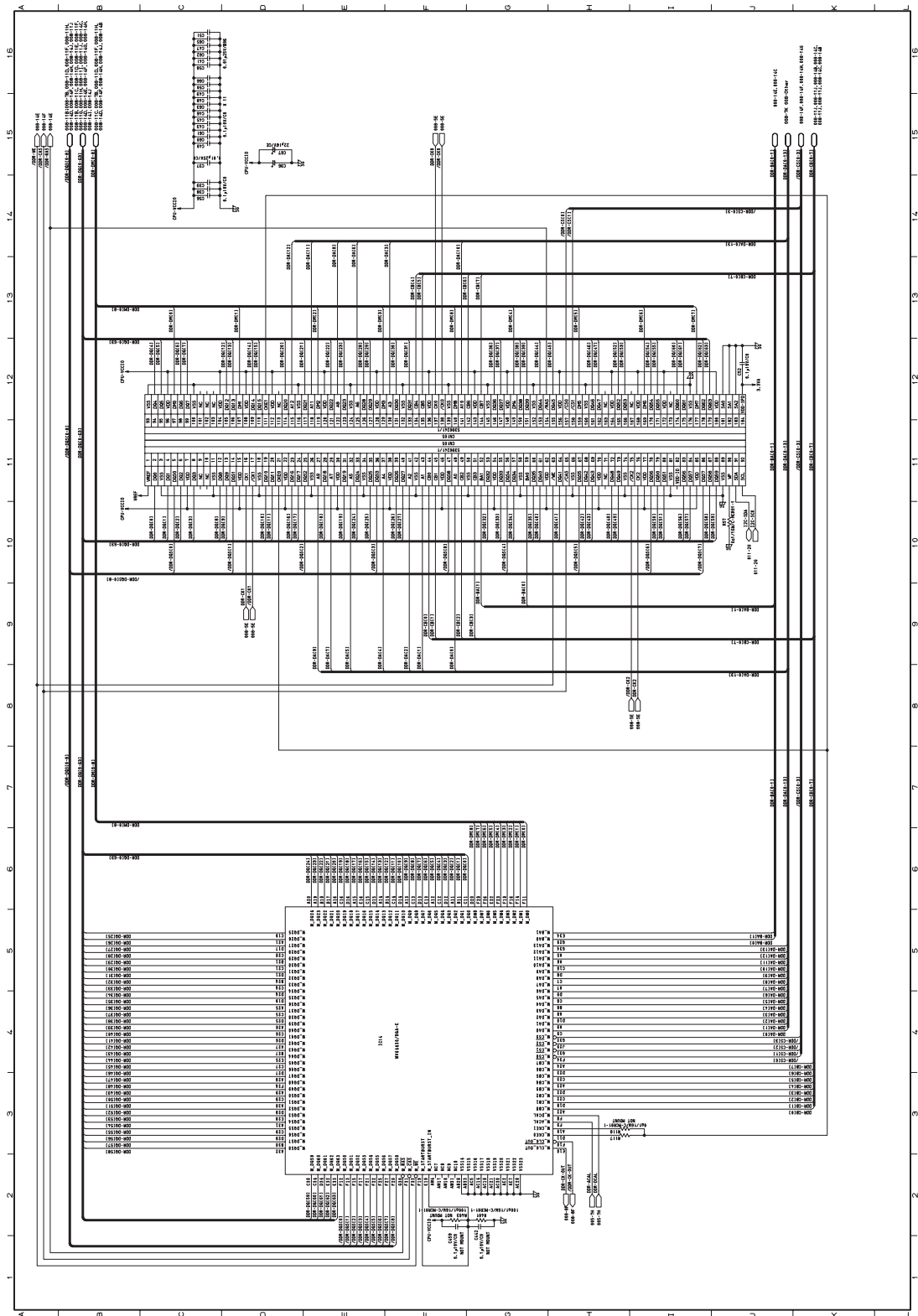


Fig. 3-7

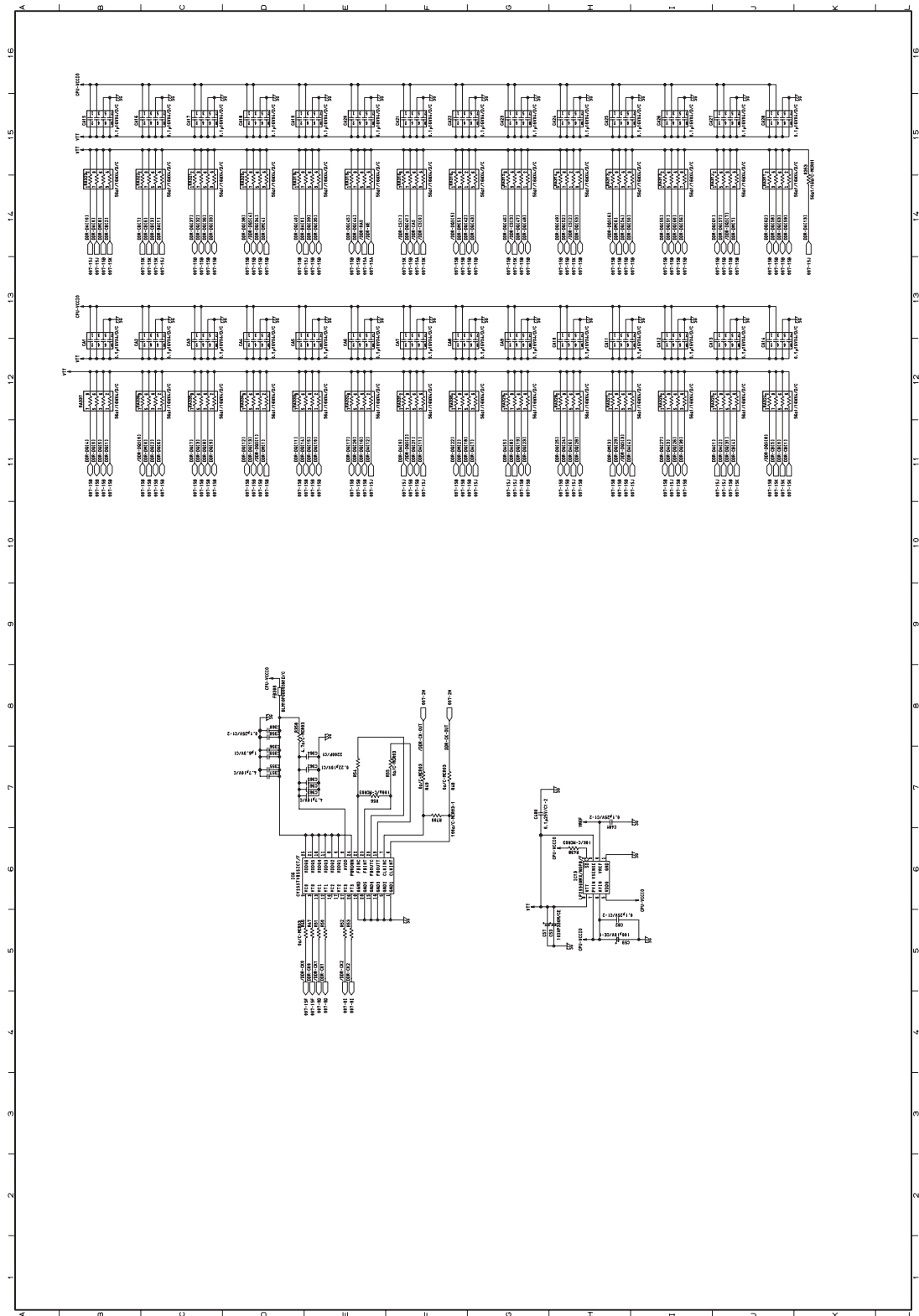


Fig. 3-8



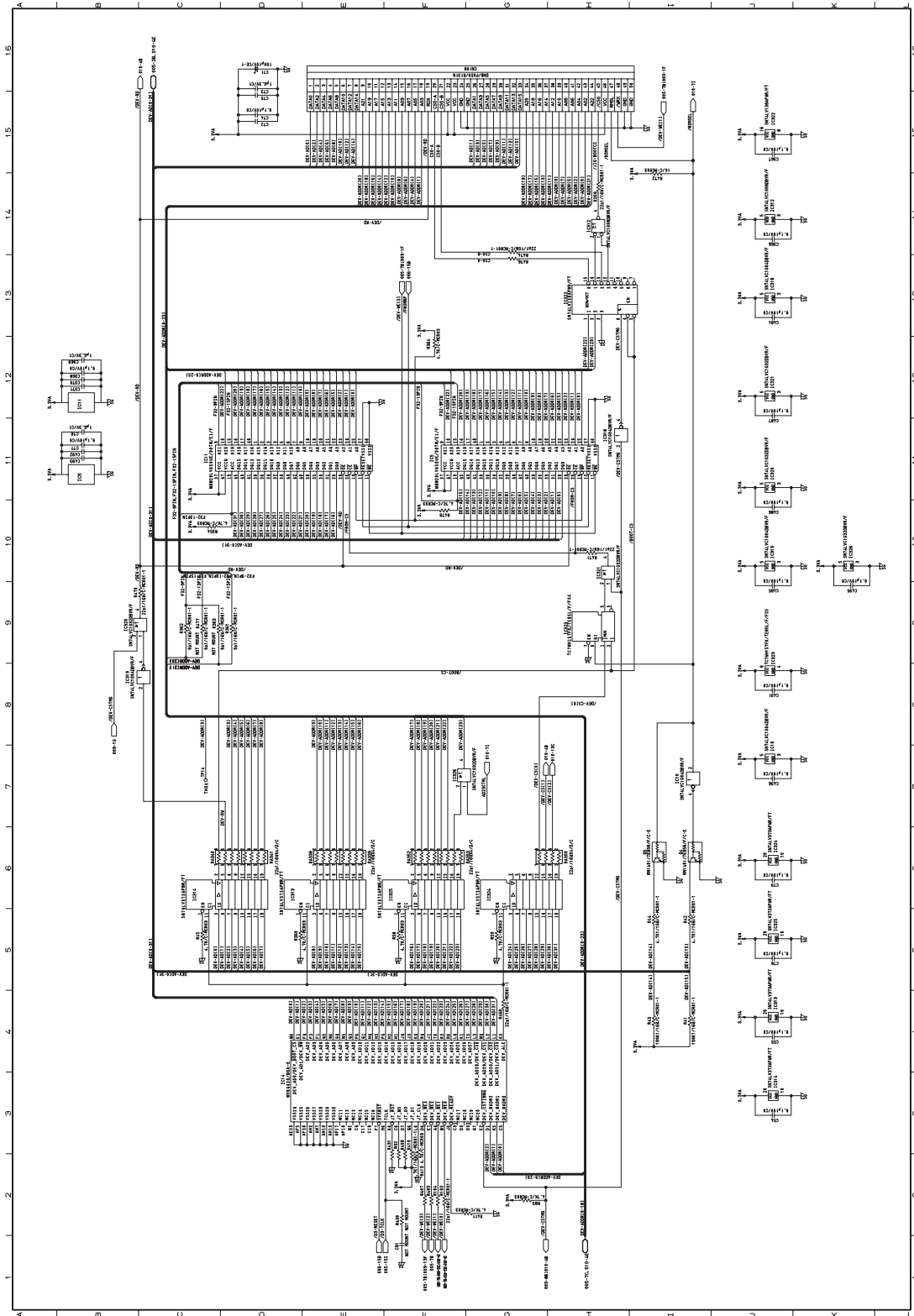


Fig. 3-9

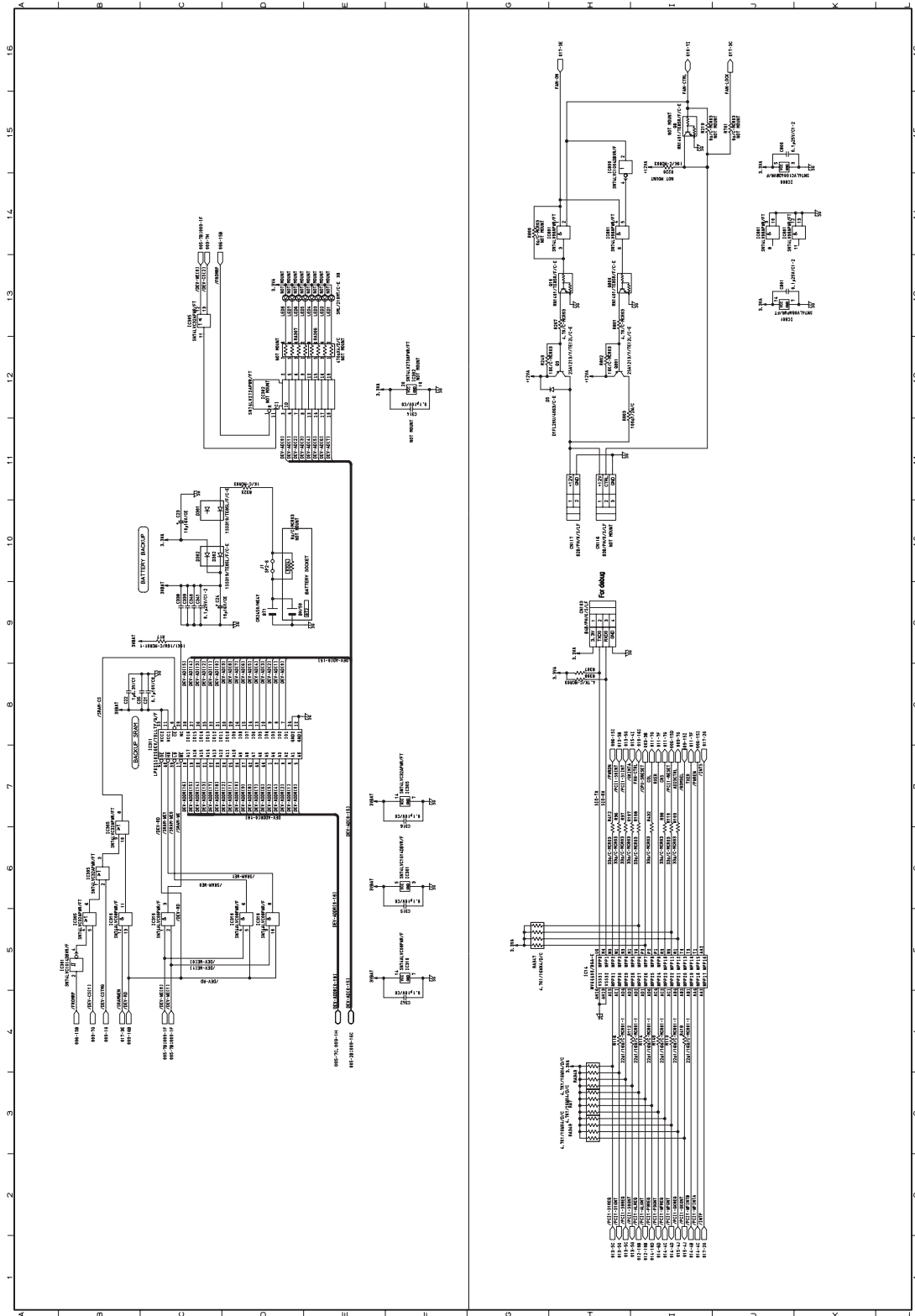


Fig. 3-10



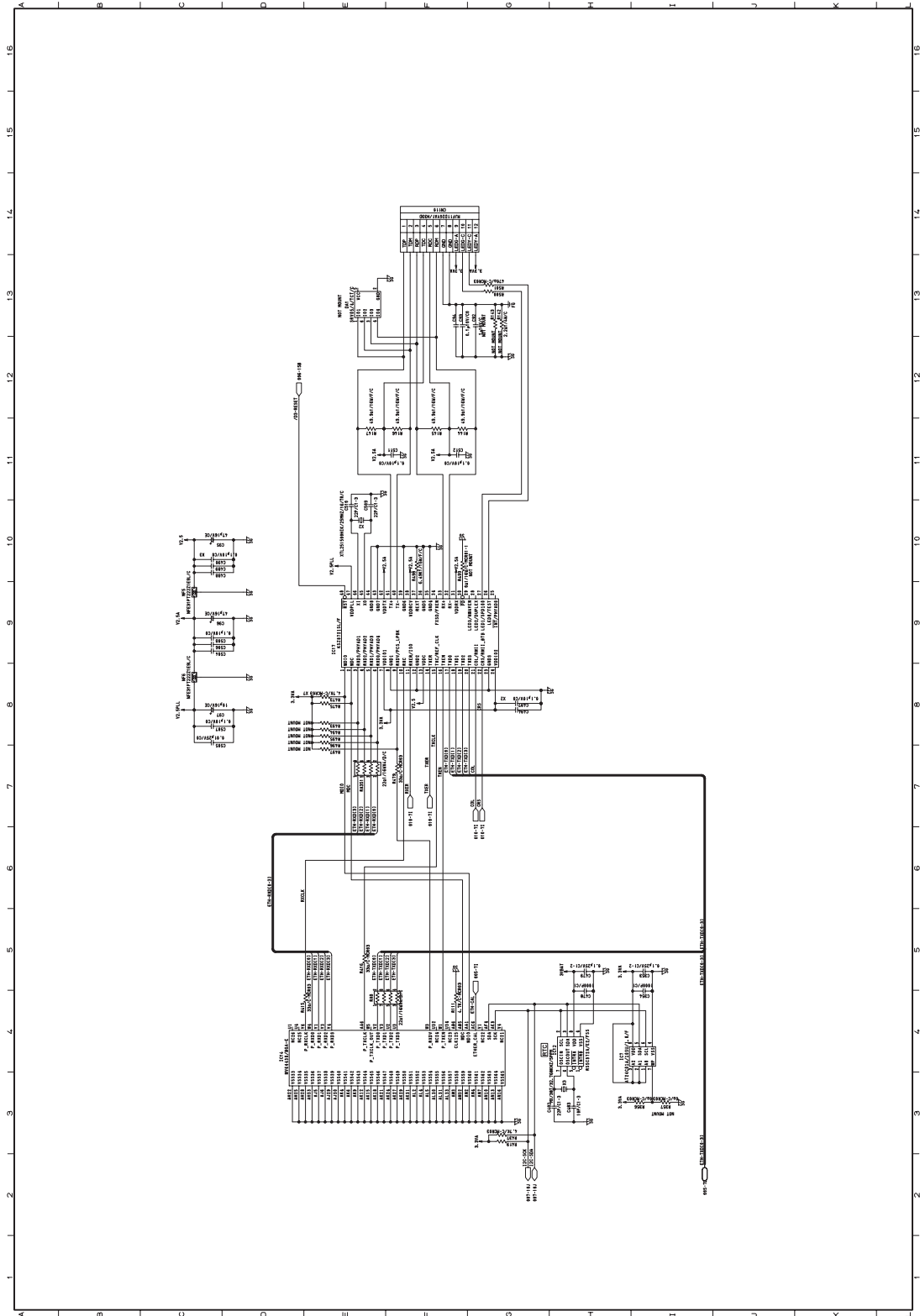


Fig. 3-11

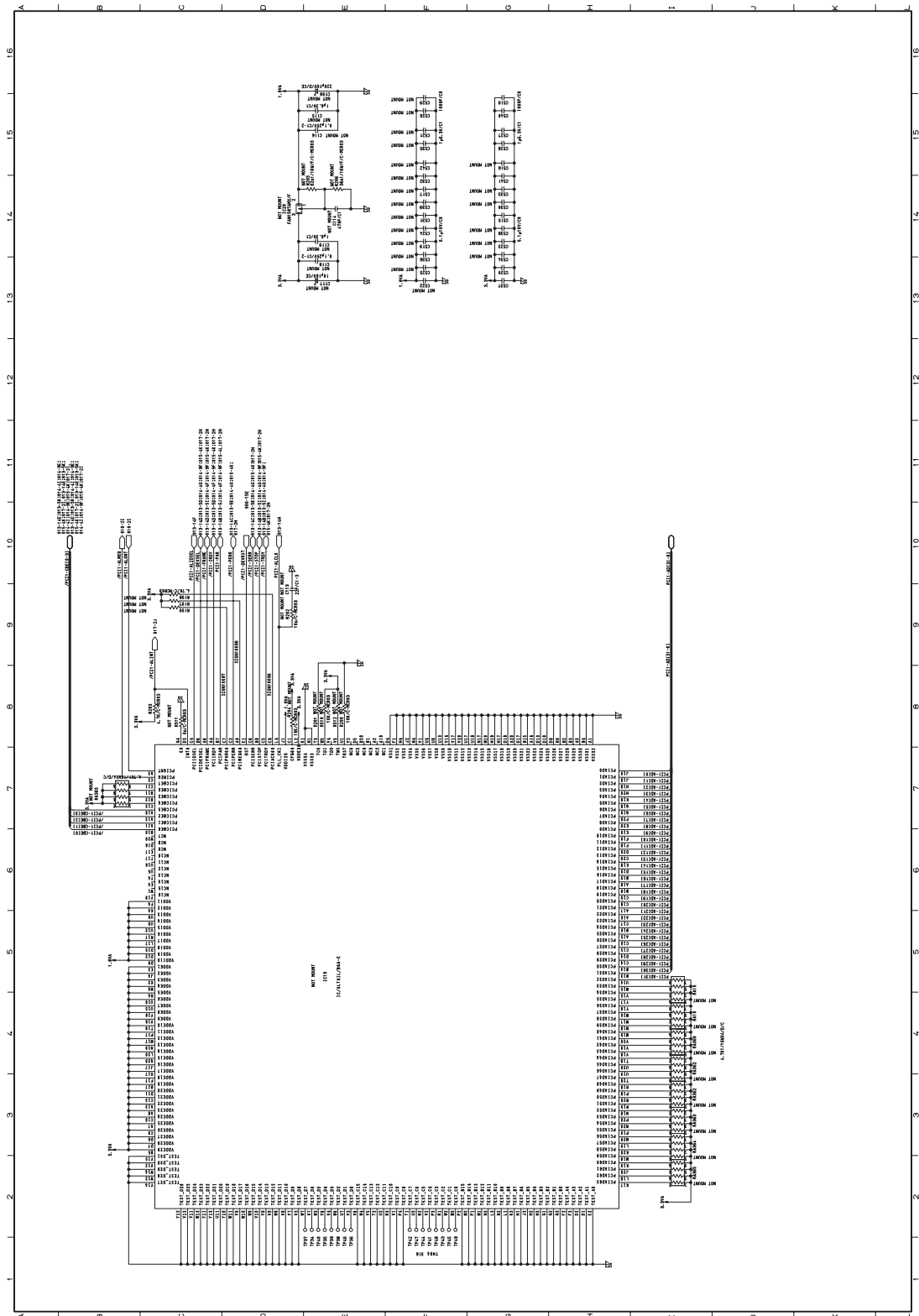


Fig. 3-12



SYS board 13/18

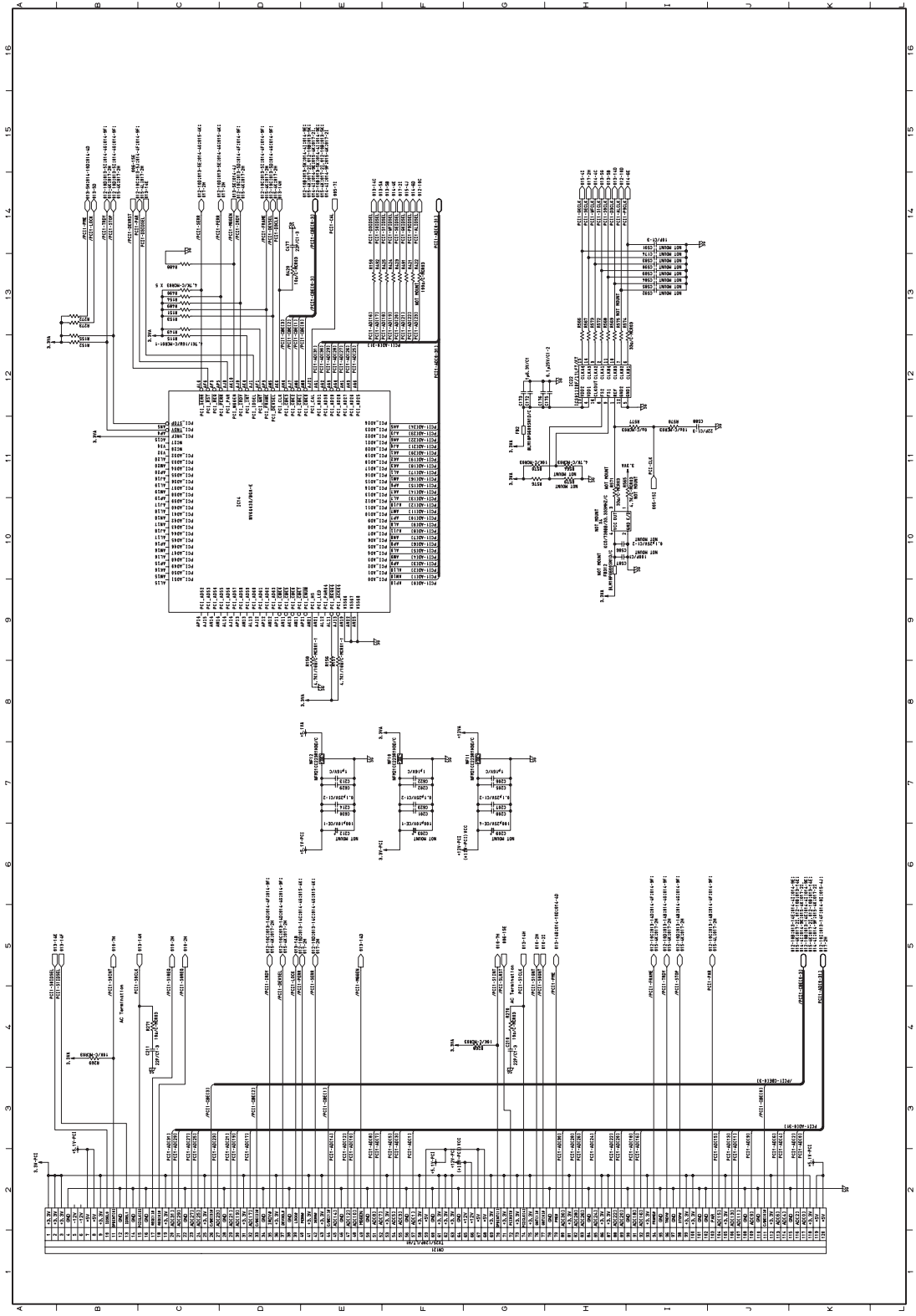


Fig. 3-13

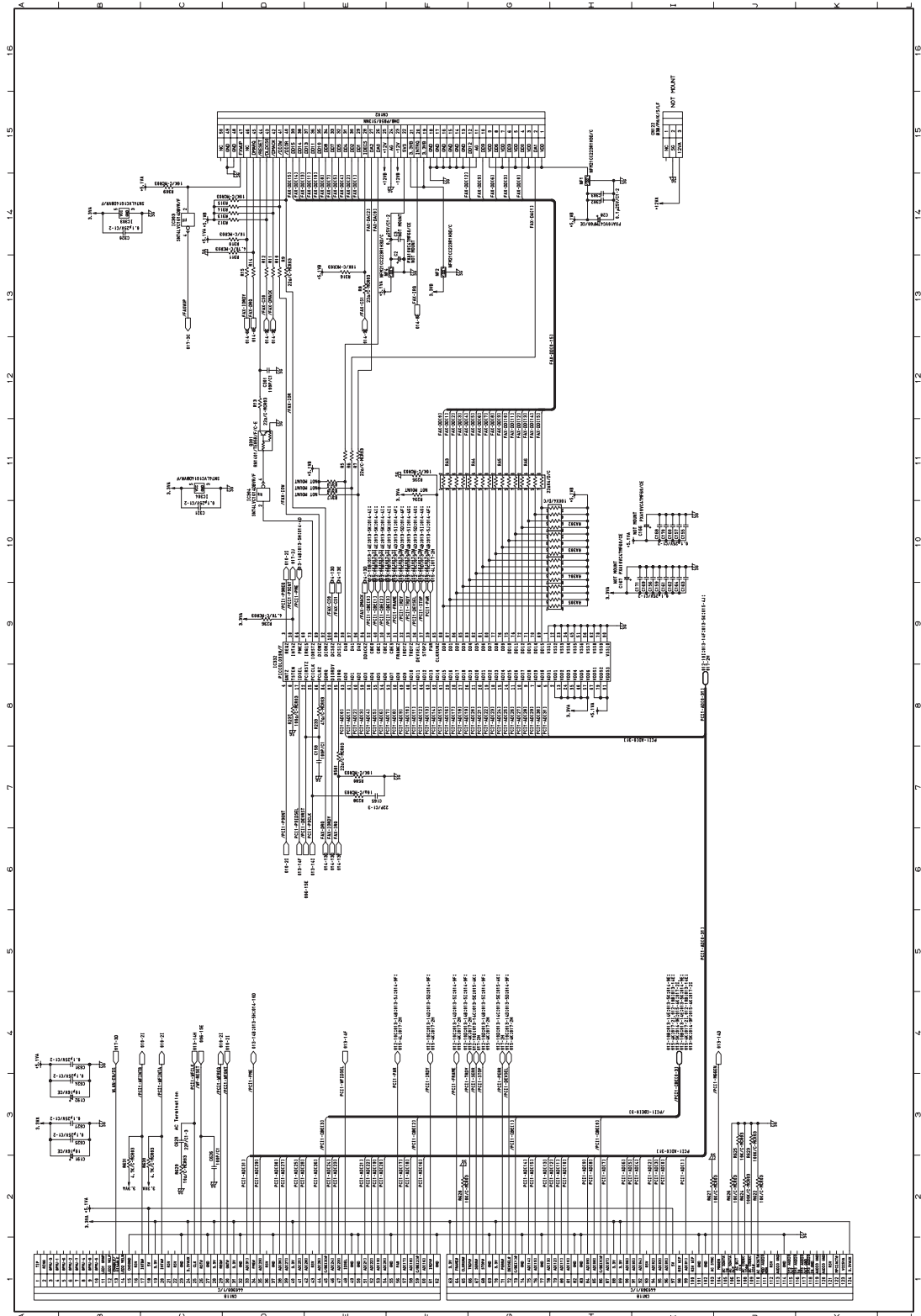


Fig. 3-14



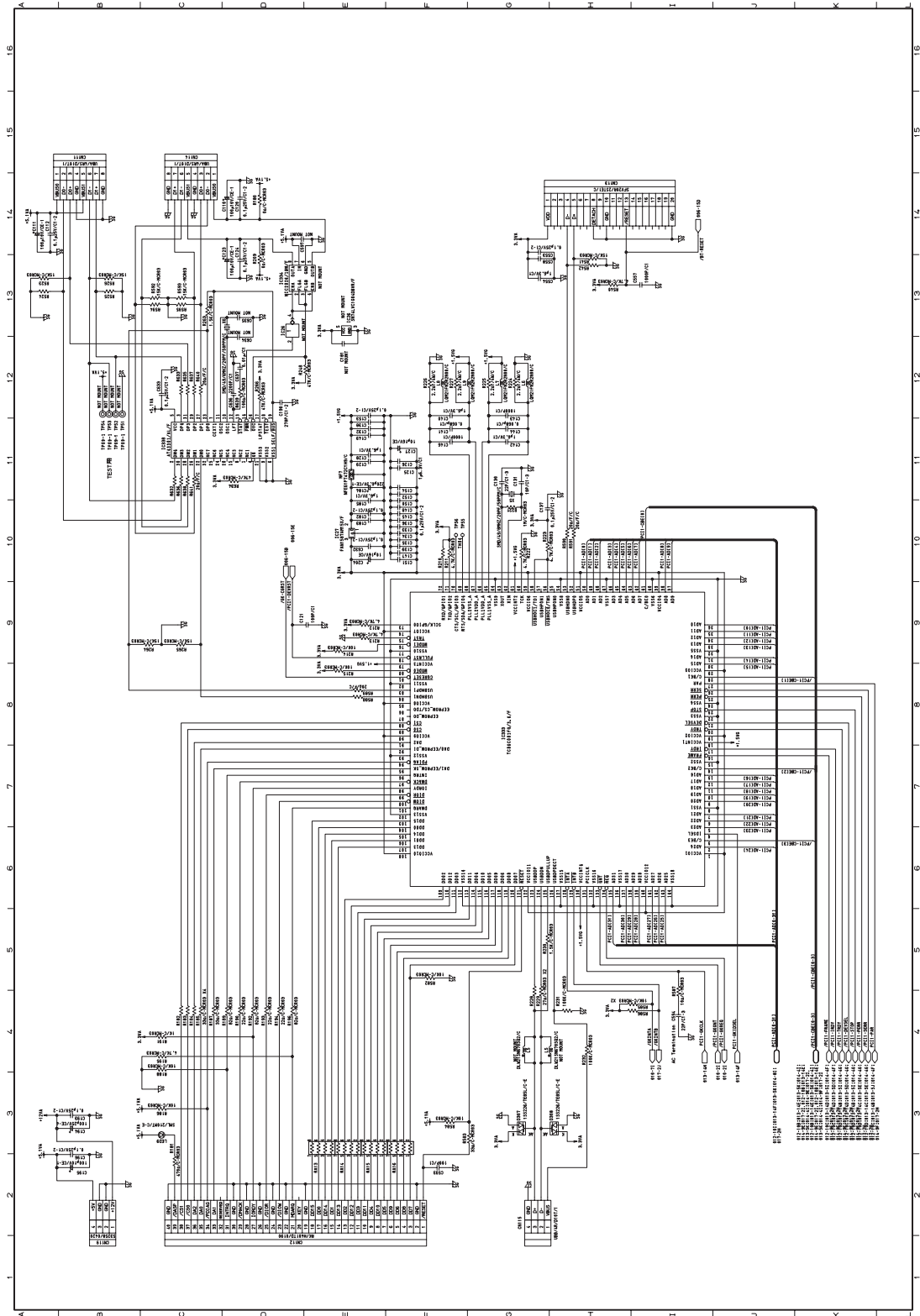


Fig. 3-15

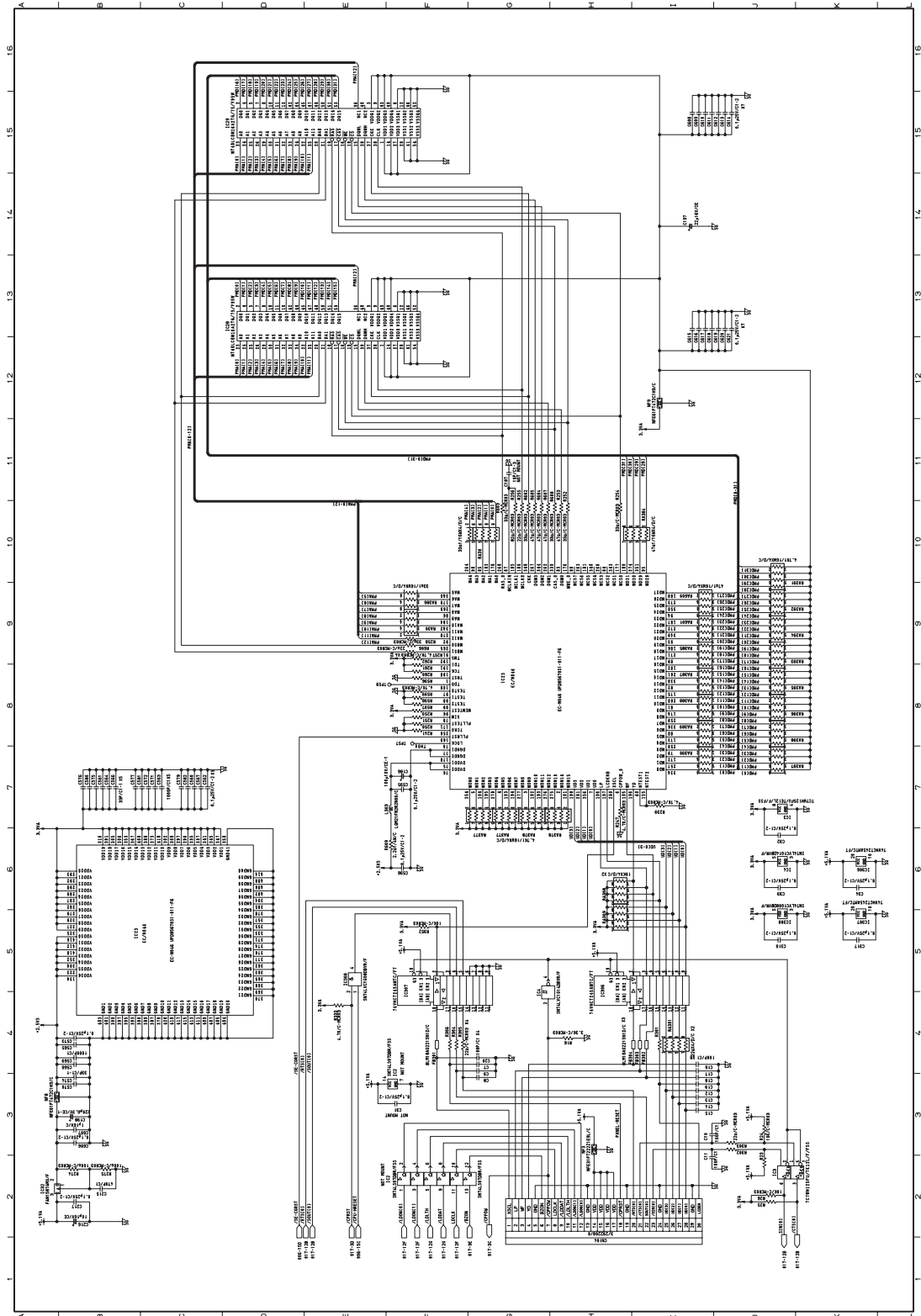


Fig. 3-16

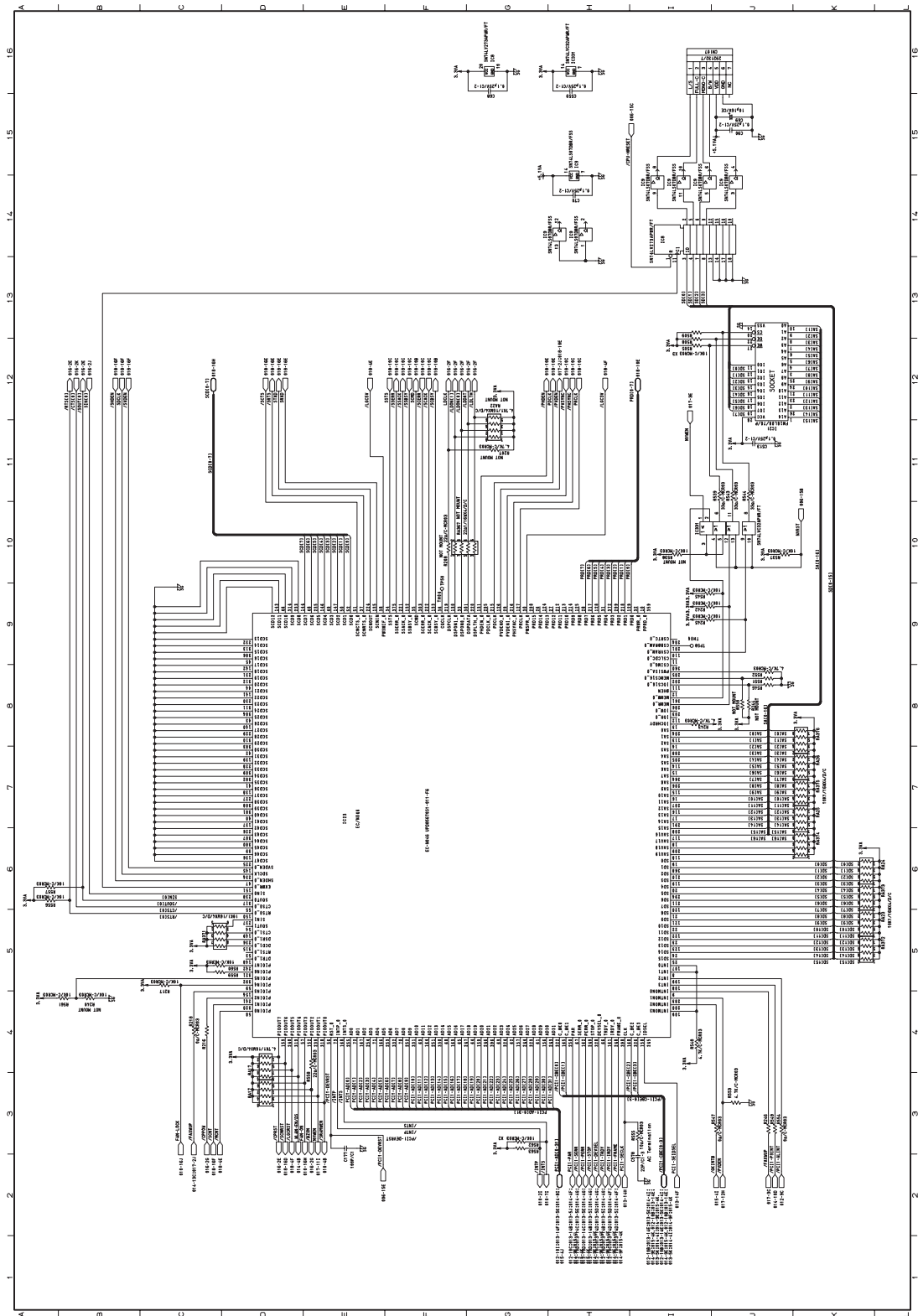


Fig. 3-17

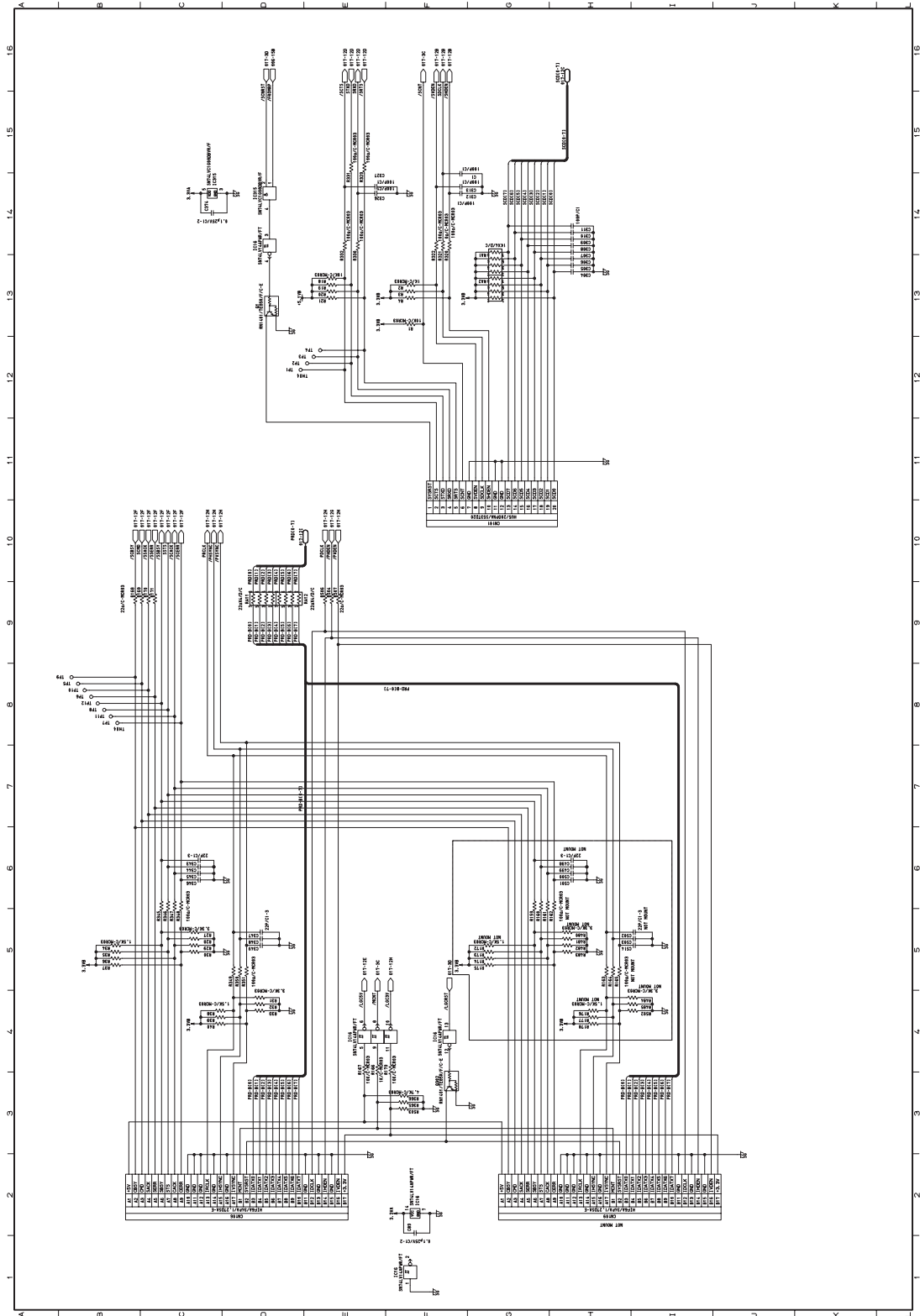


Fig. 3-18

3.2 Logic circuit (LGC board)

LGC board 1/19

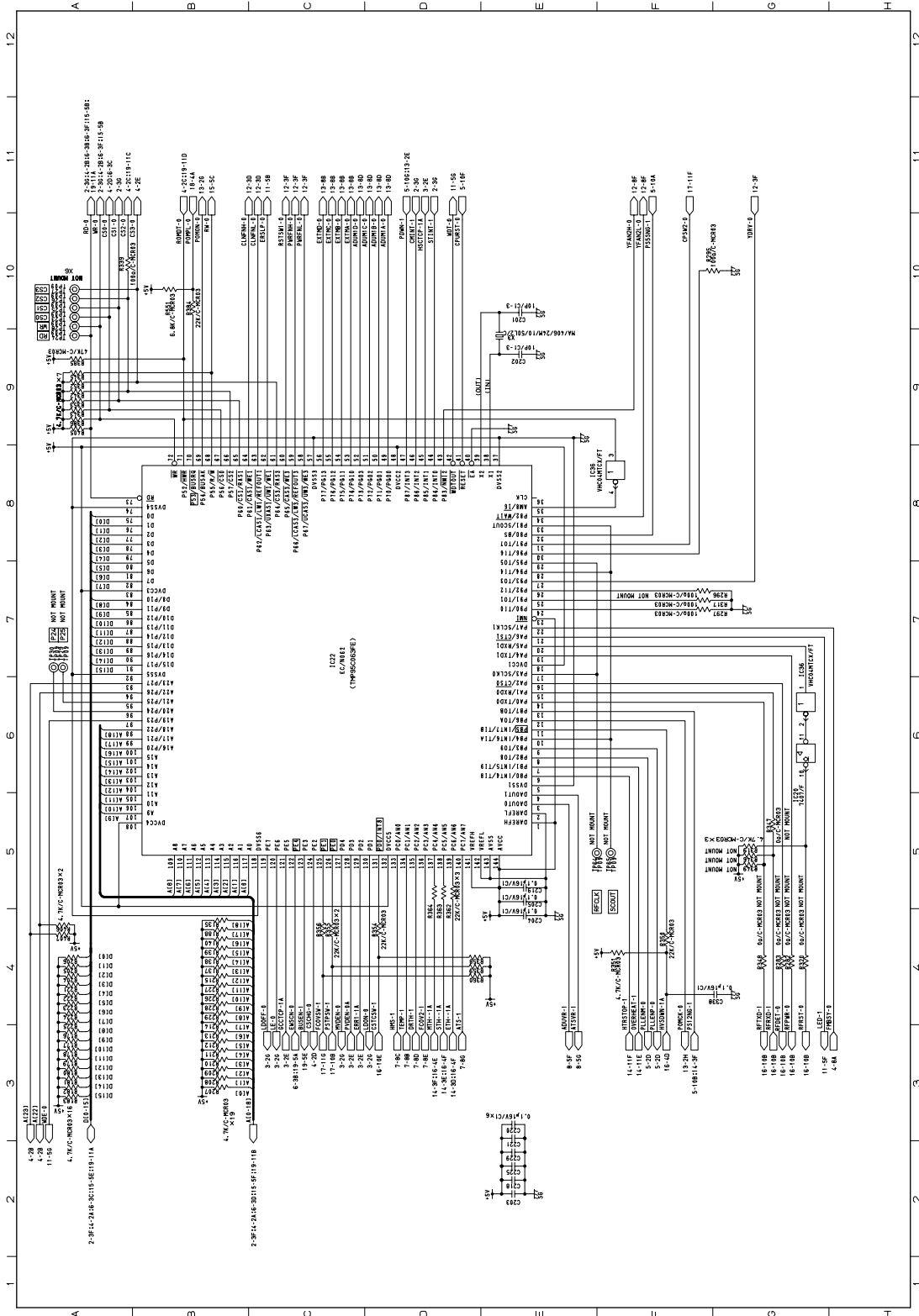


Fig. 3-19

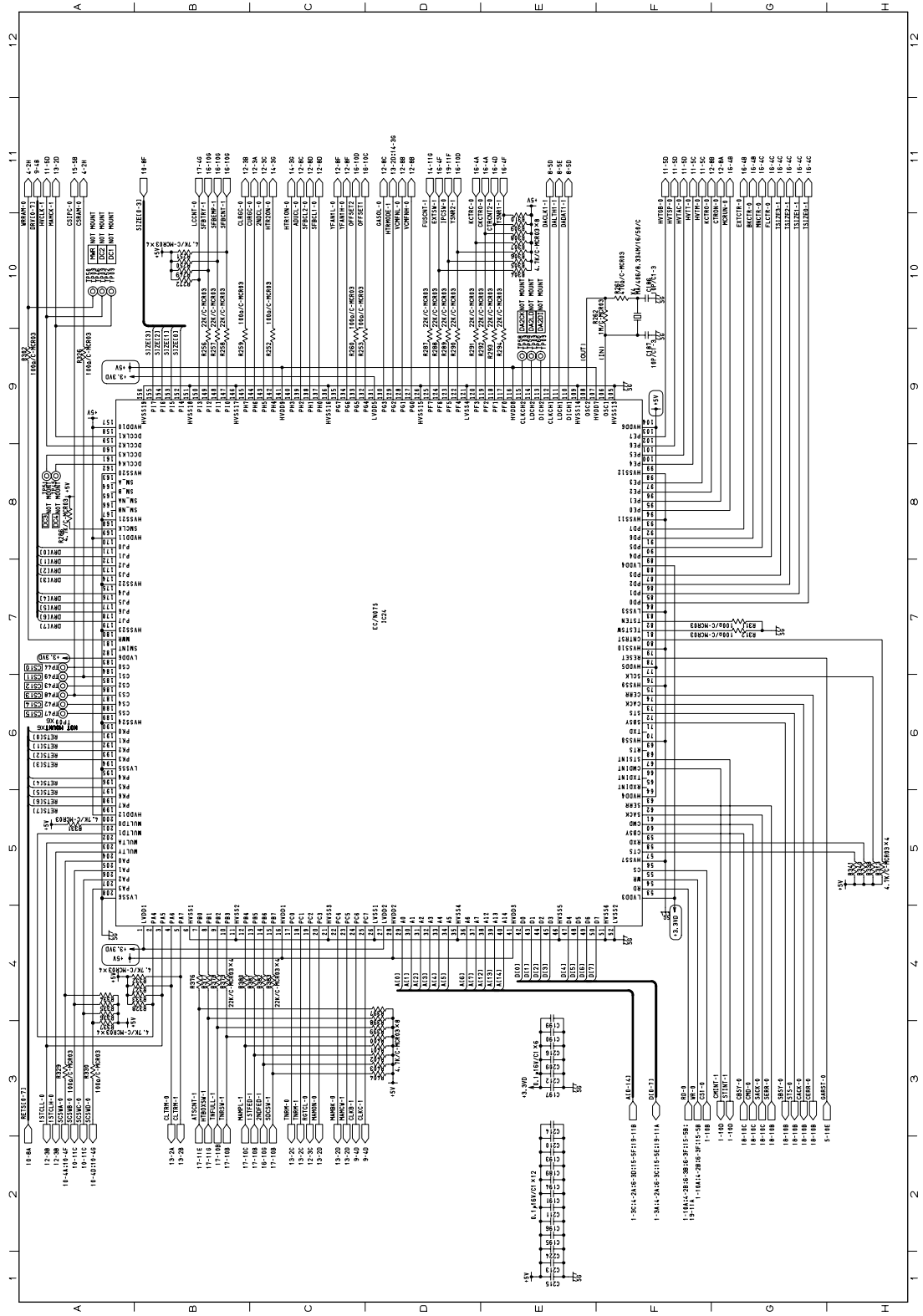


Fig. 3-20

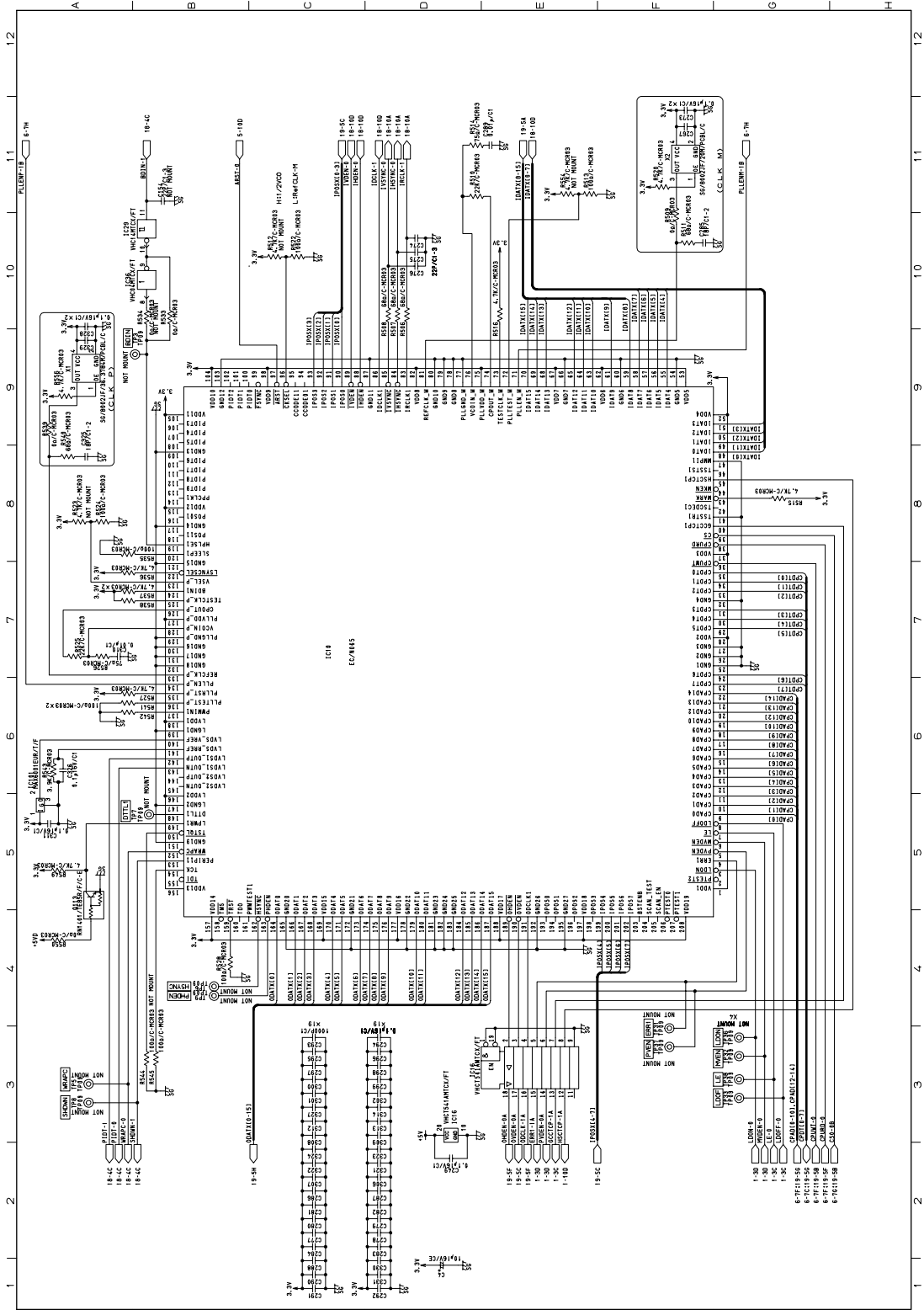


Fig. 3-21

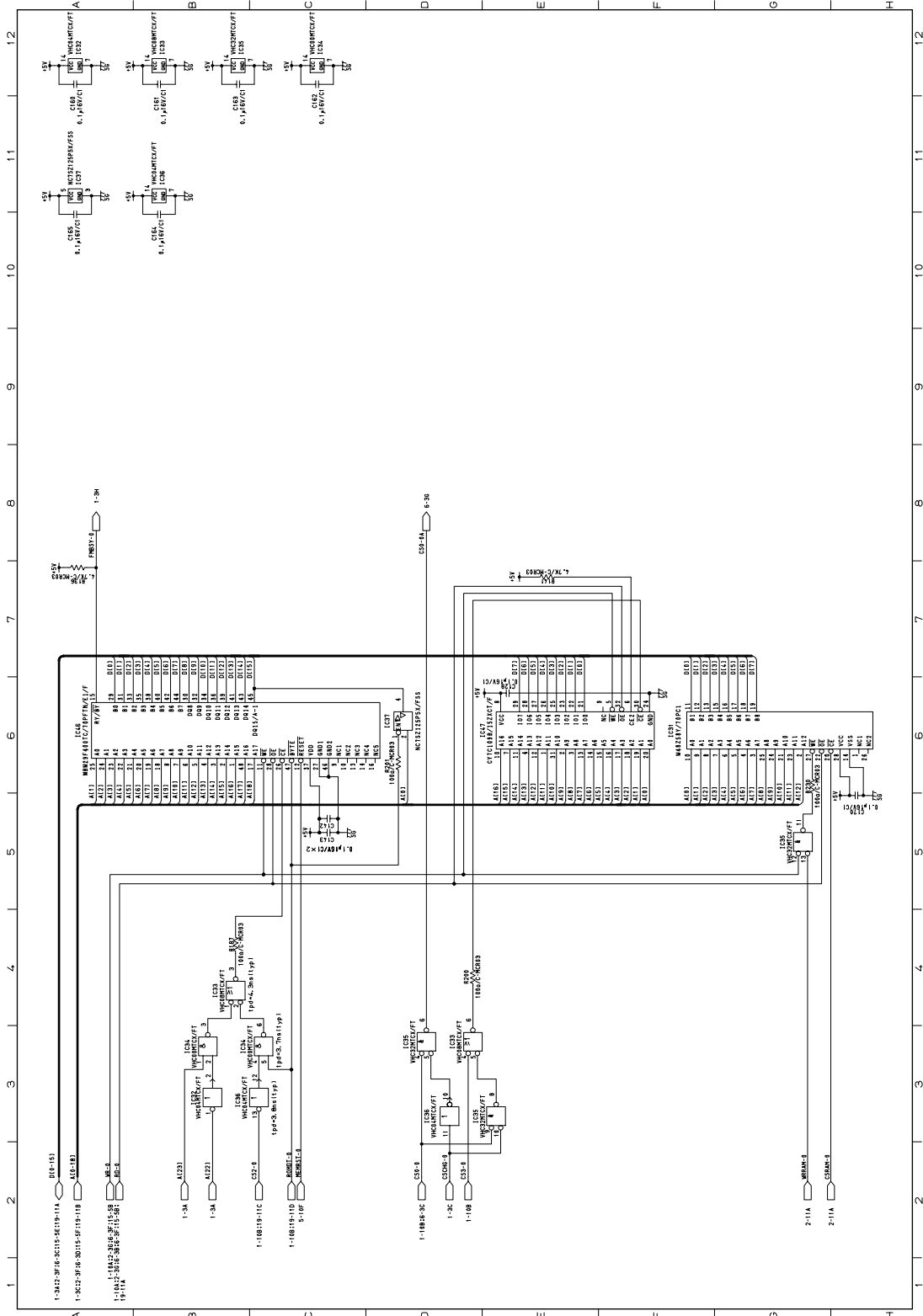


Fig. 3-22



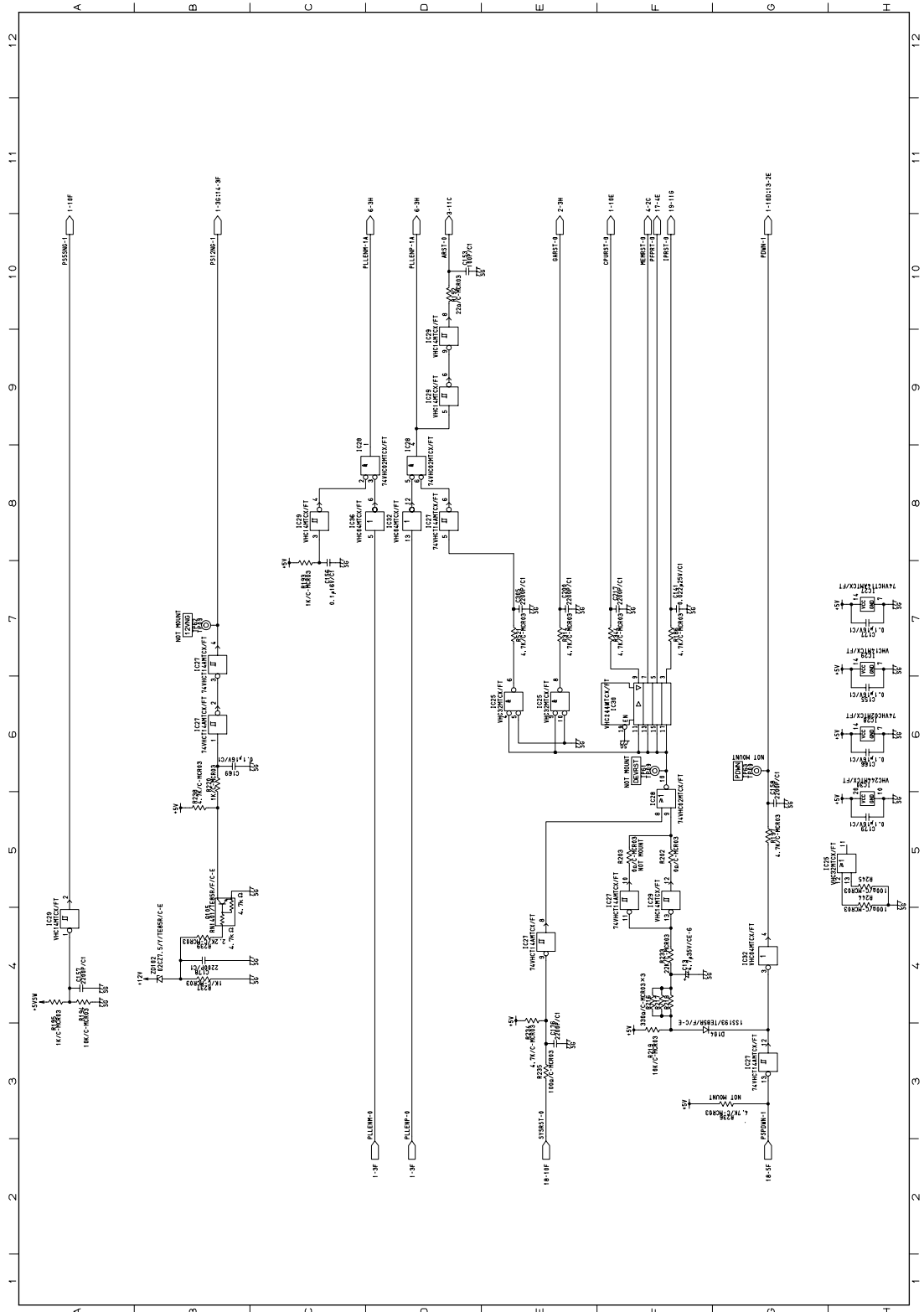


Fig. 3-23

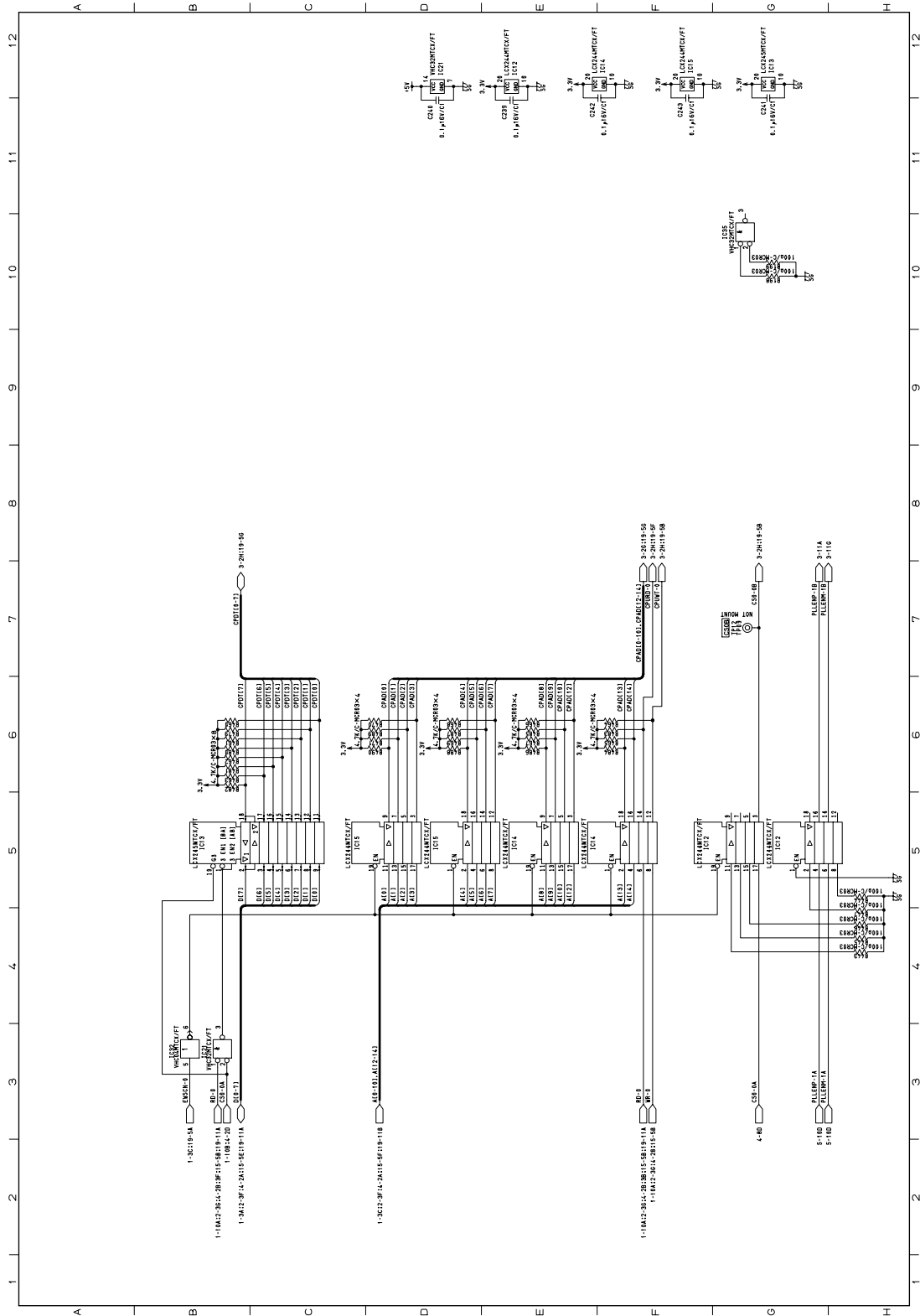


Fig. 3-24



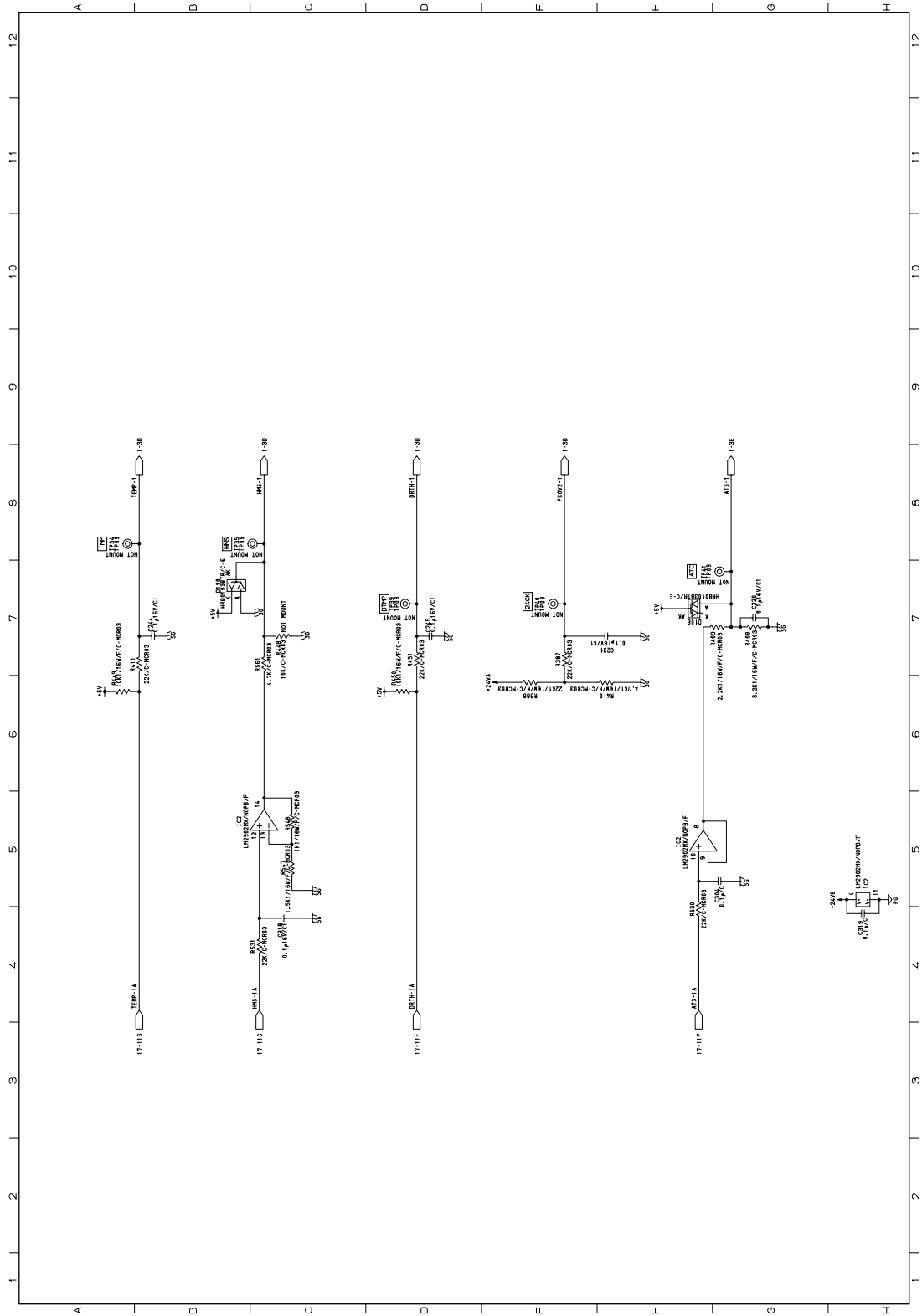


Fig. 3-25

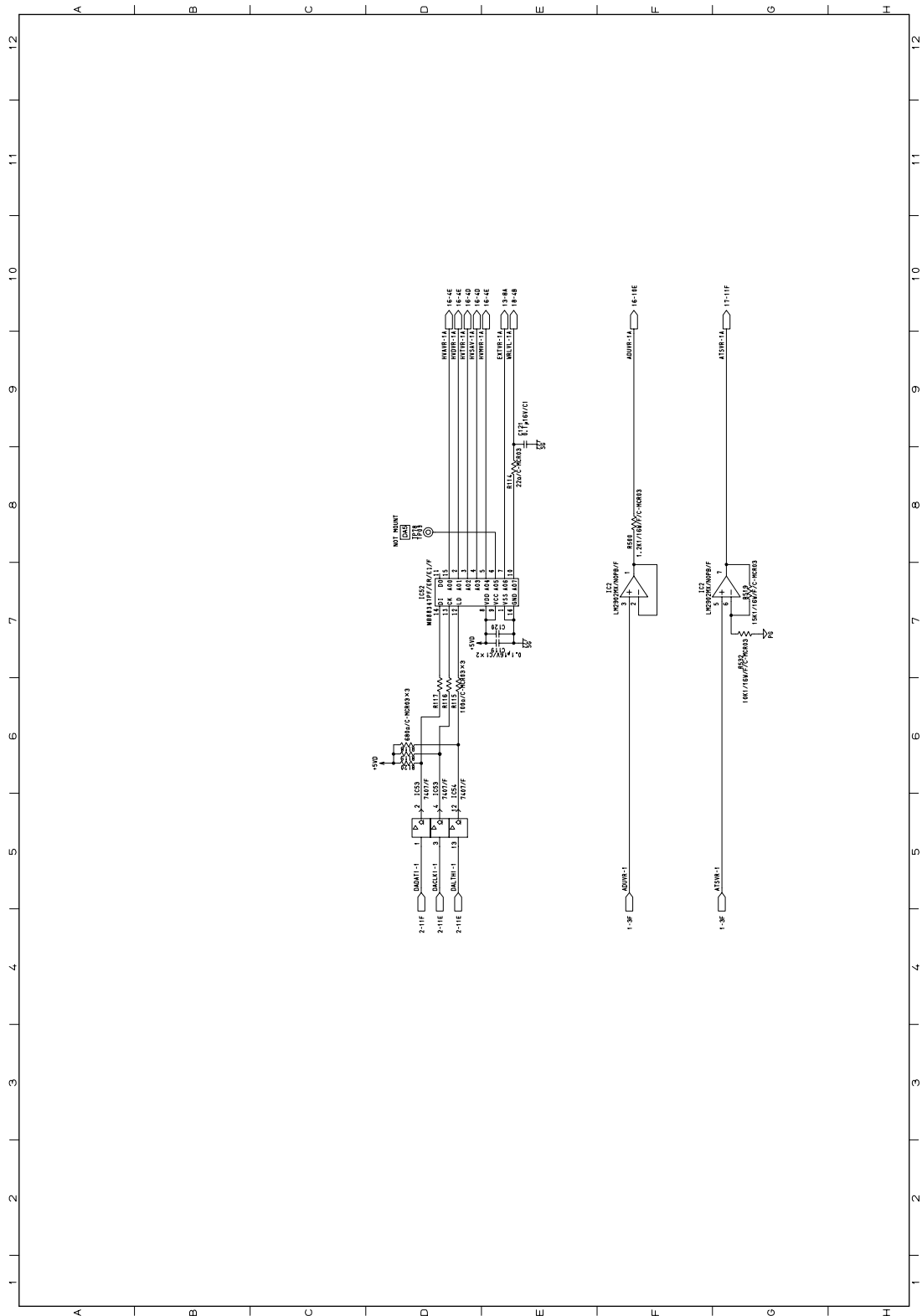


Fig. 3-26

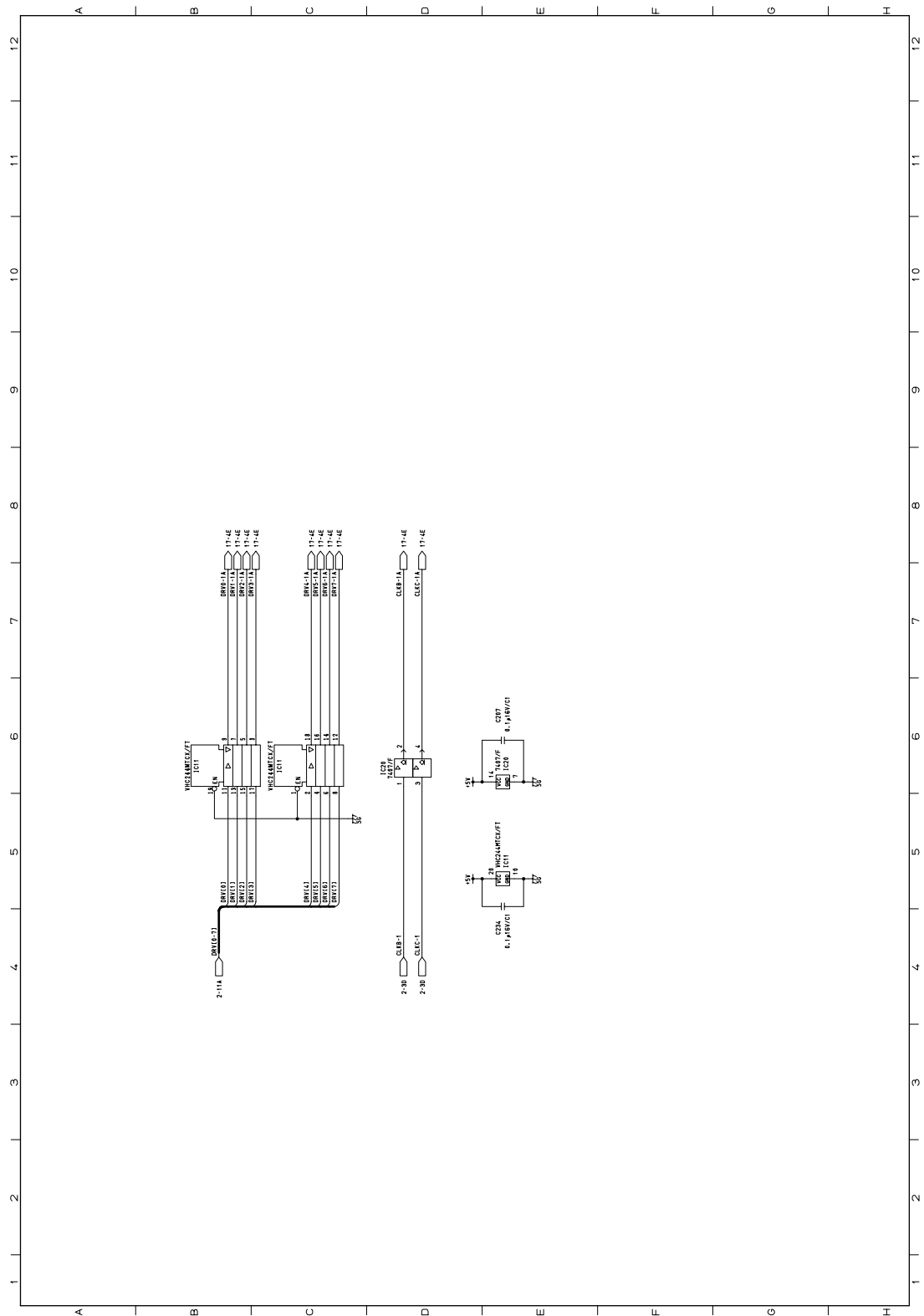


Fig. 3-27

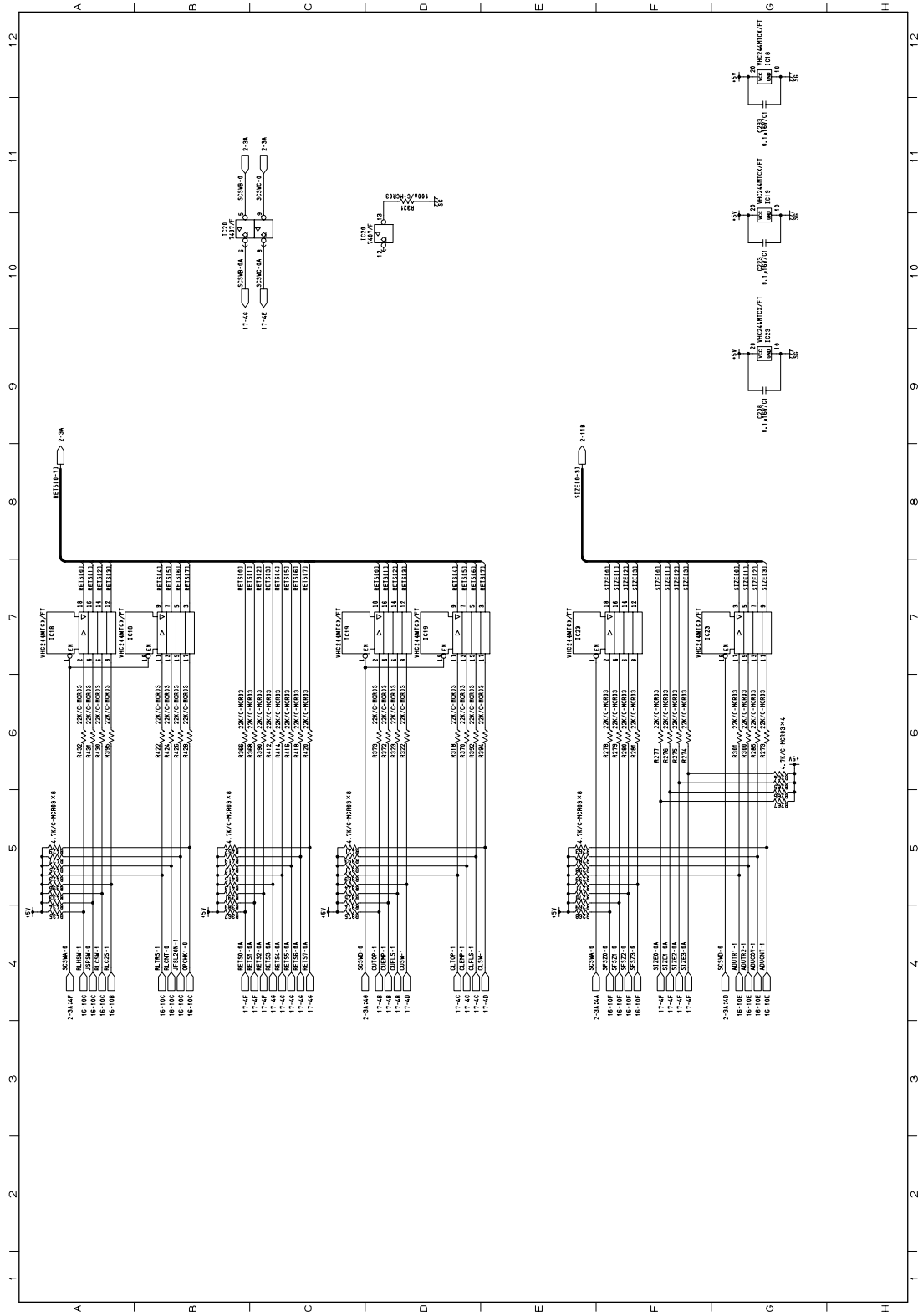


Fig. 3-28



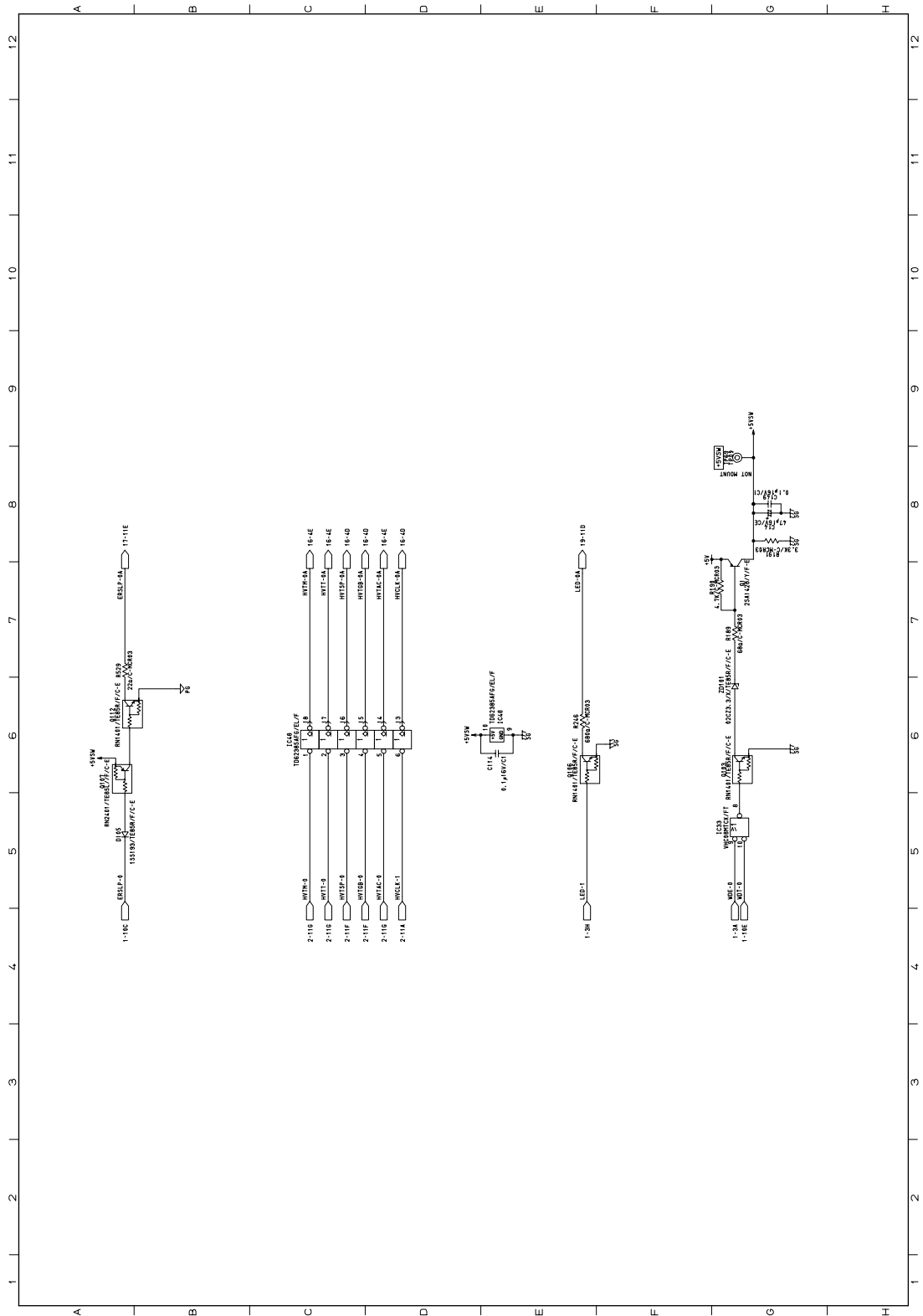


Fig. 3-29

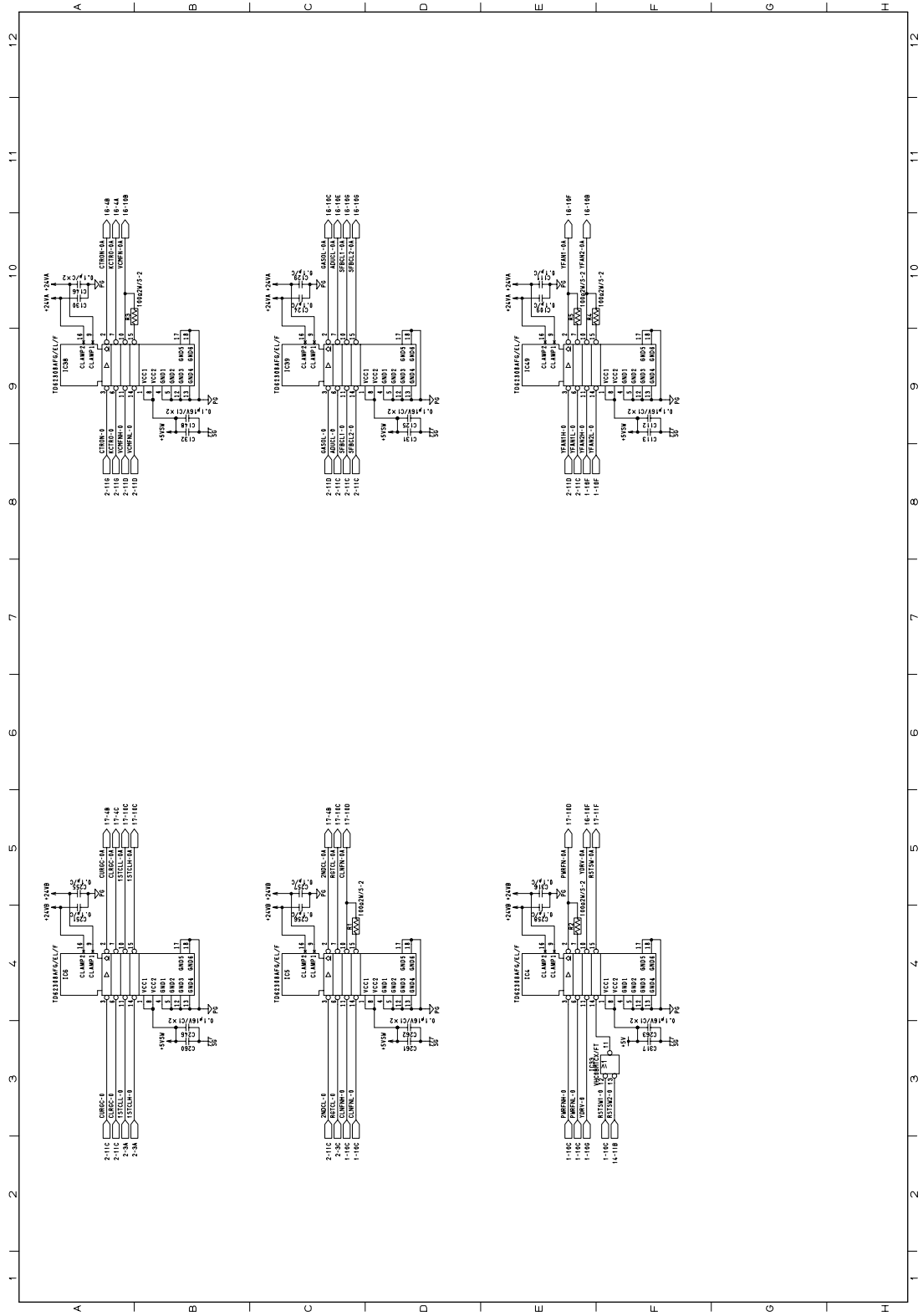


Fig. 3-30



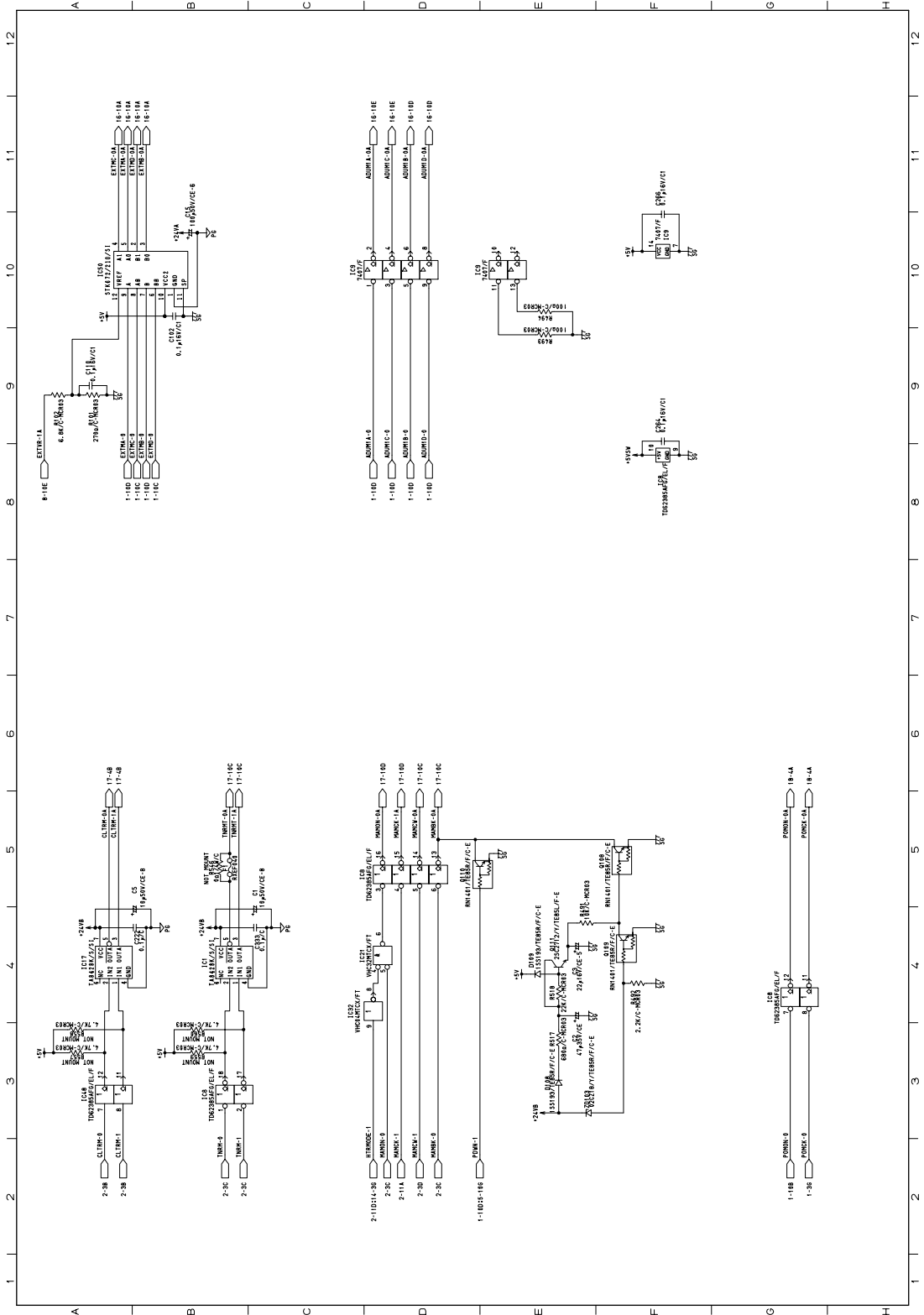


Fig. 3-31

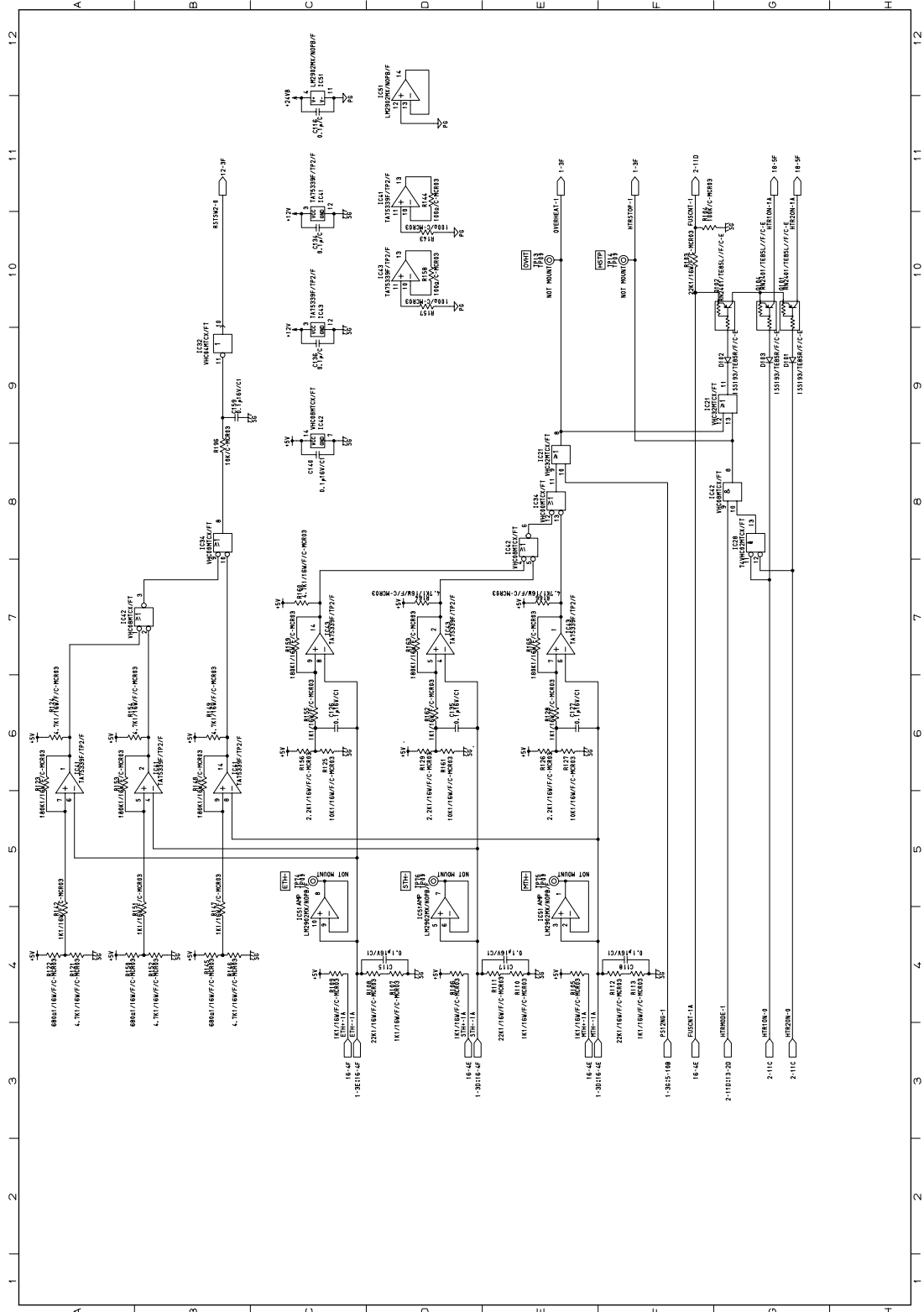


Fig. 3-32



LGC board 15/19

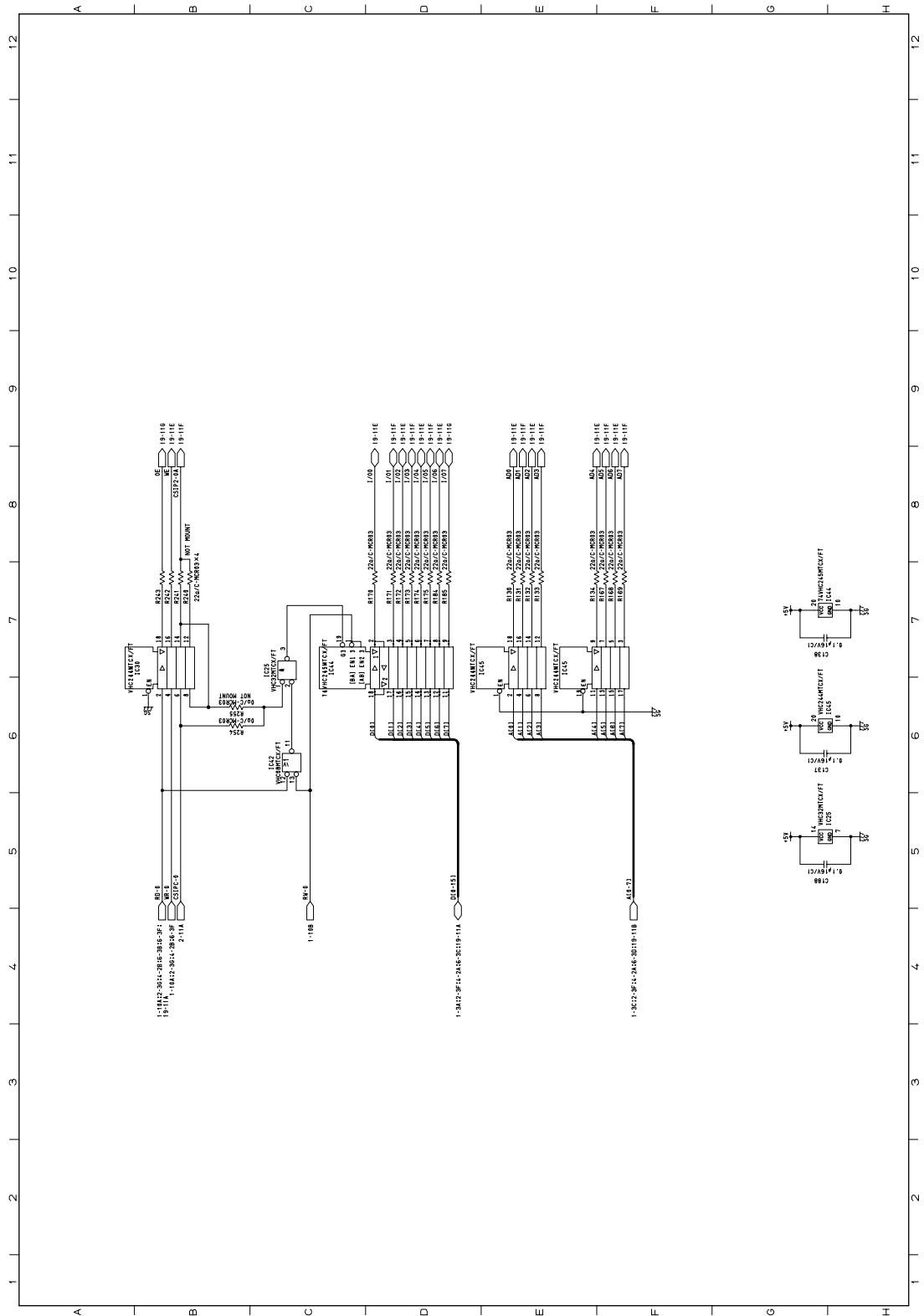


Fig. 3-33

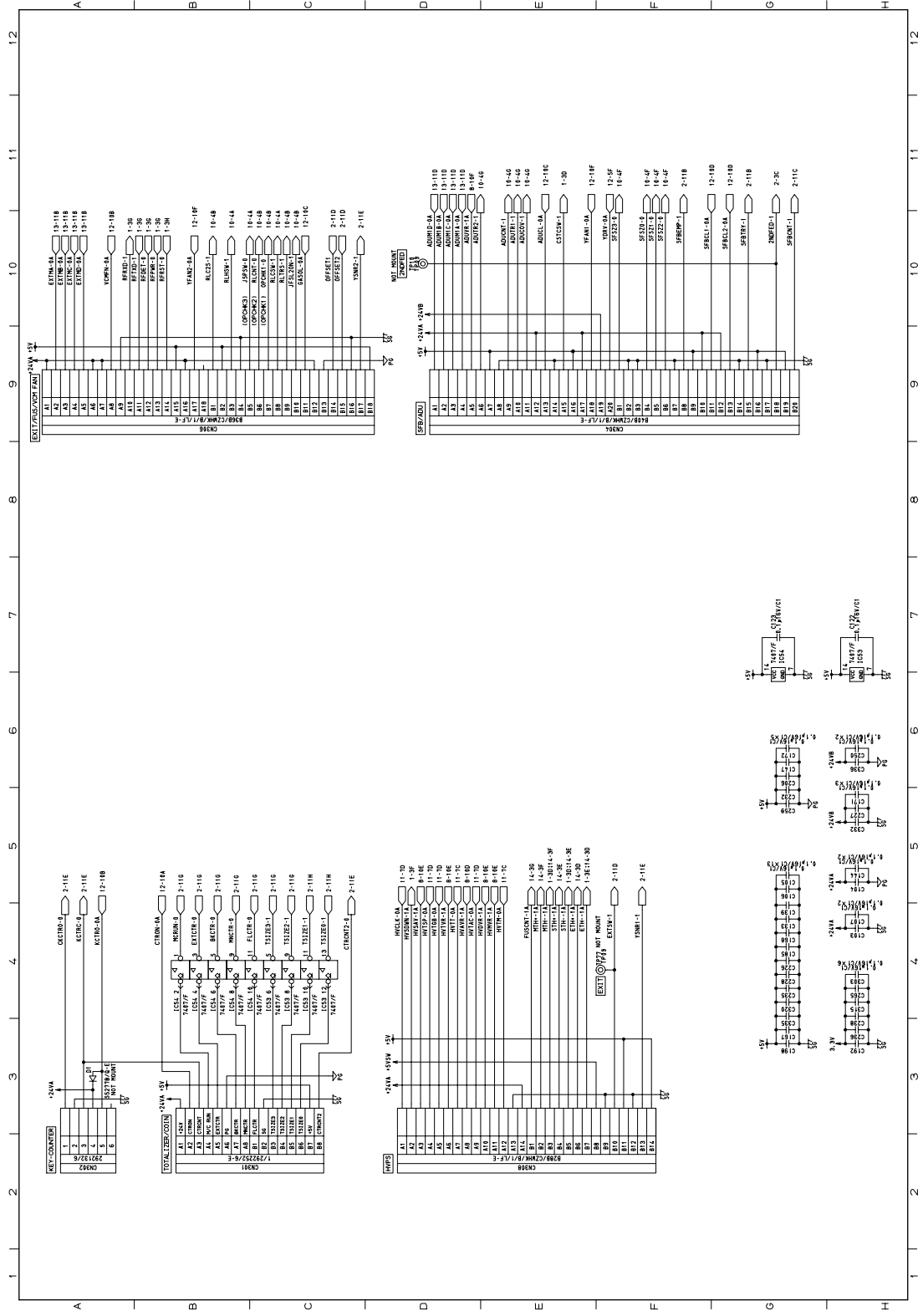


Fig. 3-34



LGC board 17/19

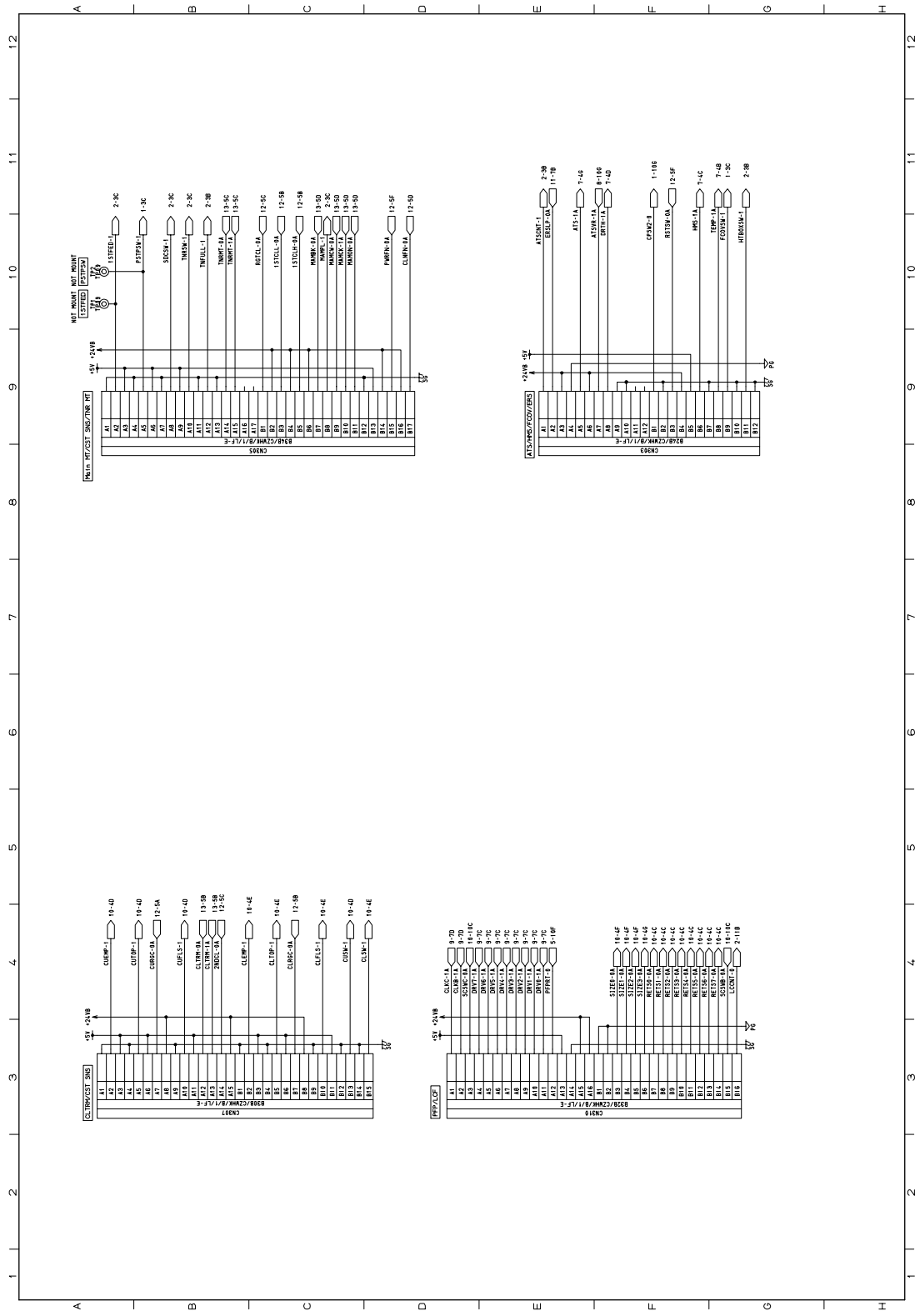


Fig. 3-35

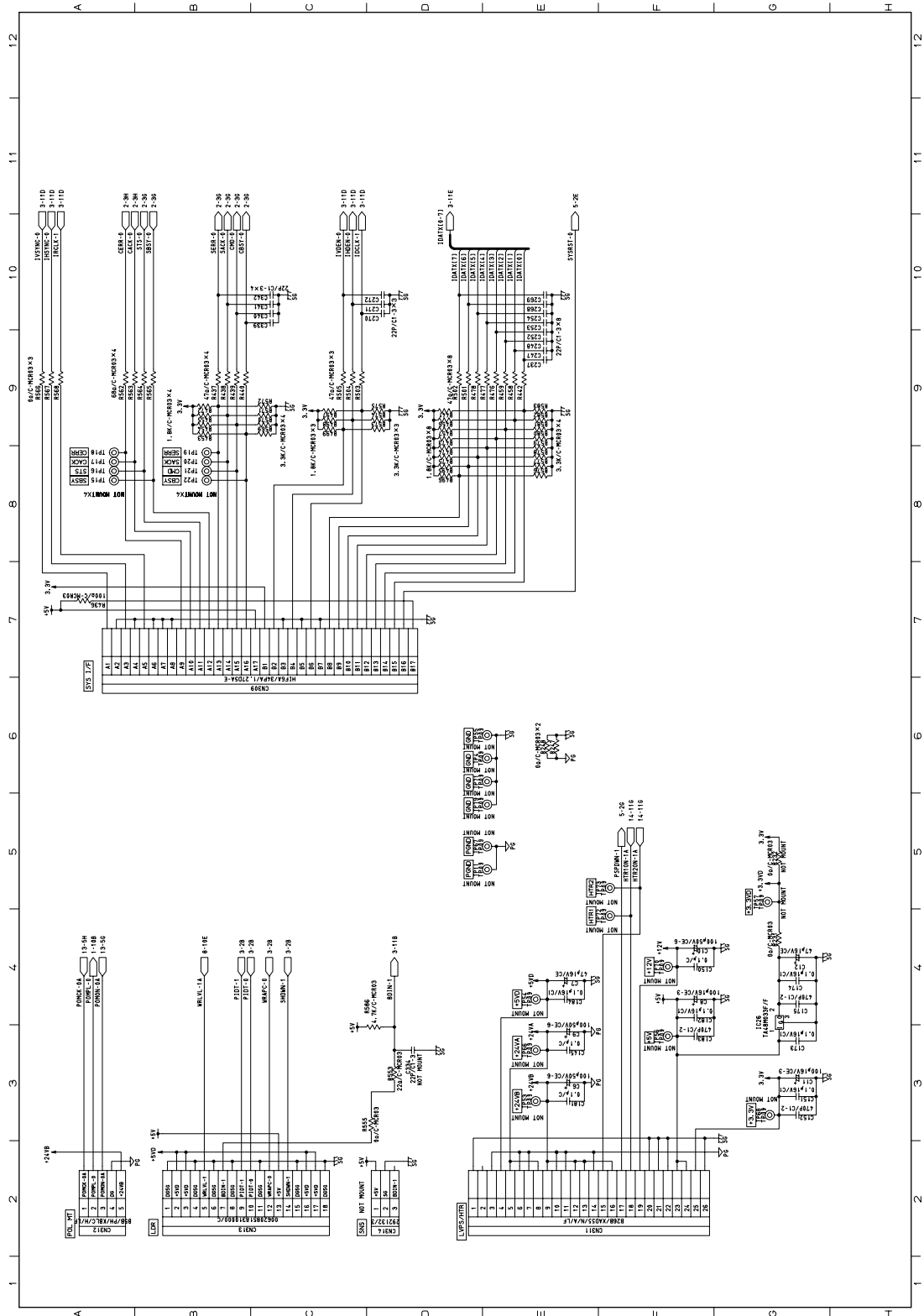


Fig. 3-36



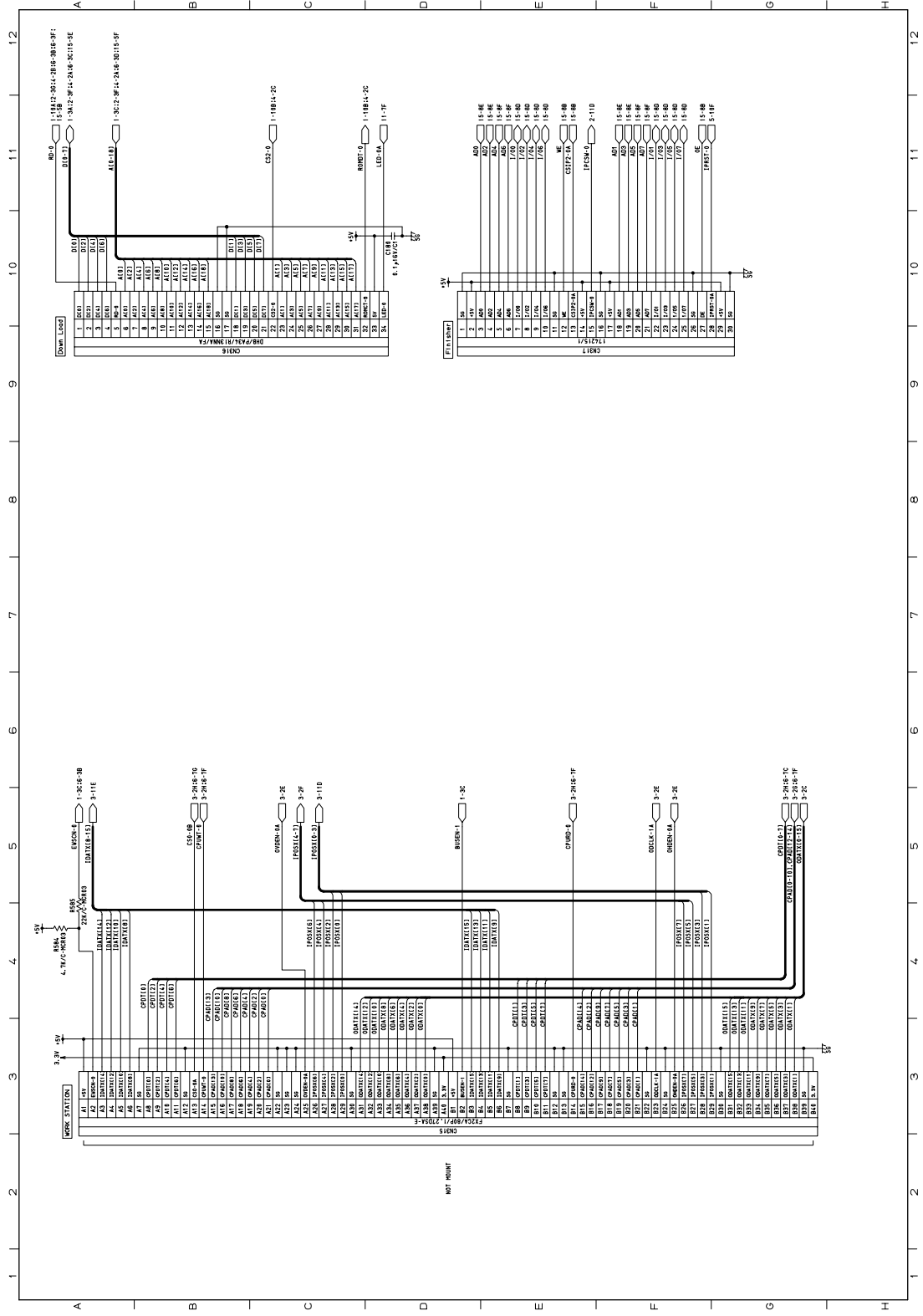


Fig. 3-37

3.3 Scanning section control circuit (SLG board)

SLG board 1/13

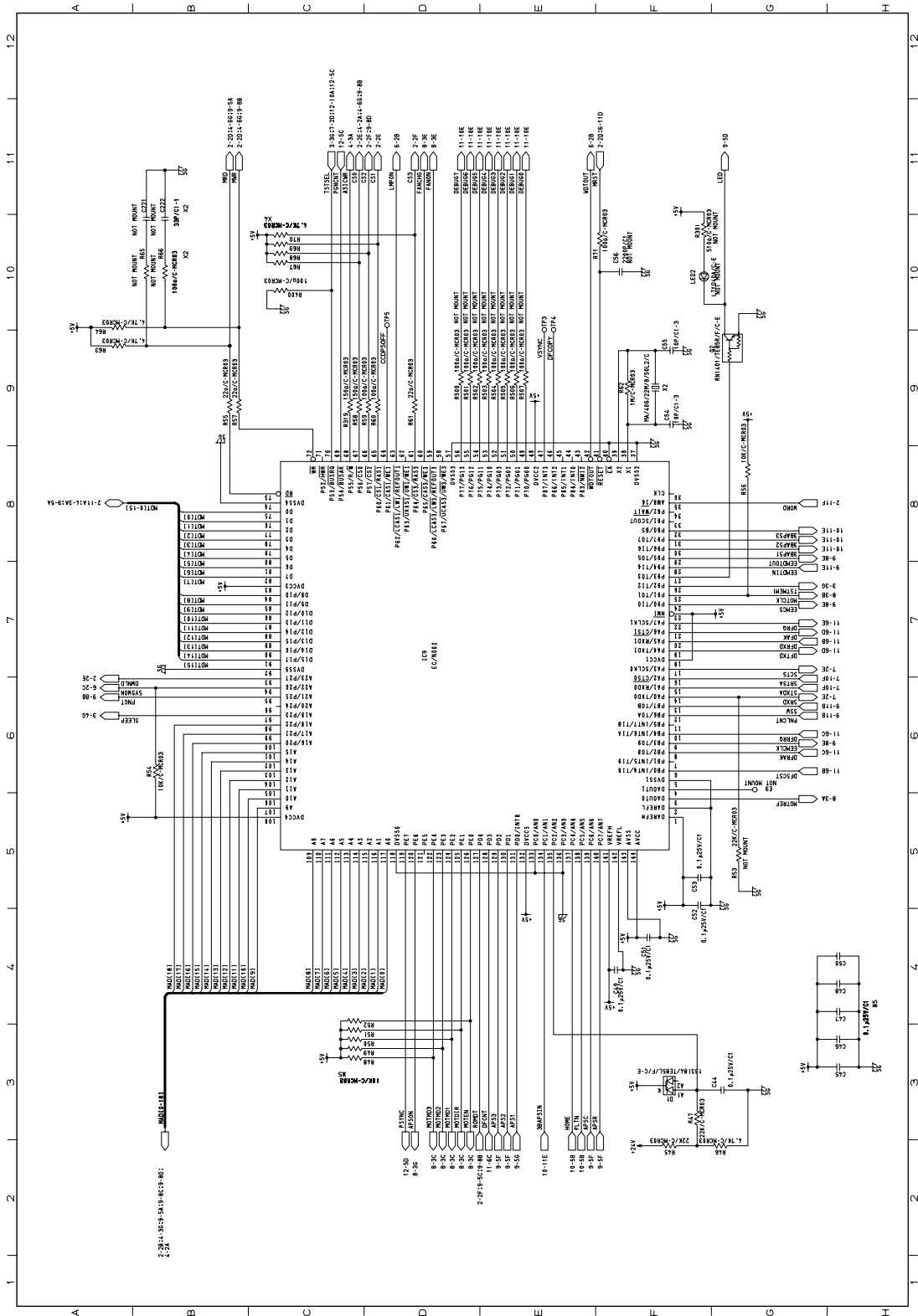


Fig. 3-38



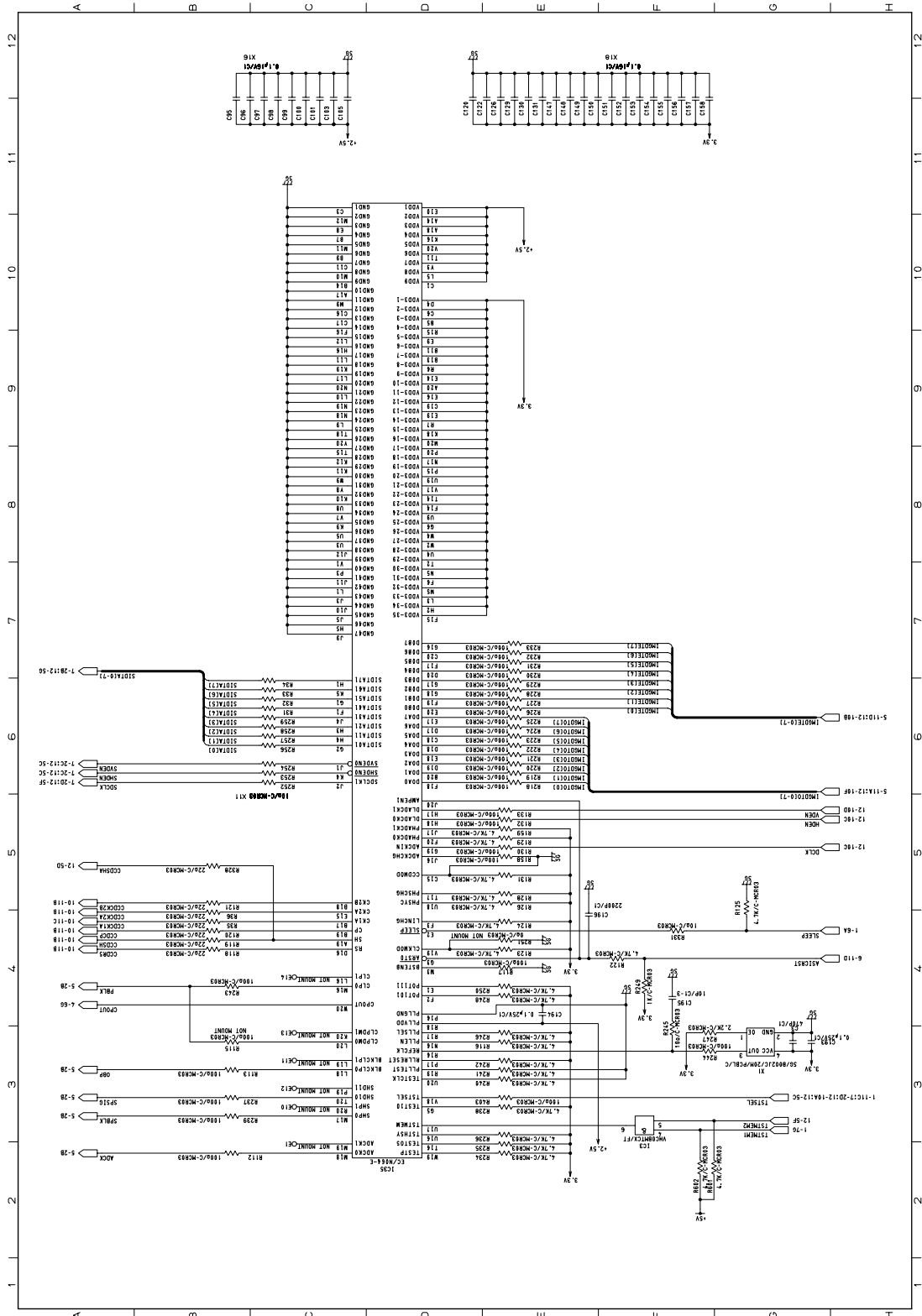


Fig. 3-40



SLG board 4/13

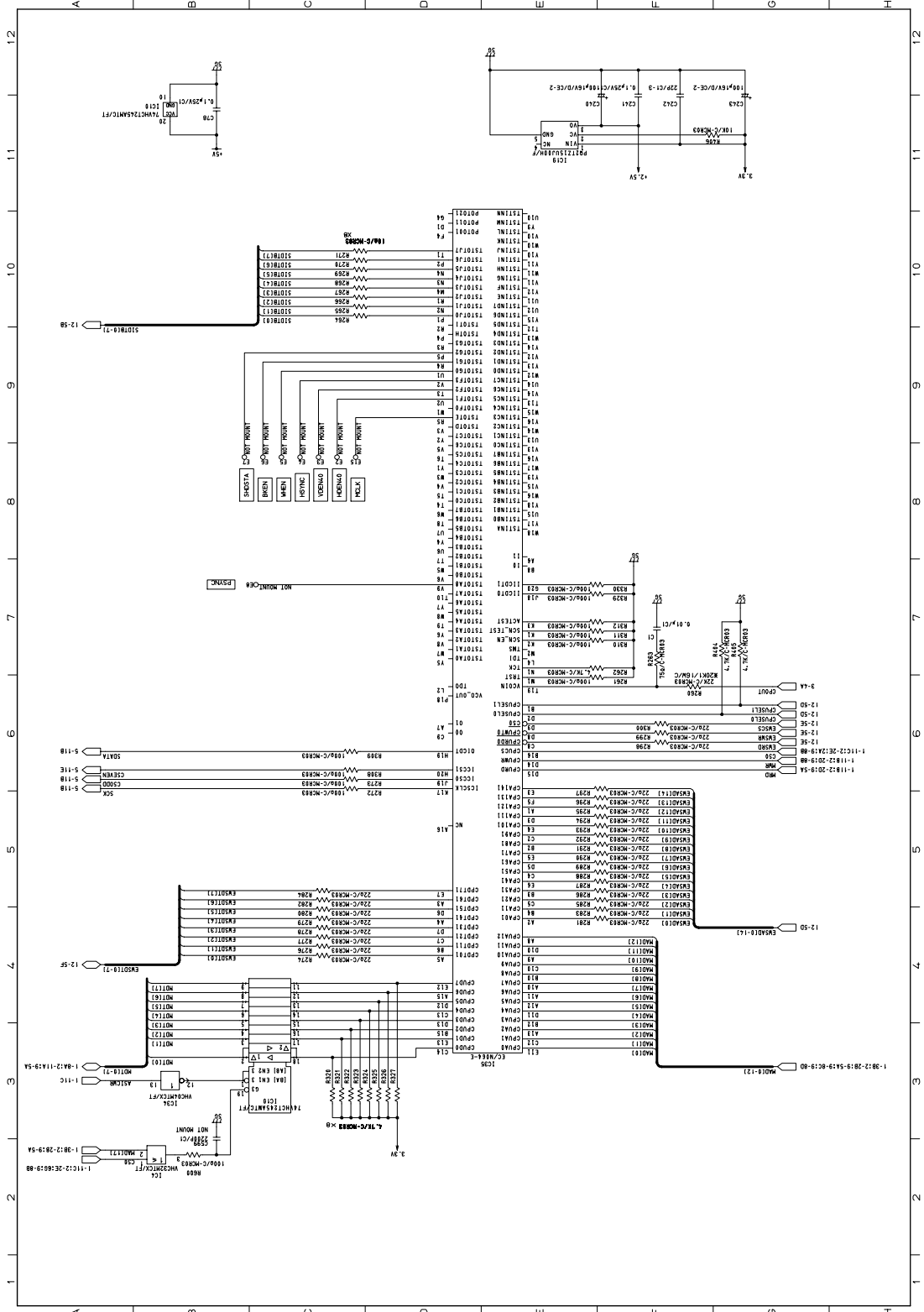


Fig. 3-41

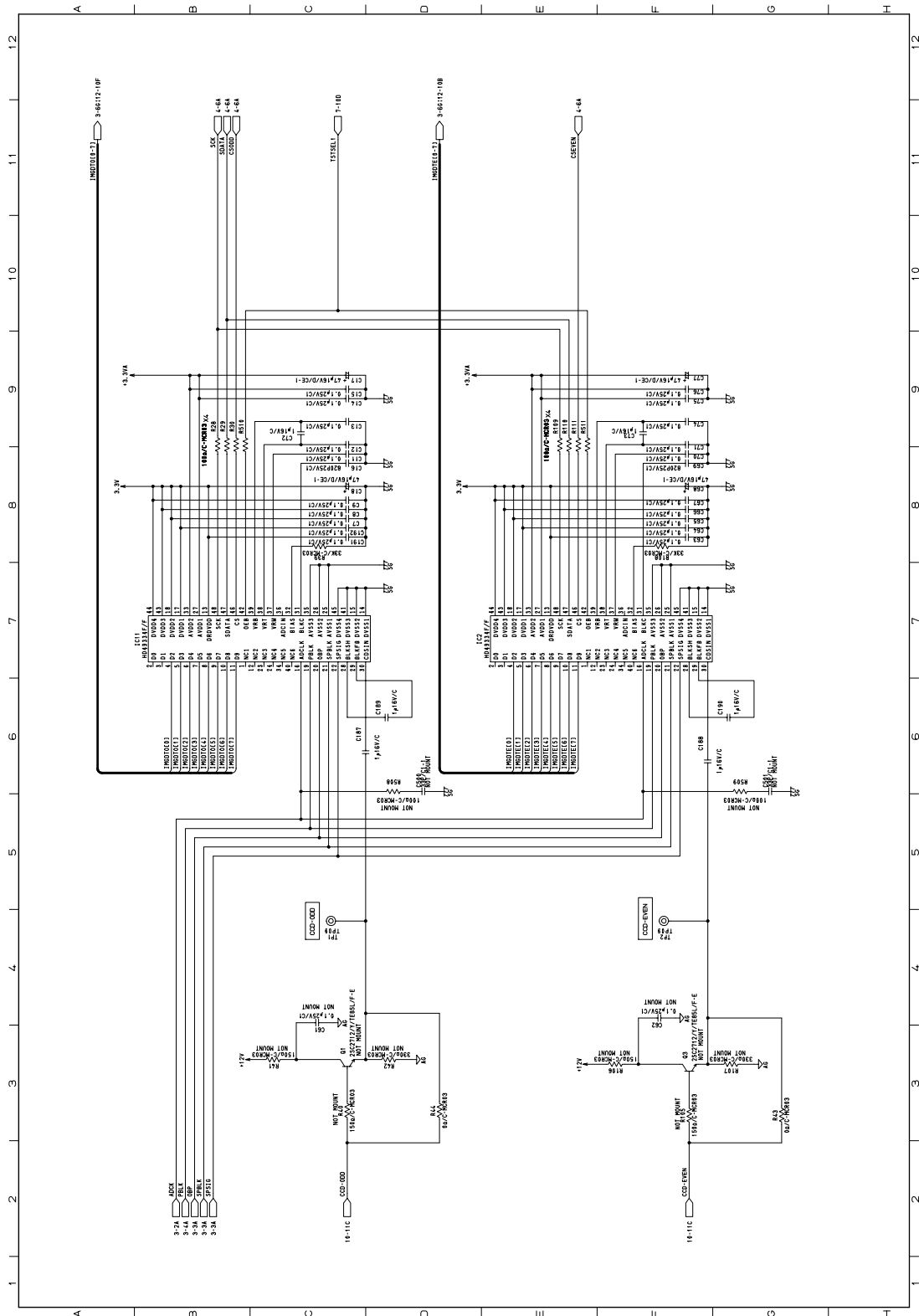


Fig. 3-42



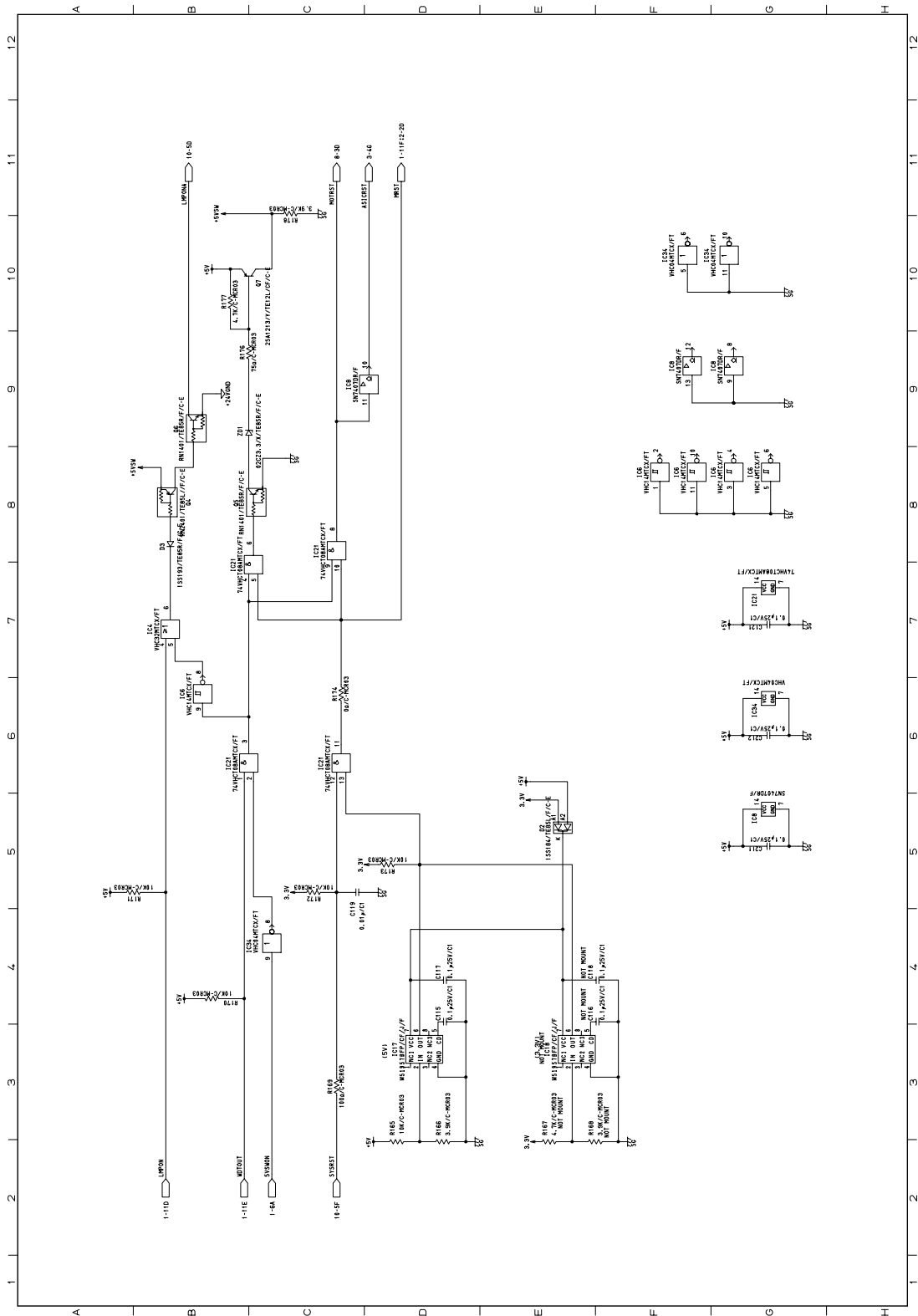


Fig. 3-43

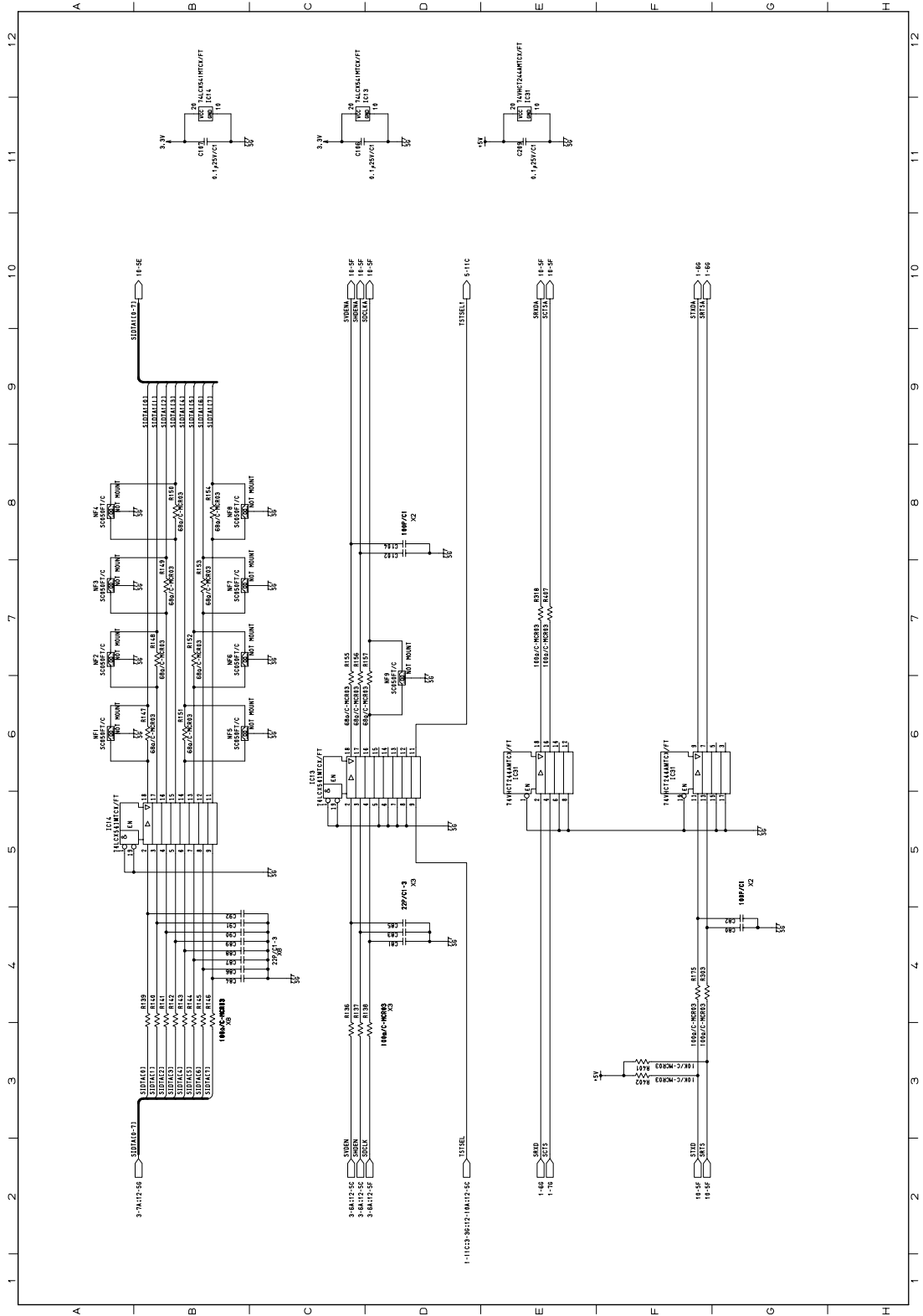


Fig. 3-44



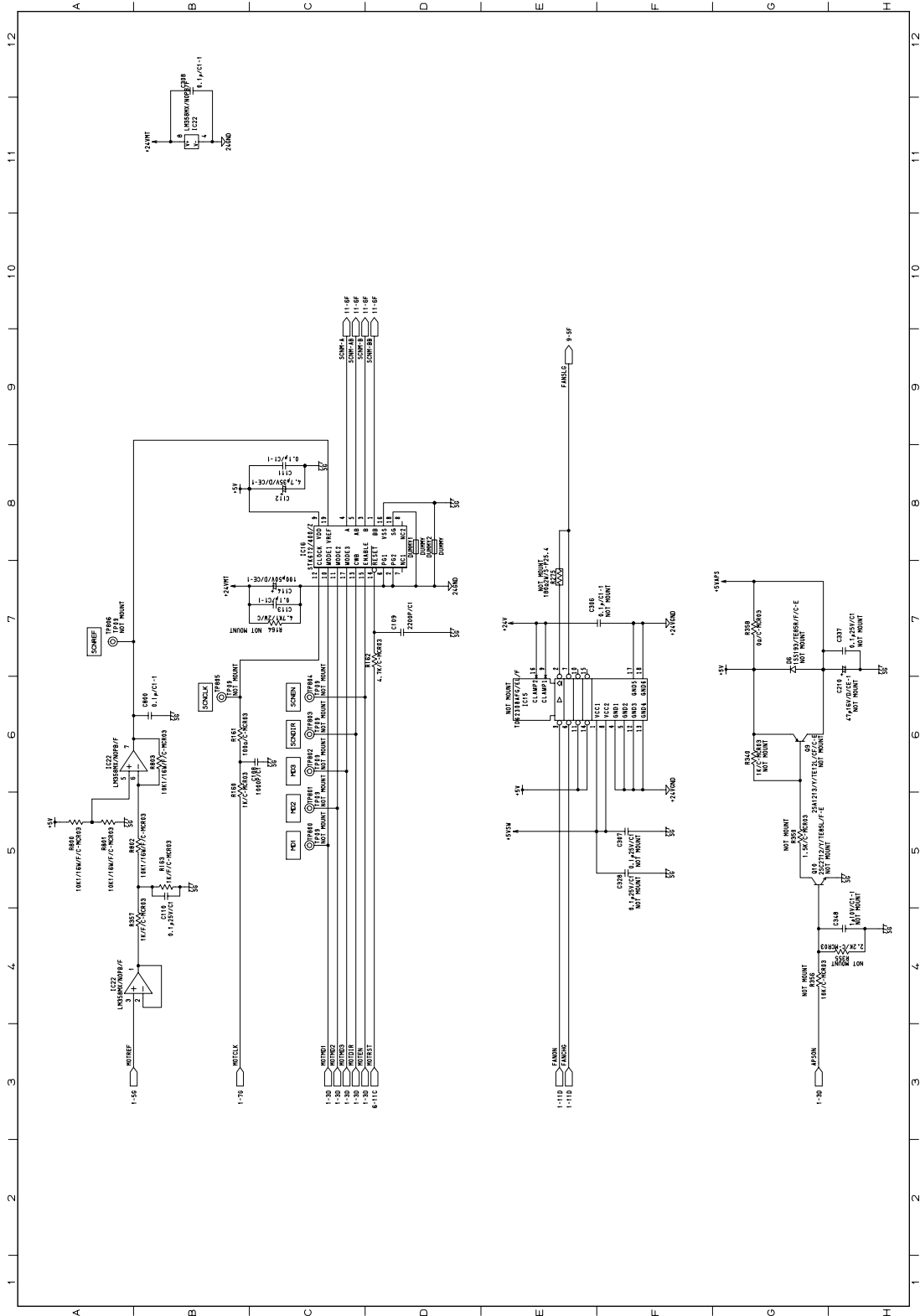


Fig. 3-45

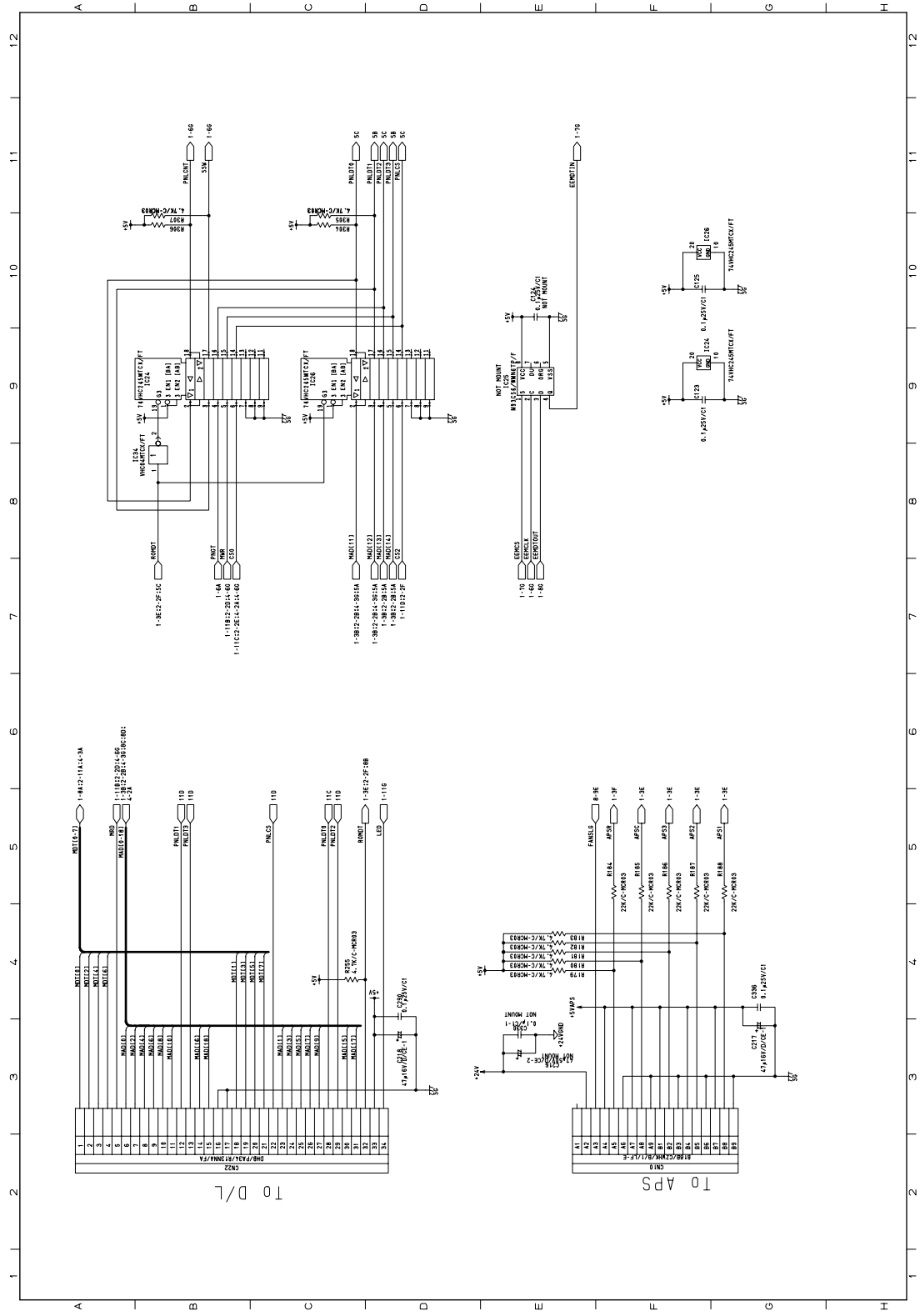


Fig. 3-46



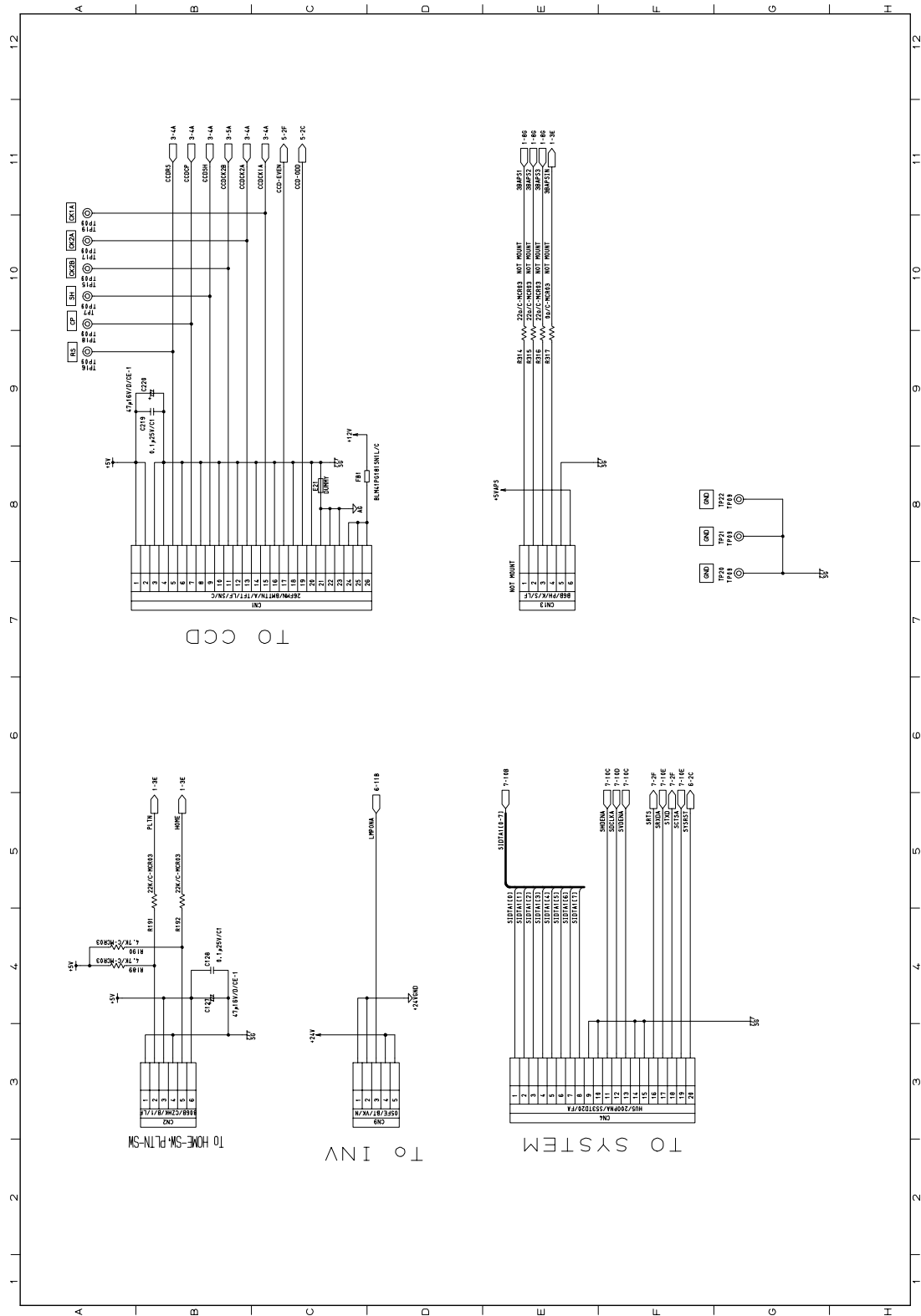


Fig. 3-47

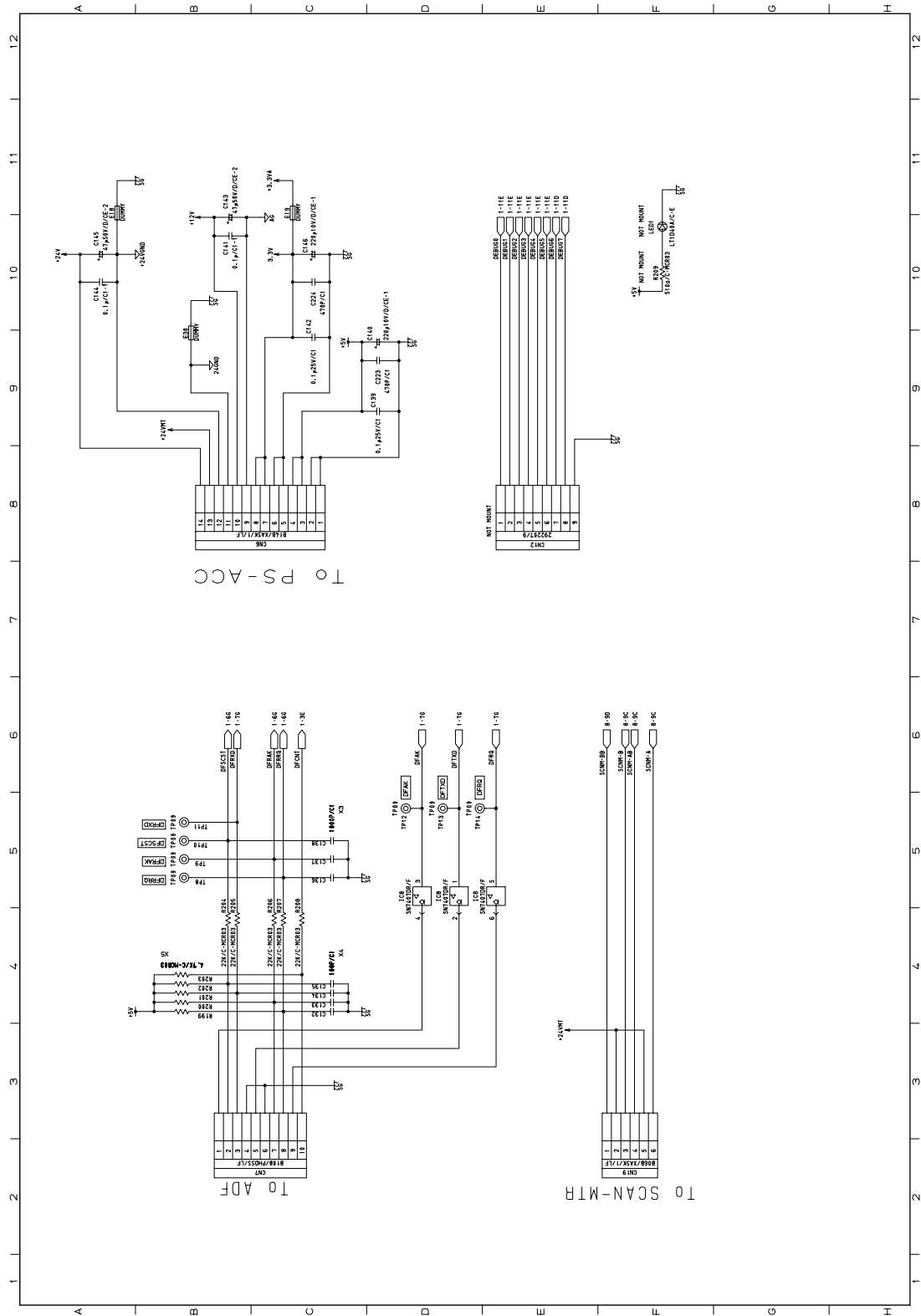


Fig. 3-48

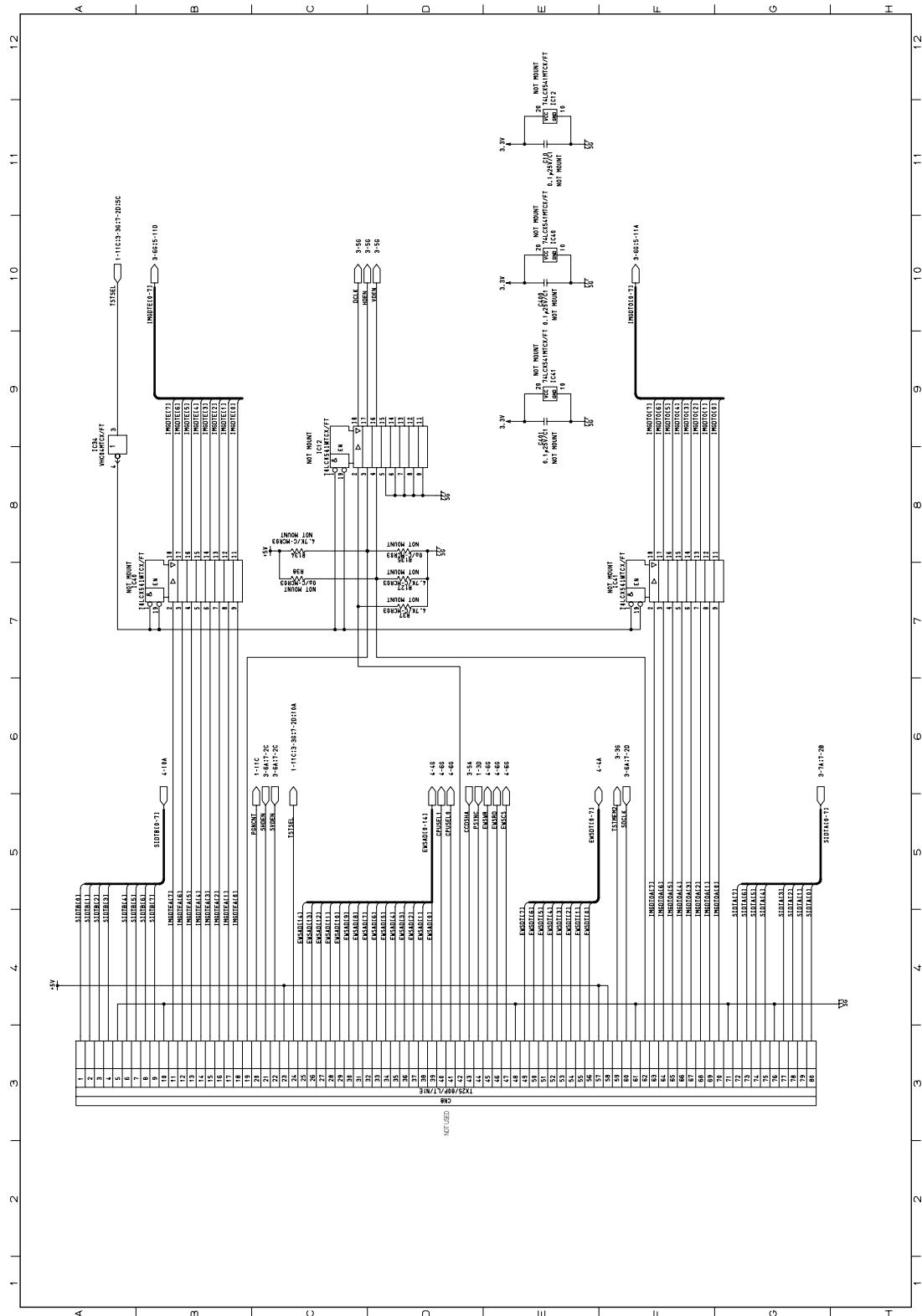


Fig. 3-49

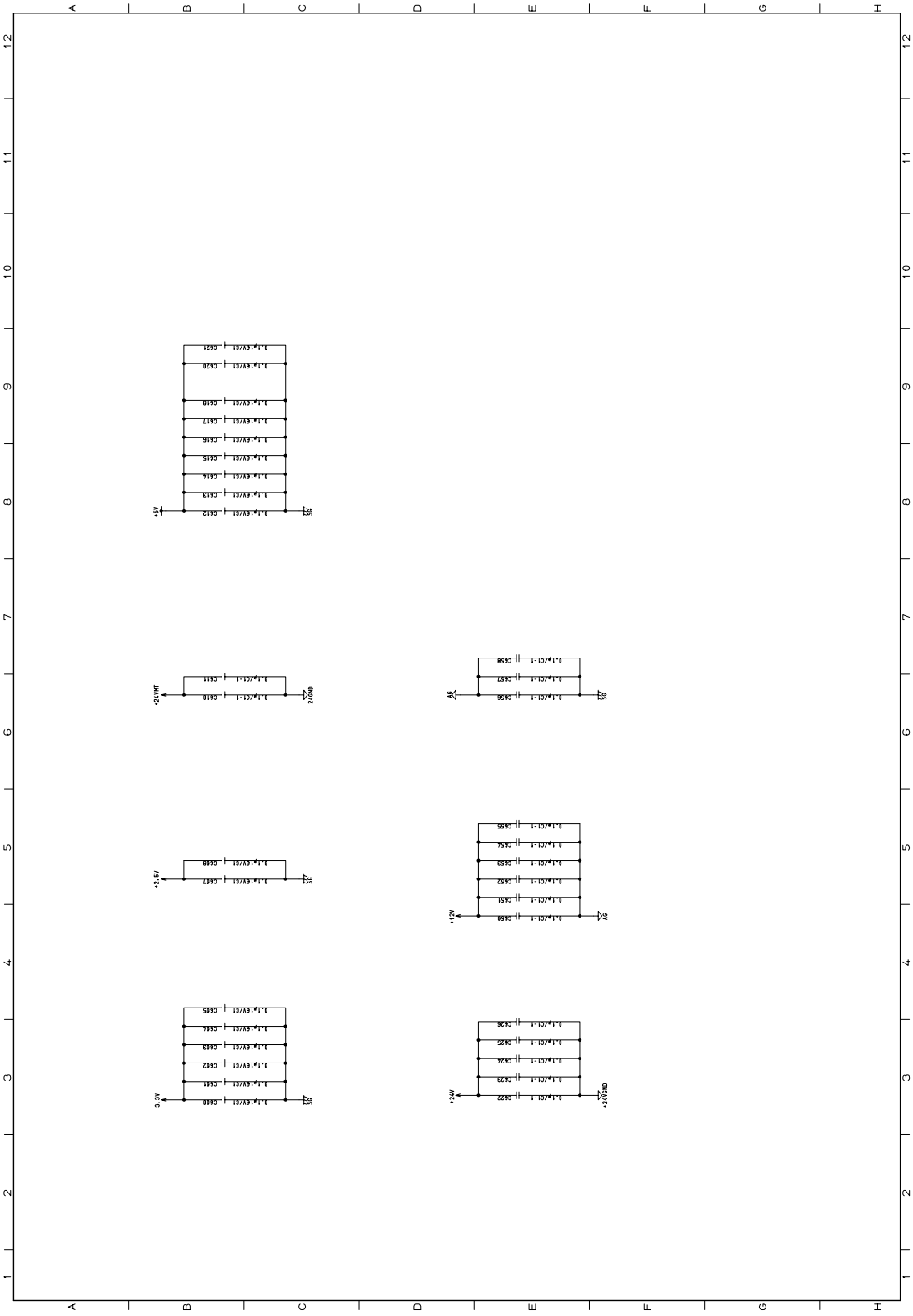


Fig. 3-50

3.4 CCD drive circuit (CCD board)

CCD board 1/2

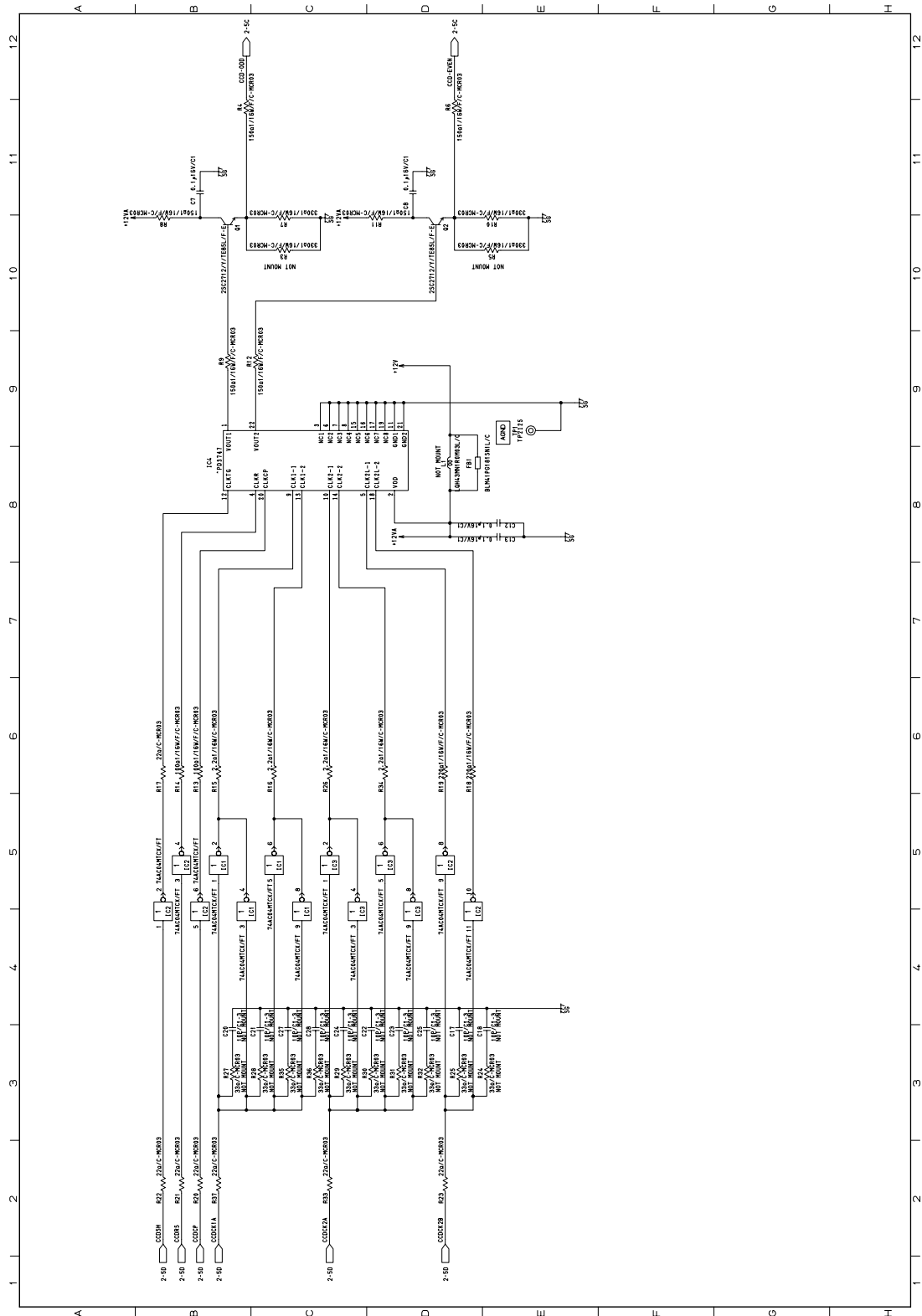


Fig. 3-51

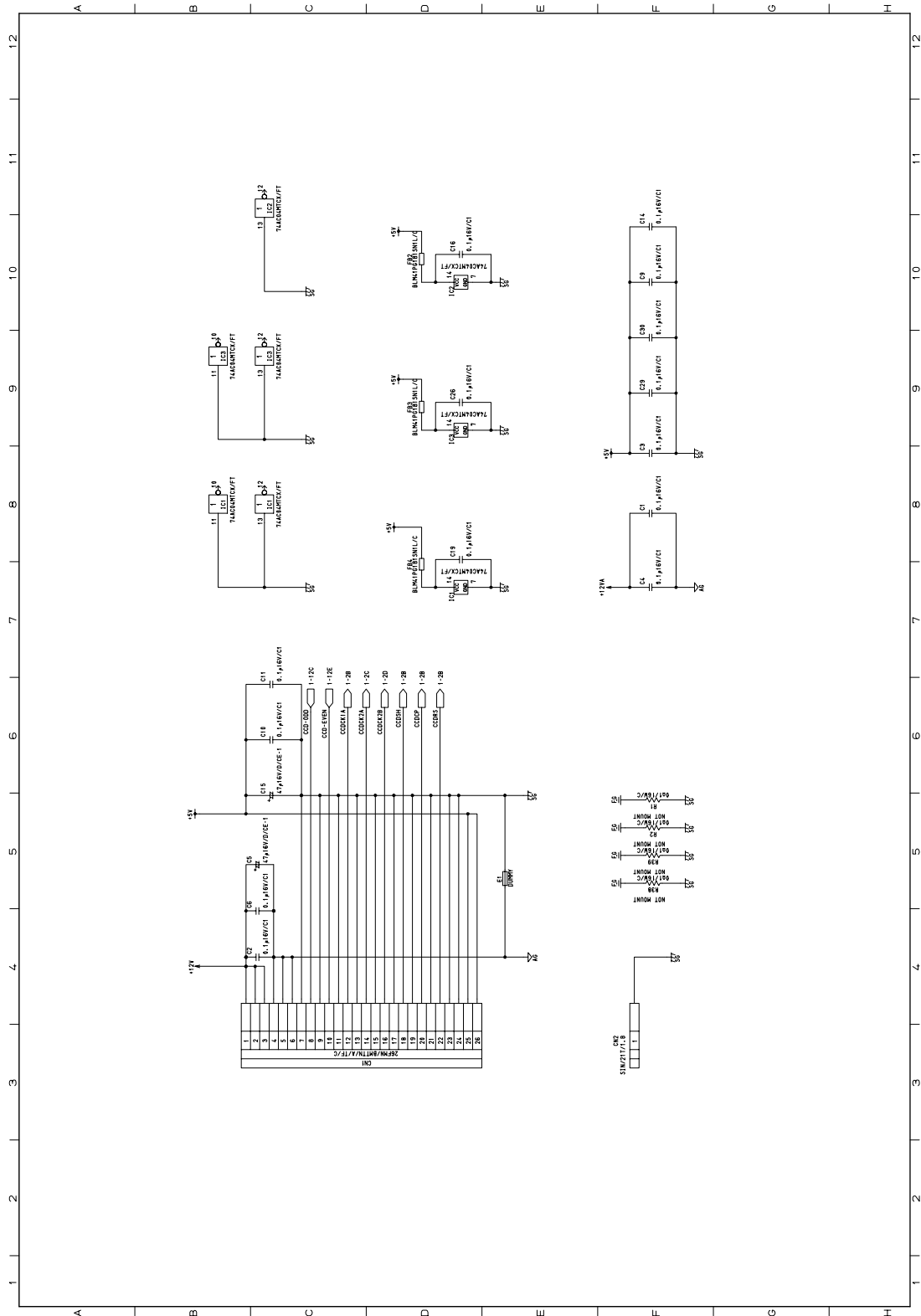


Fig. 3-52

3.5 Laser control signal relay circuit (LRL board)

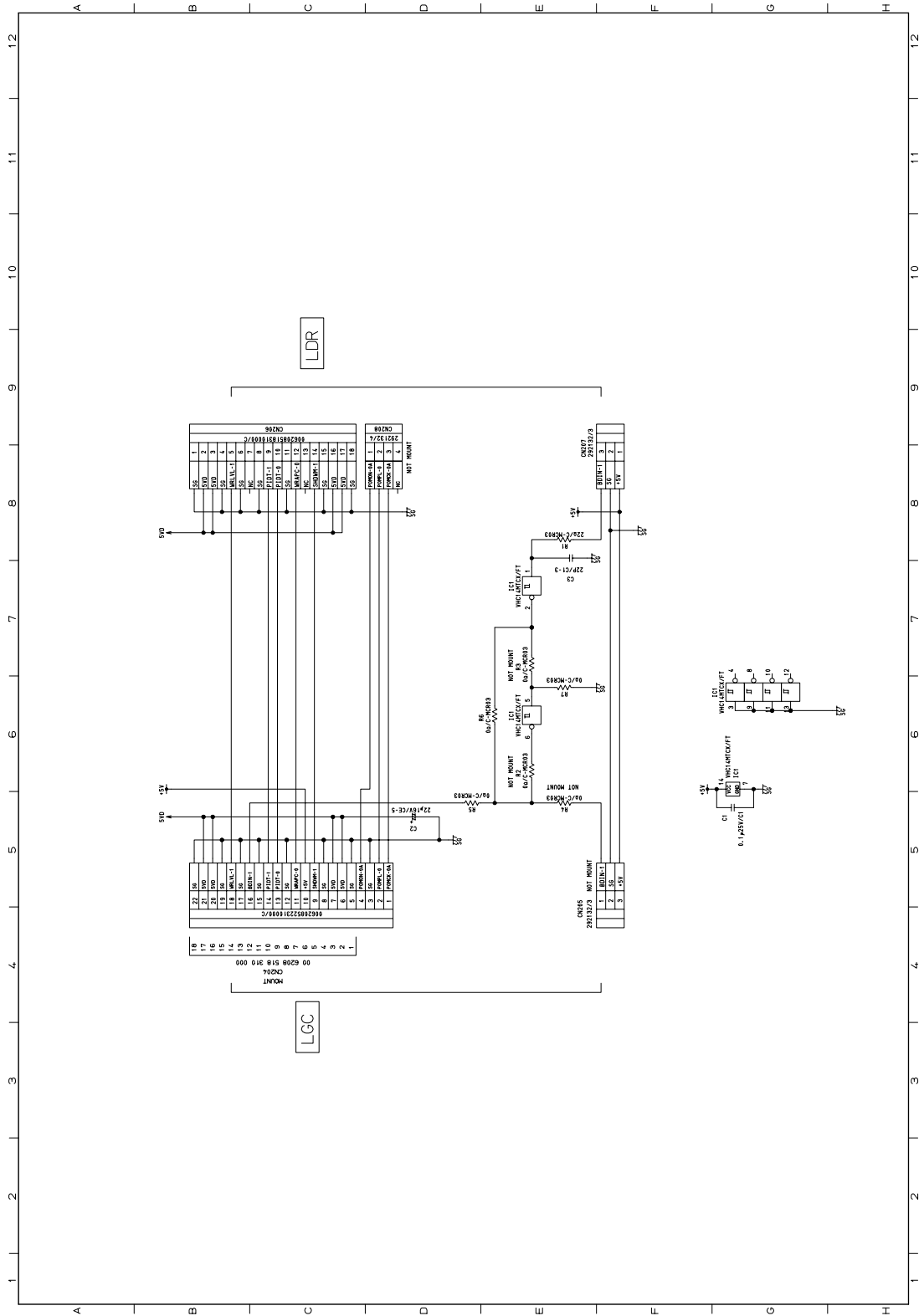


Fig. 3-53

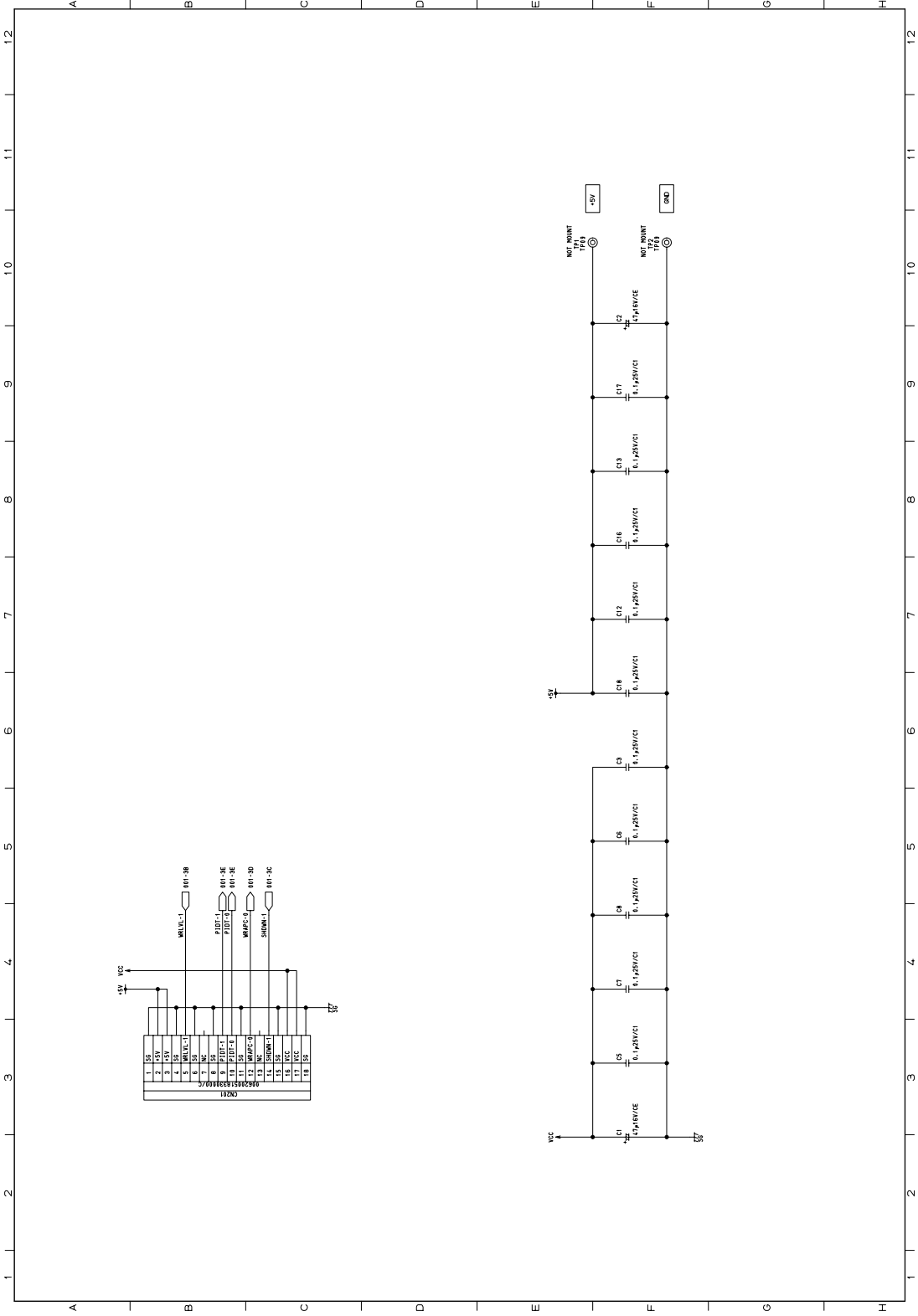


Fig. 3-55

3.8 ADU drive circuit (ADU board)

ADU board 1/2

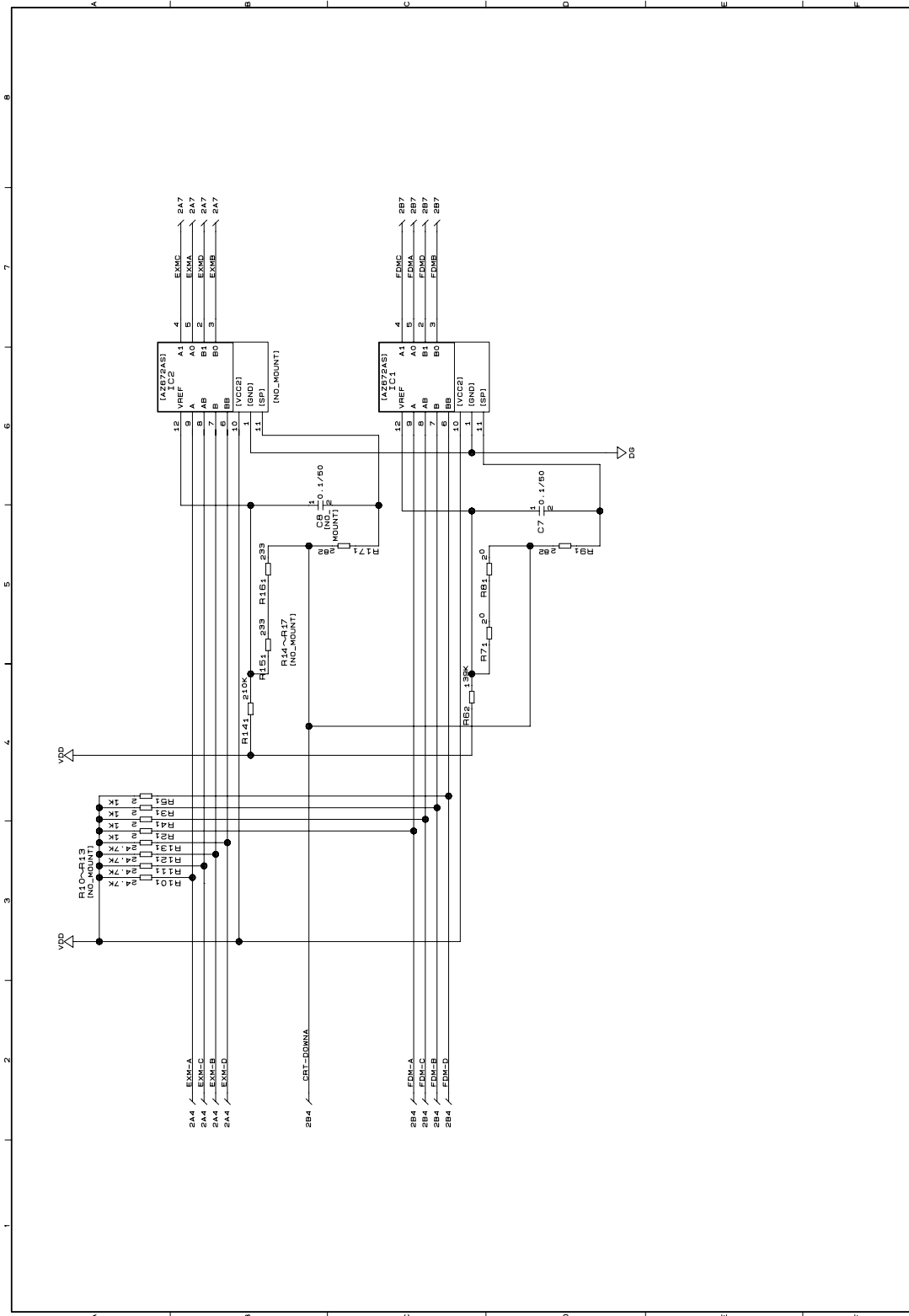


Fig. 3-57

ADU board 2/2

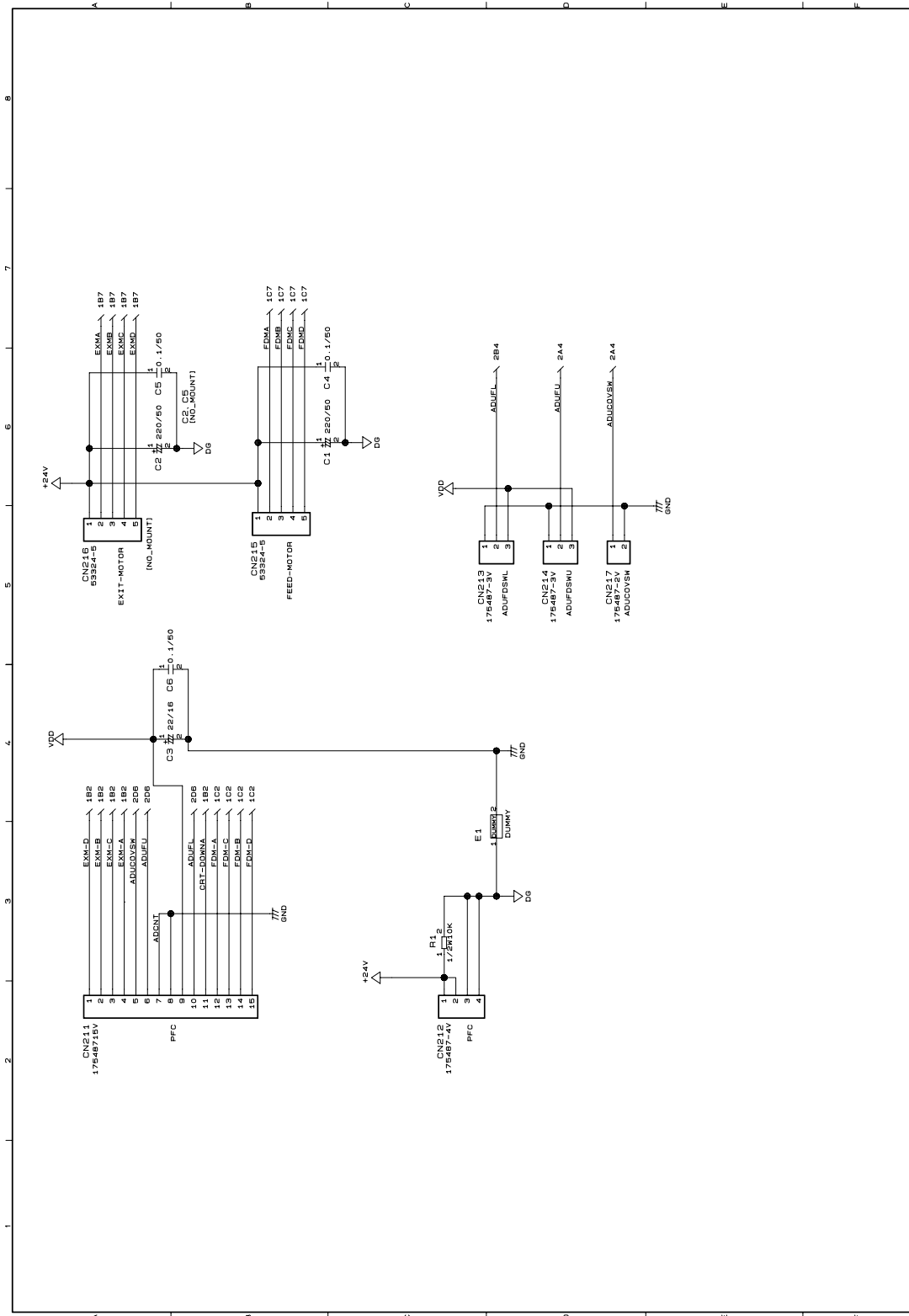


Fig. 3-58

3.9 Display circuit (DSP board)

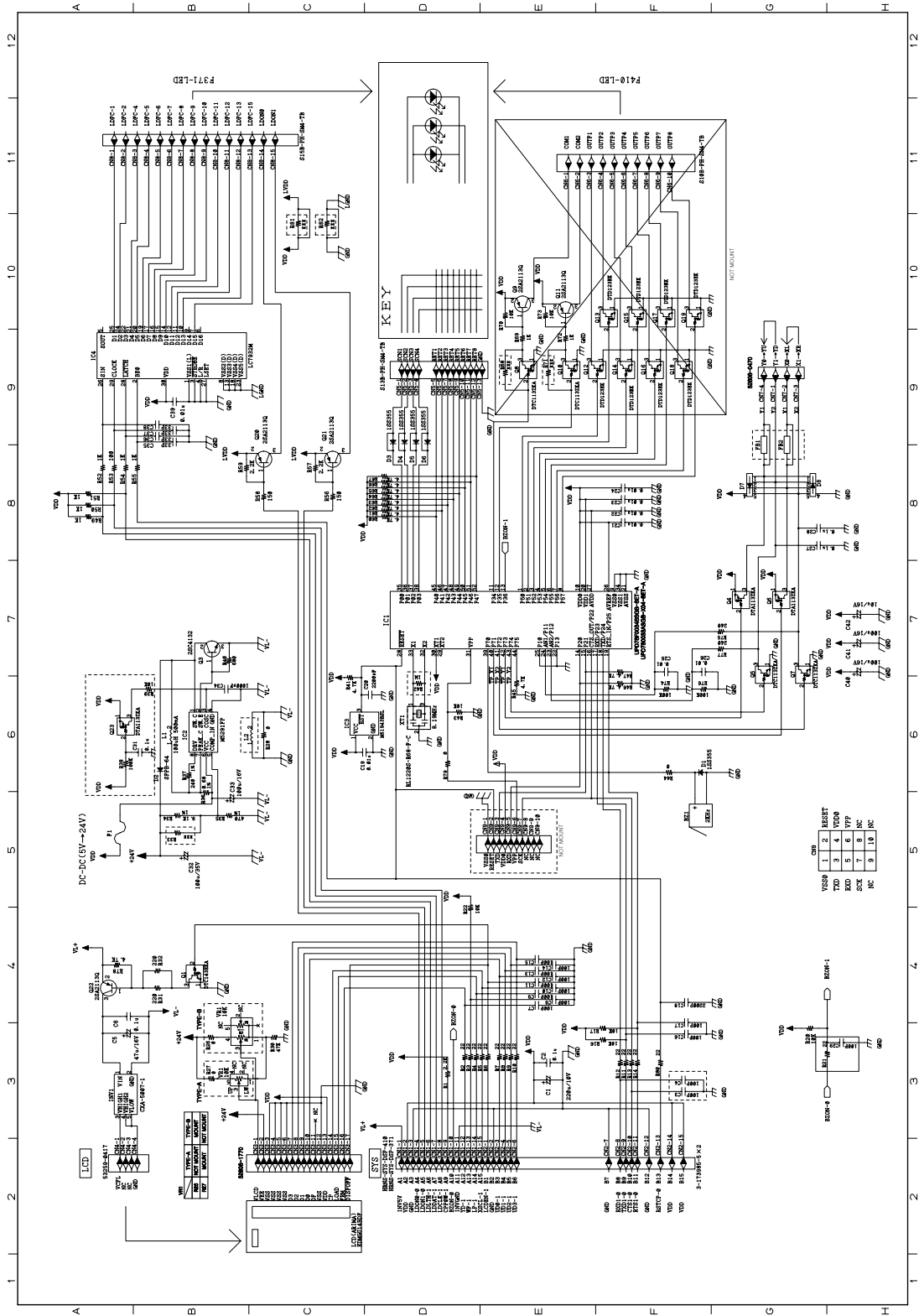


Fig. 3-59

3.10 Key control circuit (KEY board)

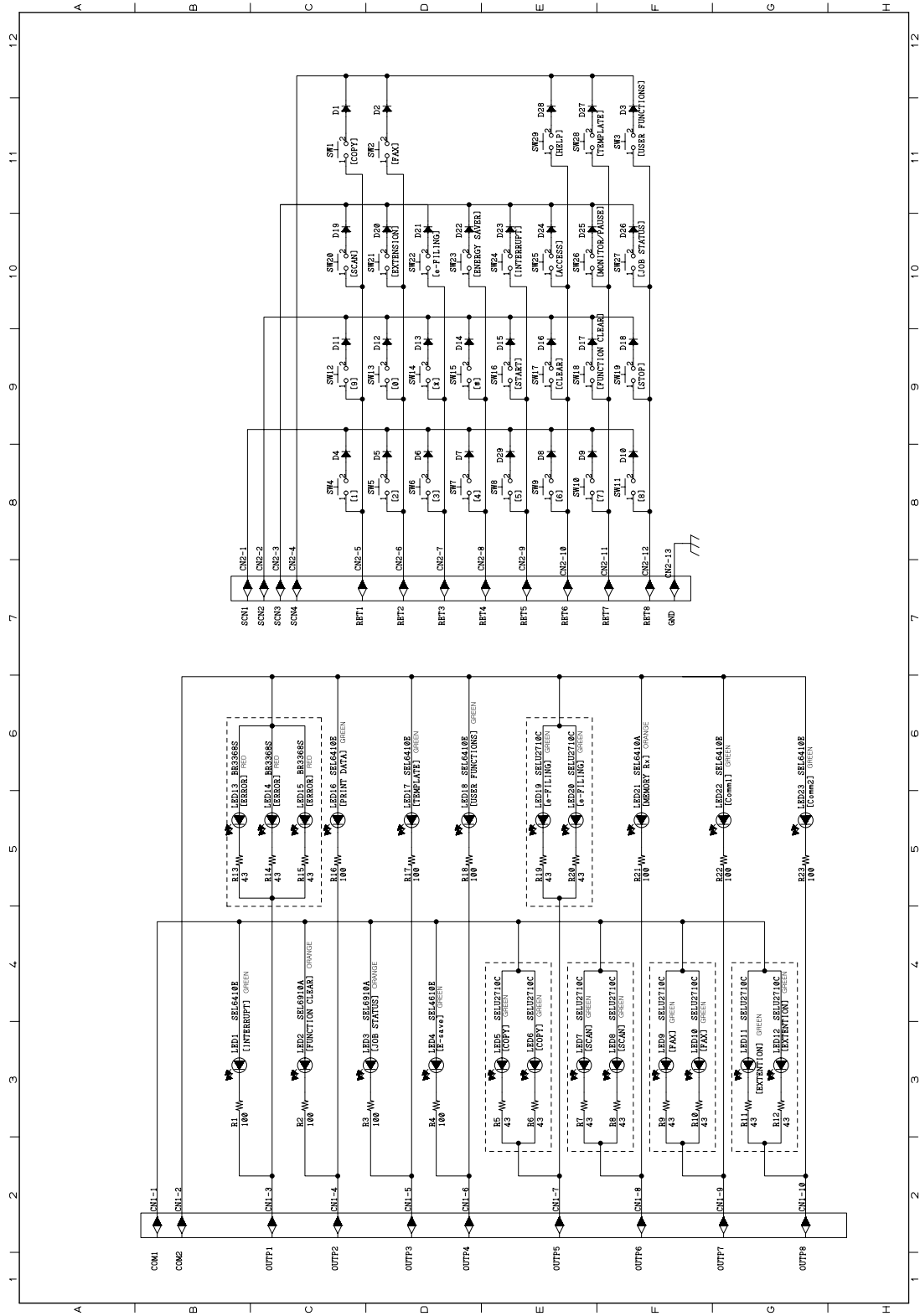


Fig. 3-60

3.11 Fuse circuit (FUS board)

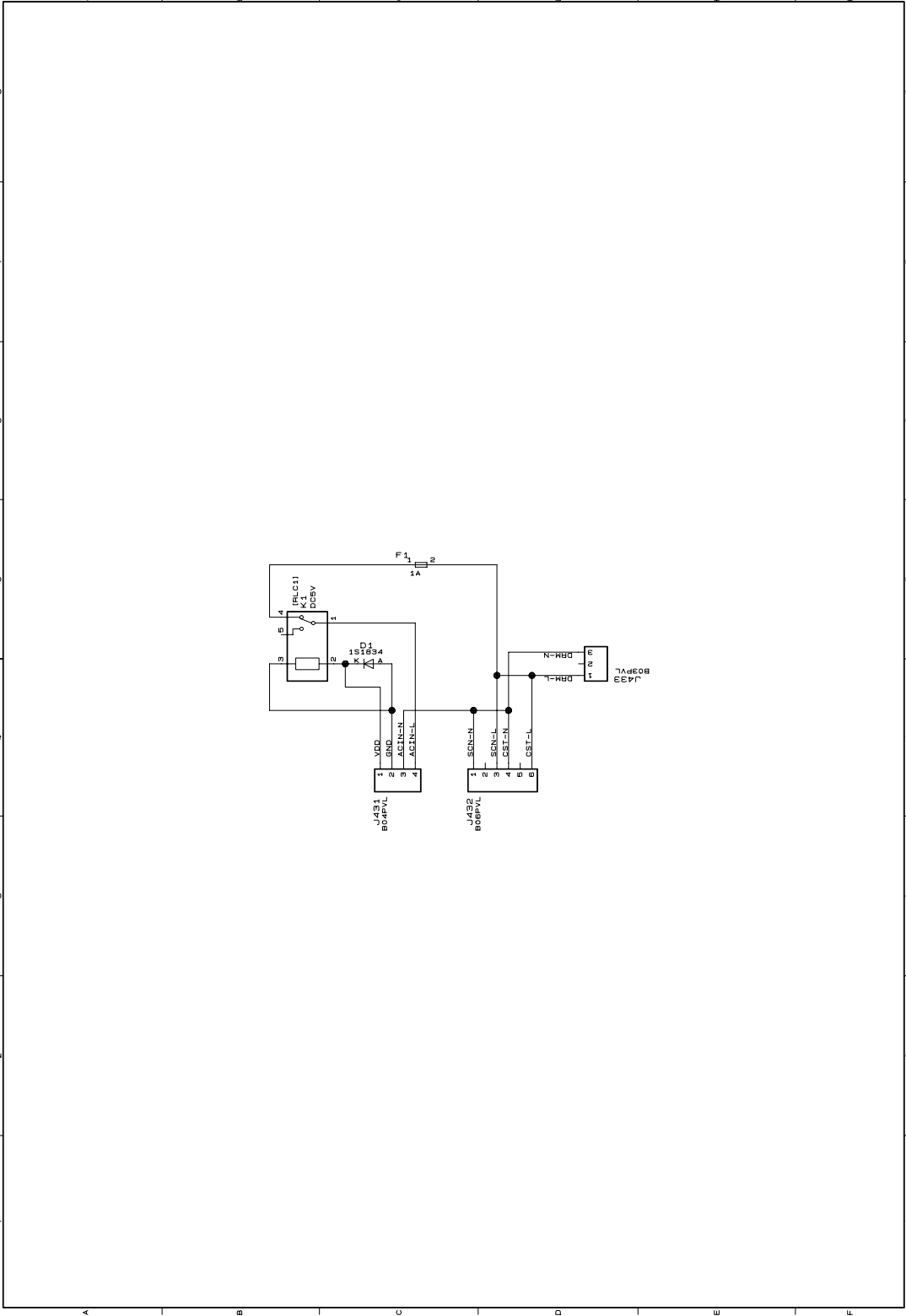


Fig. 3-61

3.12 Facsimile circuit (FAX board: GD-1150)

FAX board 1/14

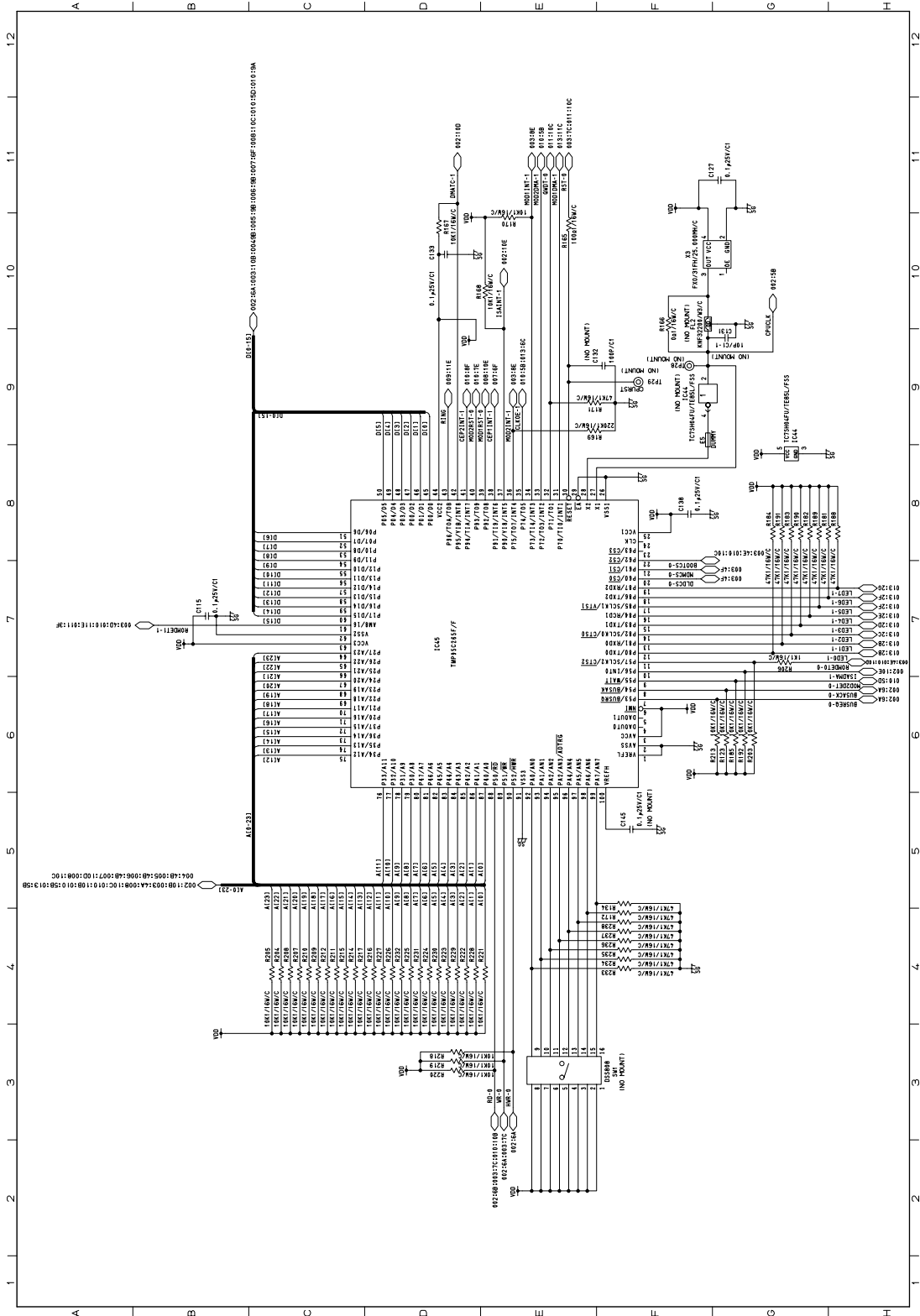


Fig. 3-62



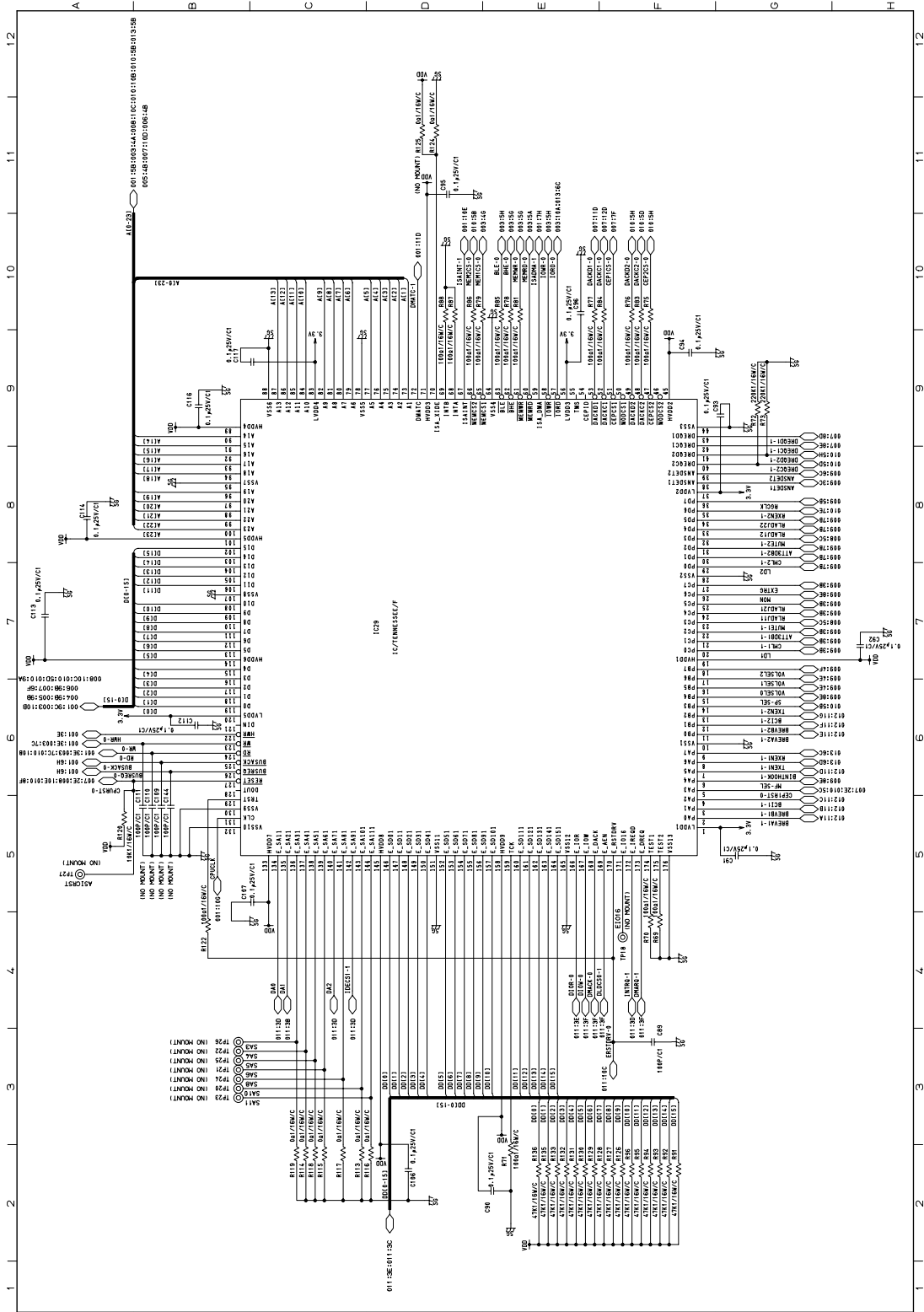


Fig. 3-63

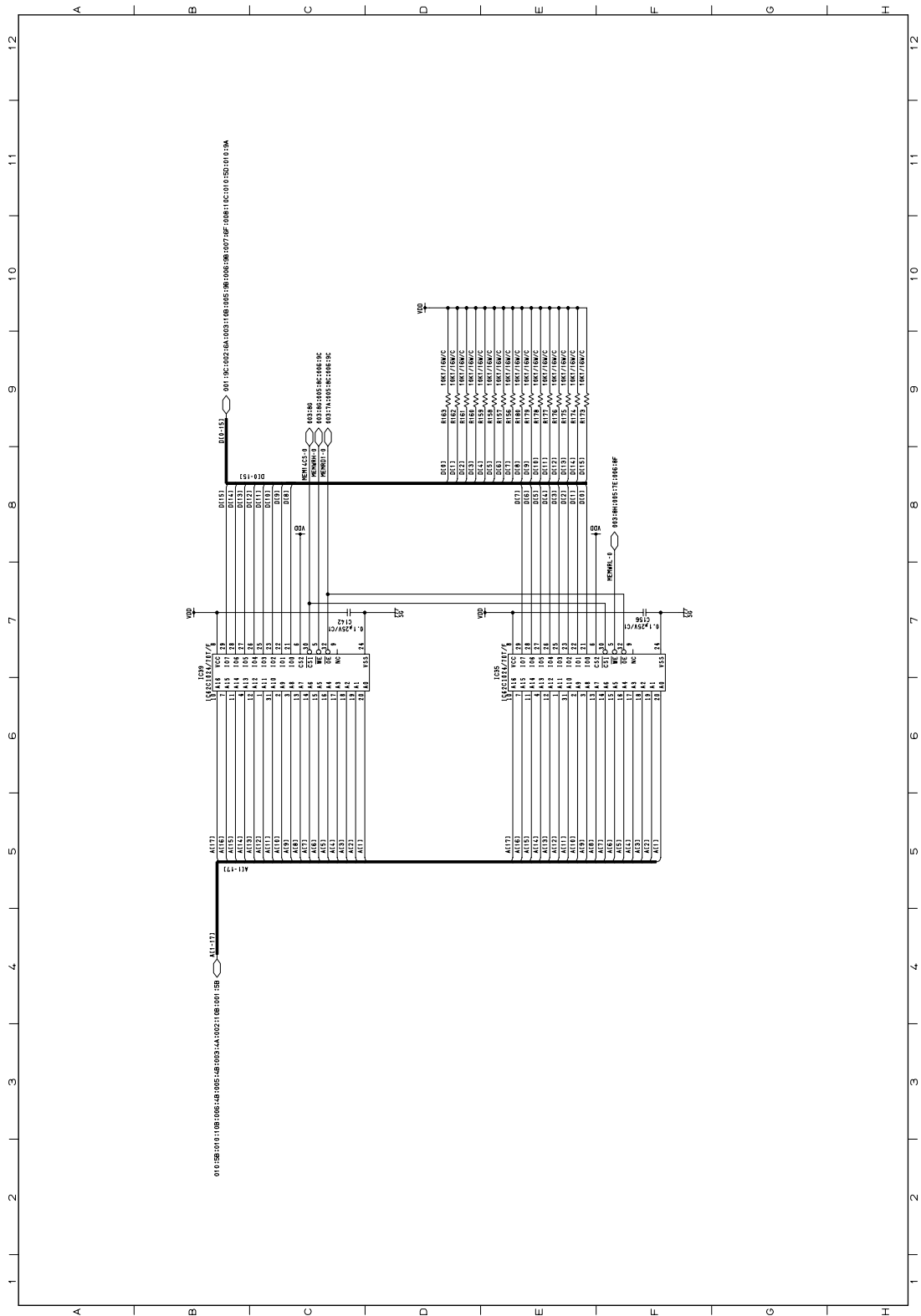


Fig. 3-65

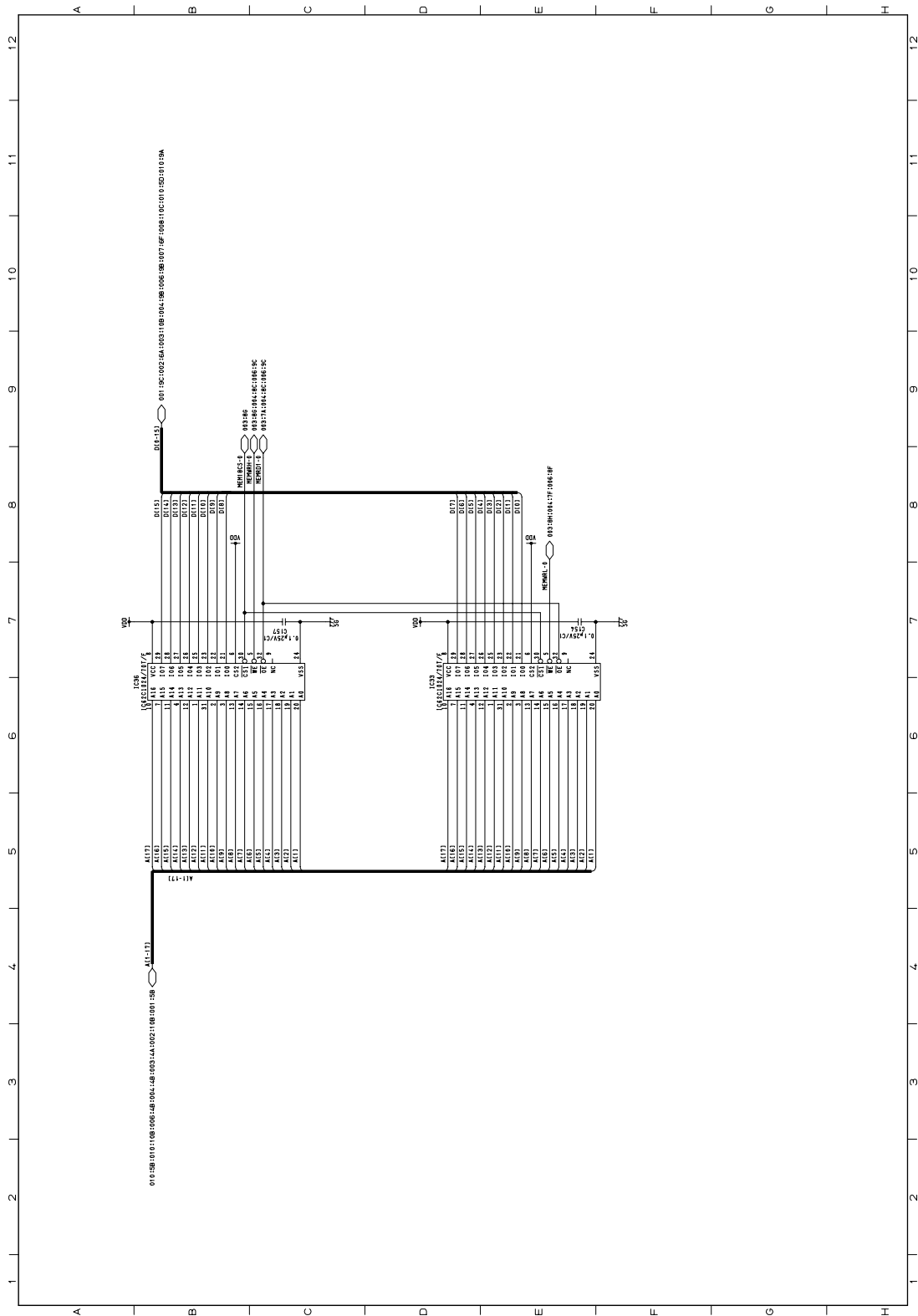


Fig. 3-66

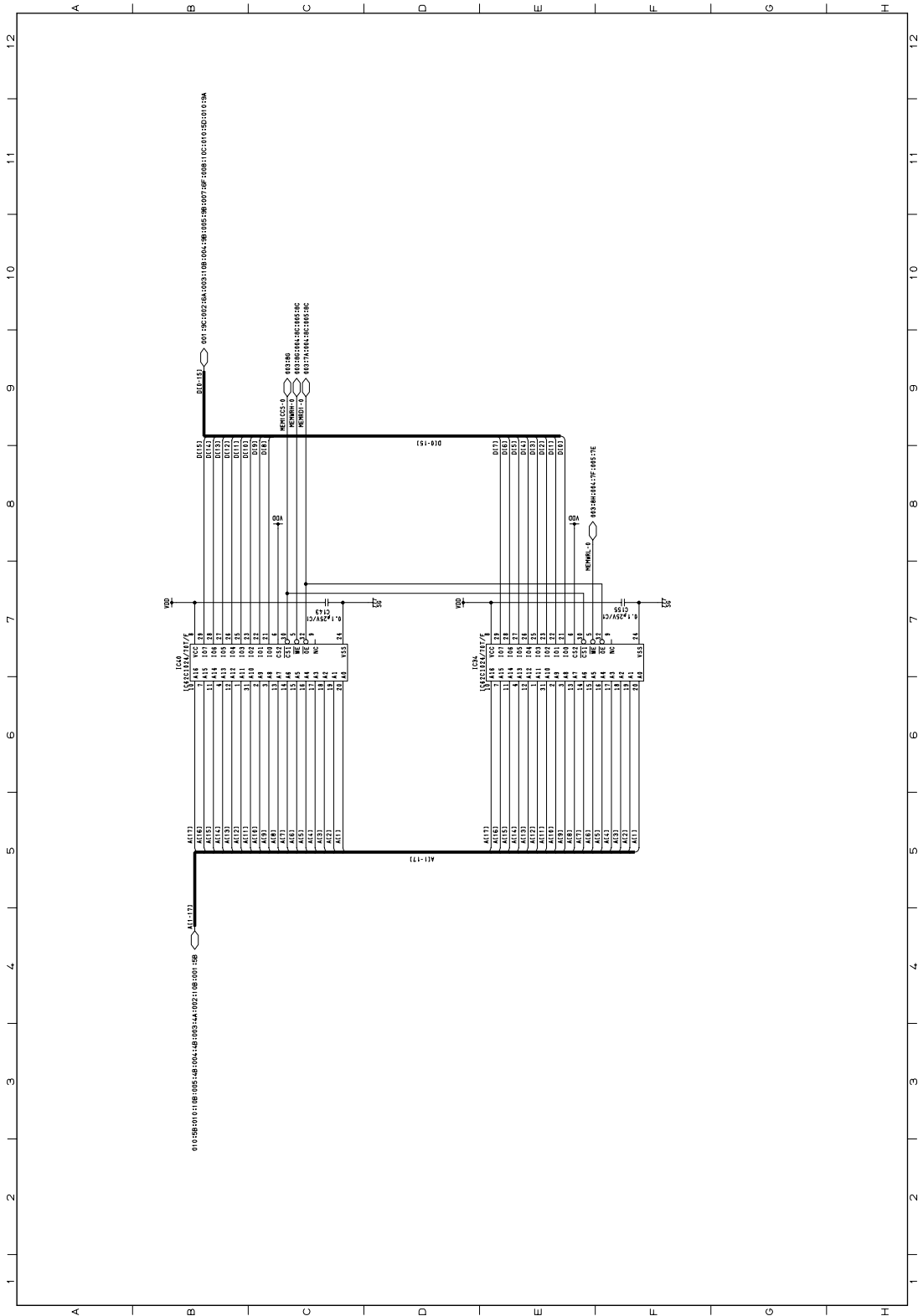


Fig. 3-67

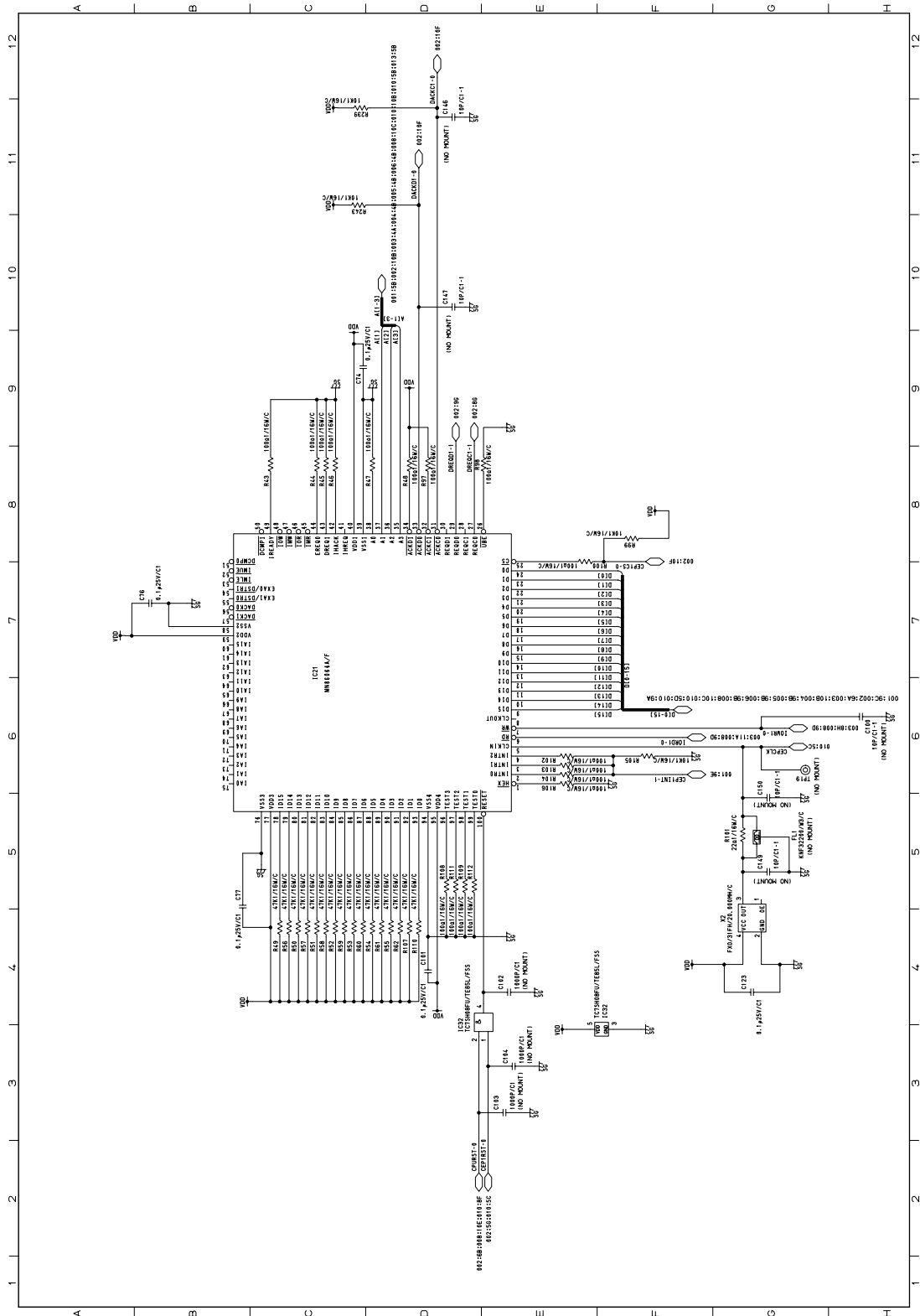


Fig. 3-68



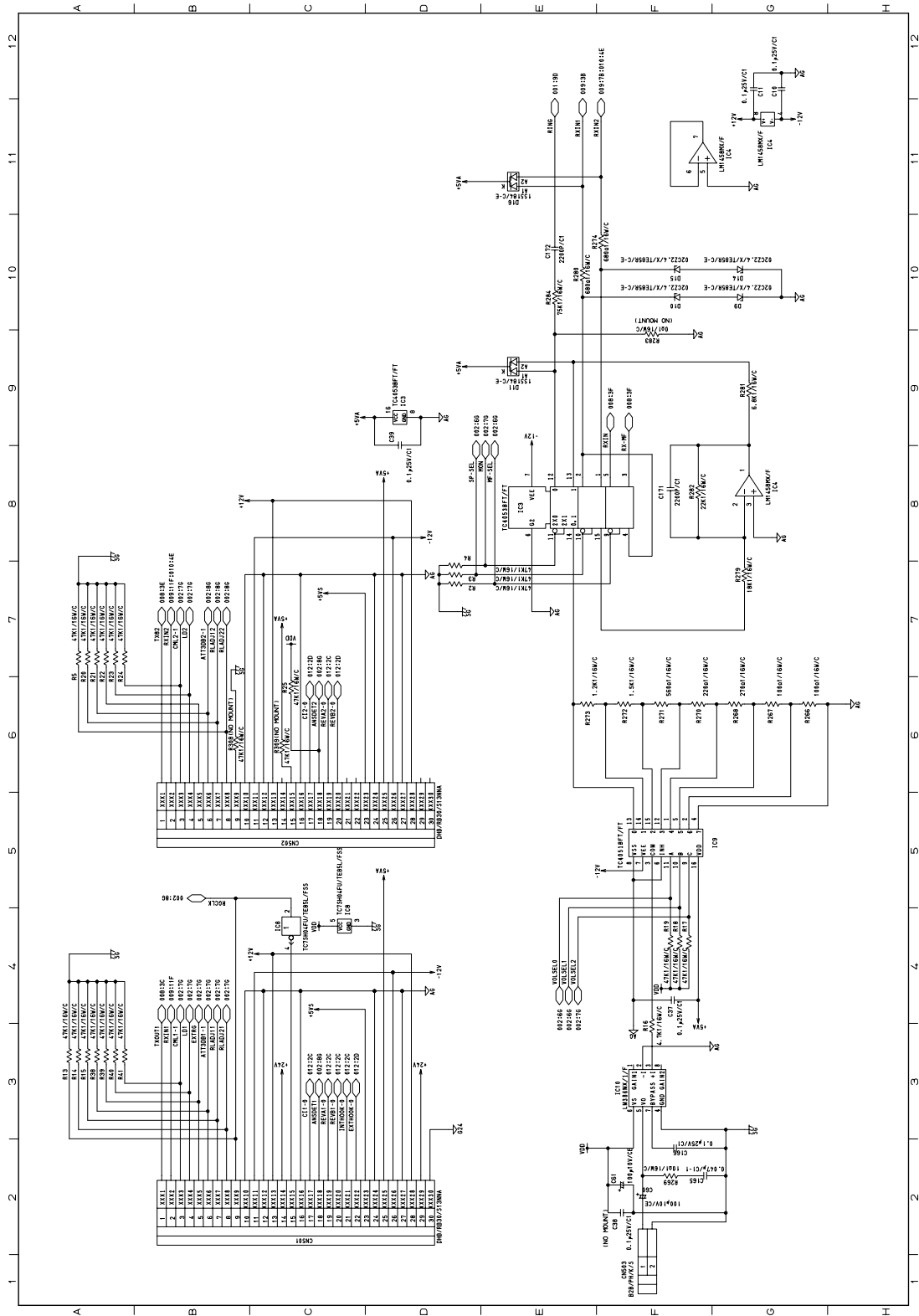


Fig. 3-70



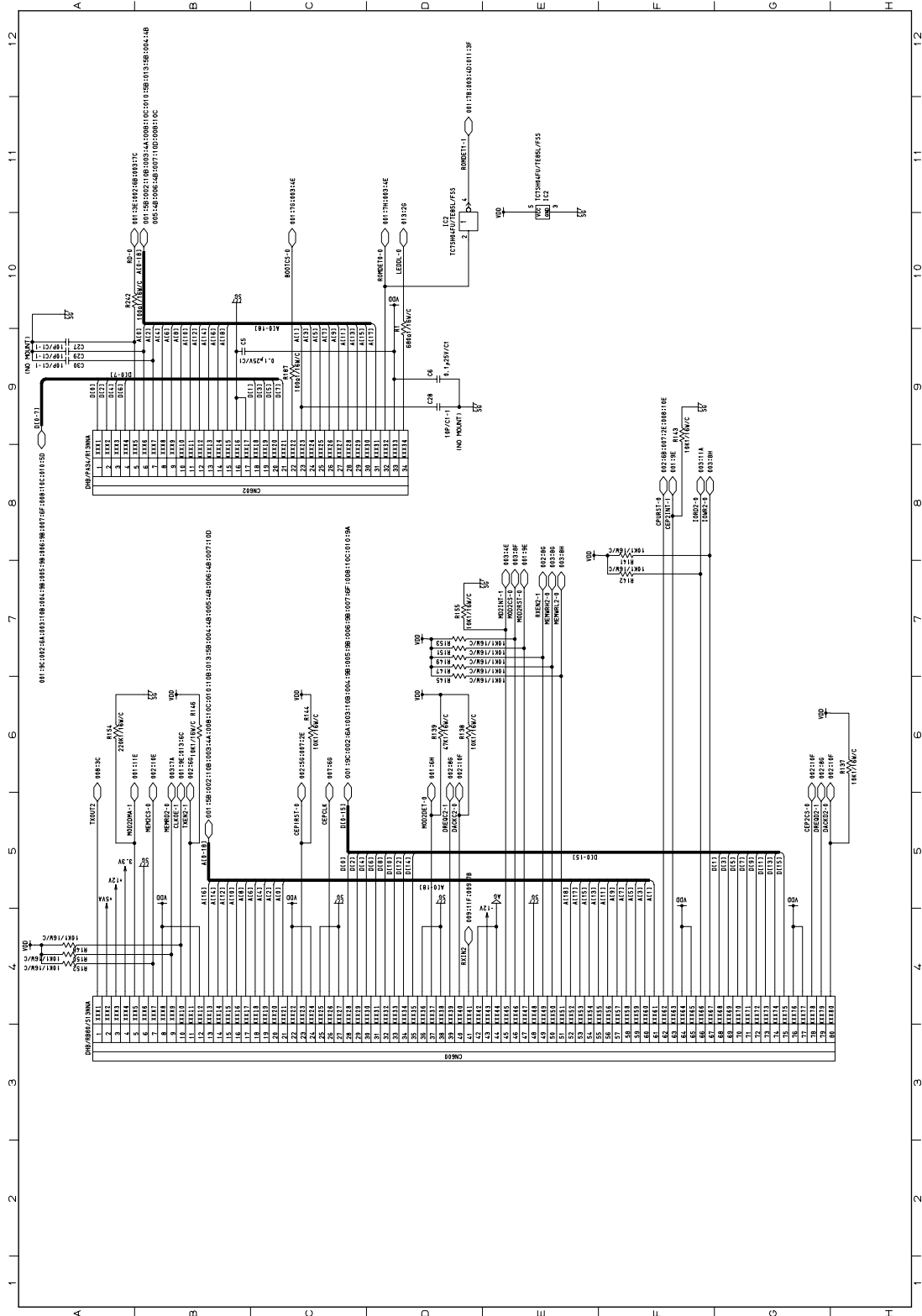


Fig. 3-71

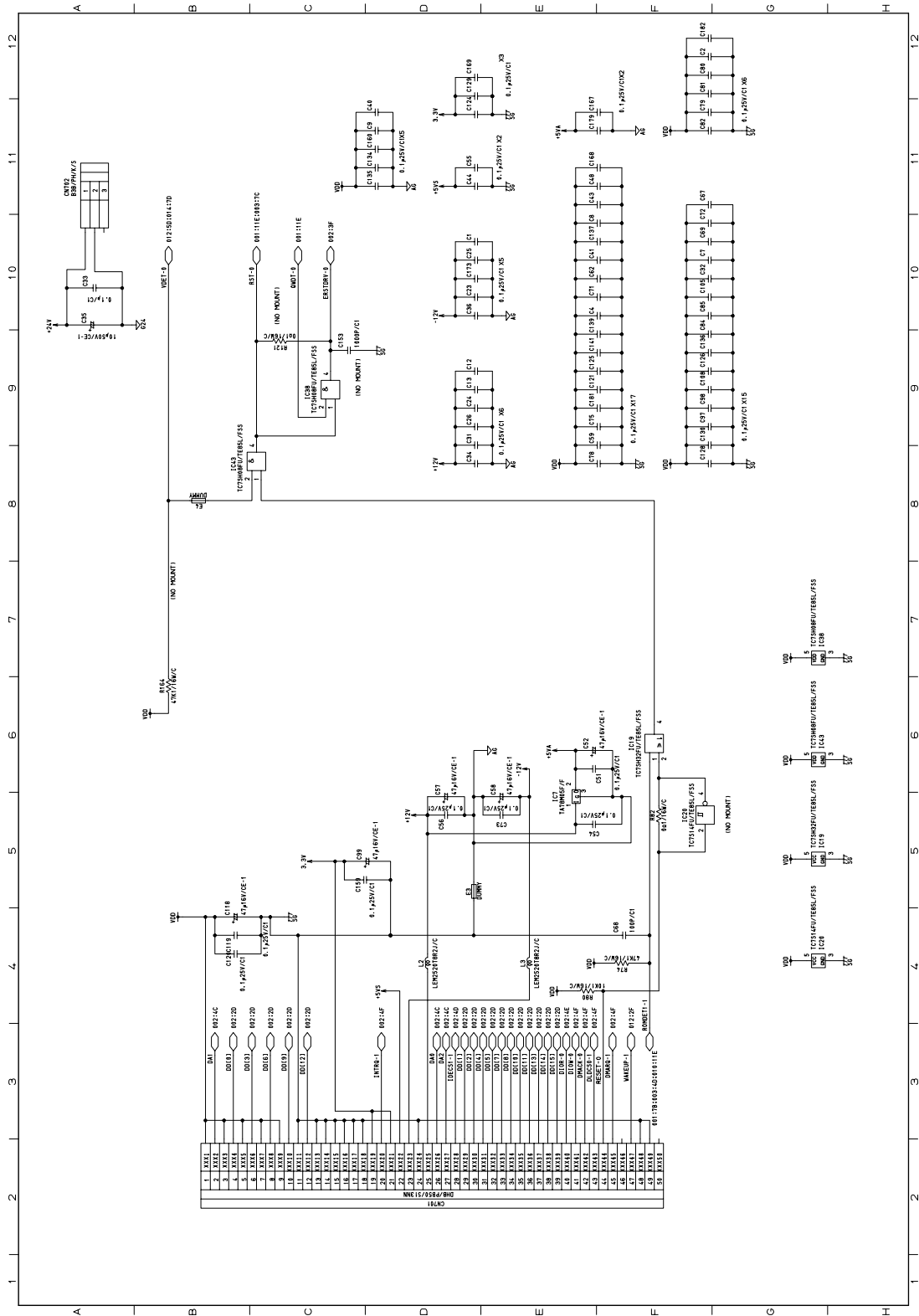


Fig. 3-72



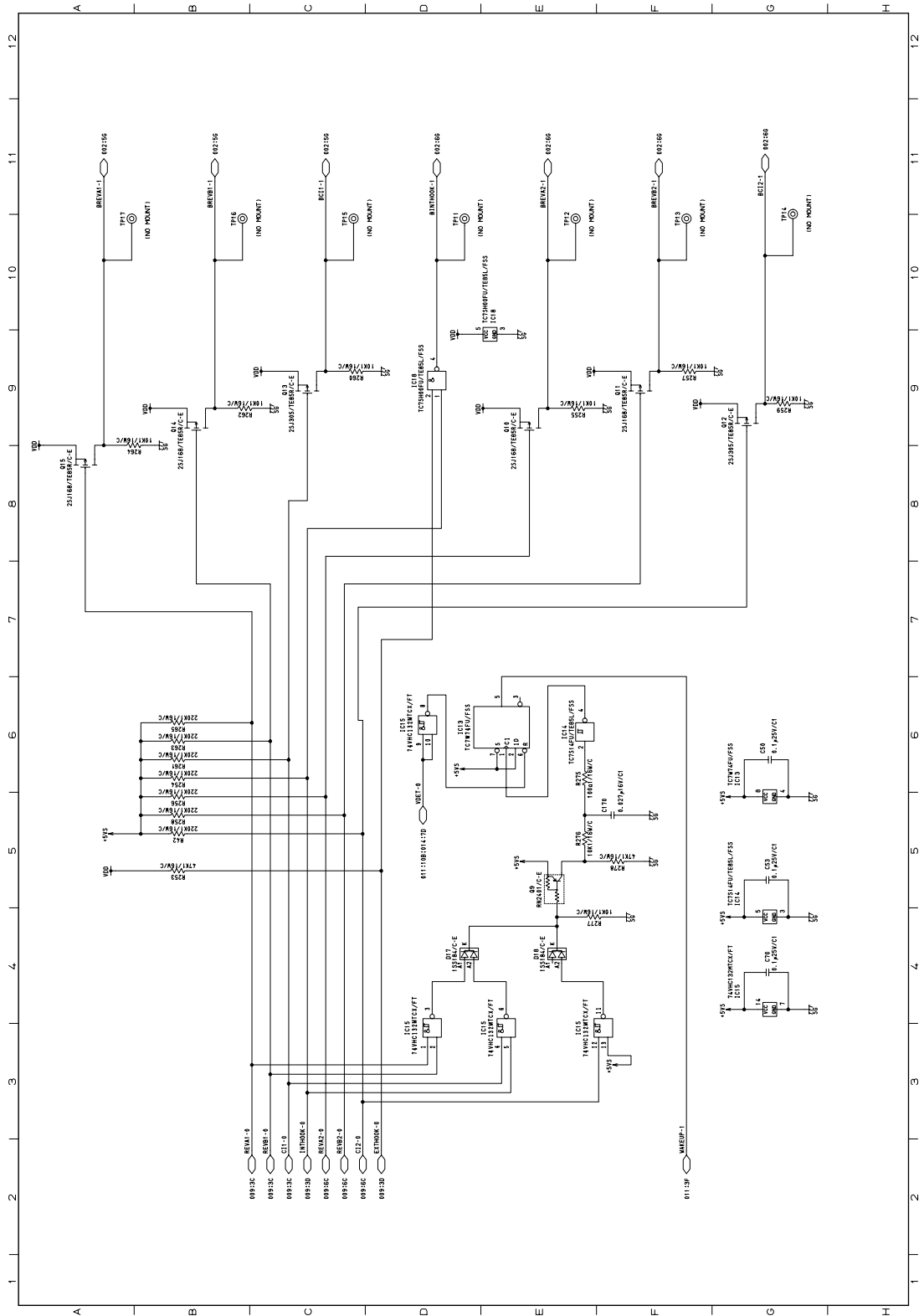


Fig. 3-73

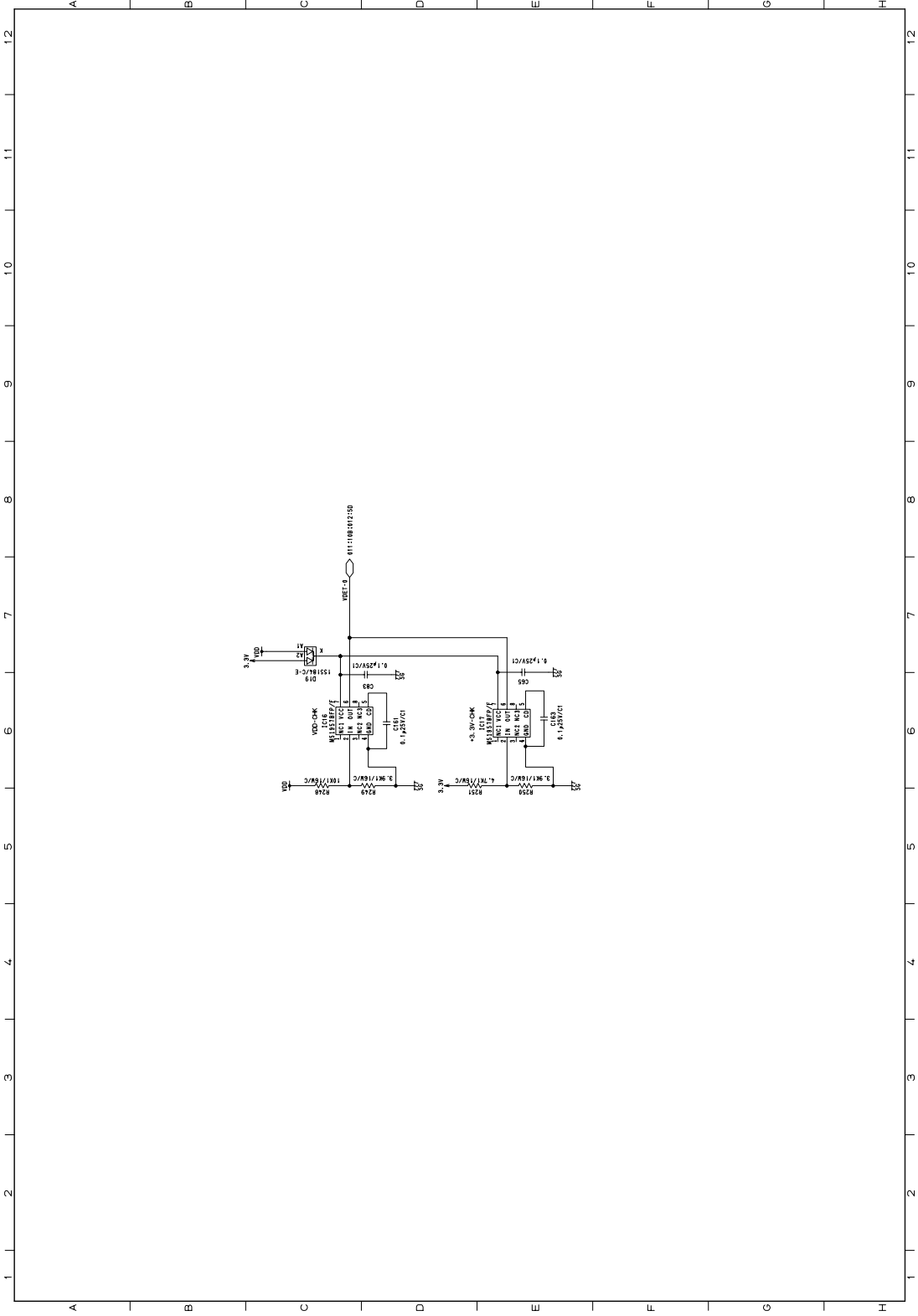


Fig. 3-75

3.13 Modem circuit (MDM board: GD-1160)

MDM board 1/4

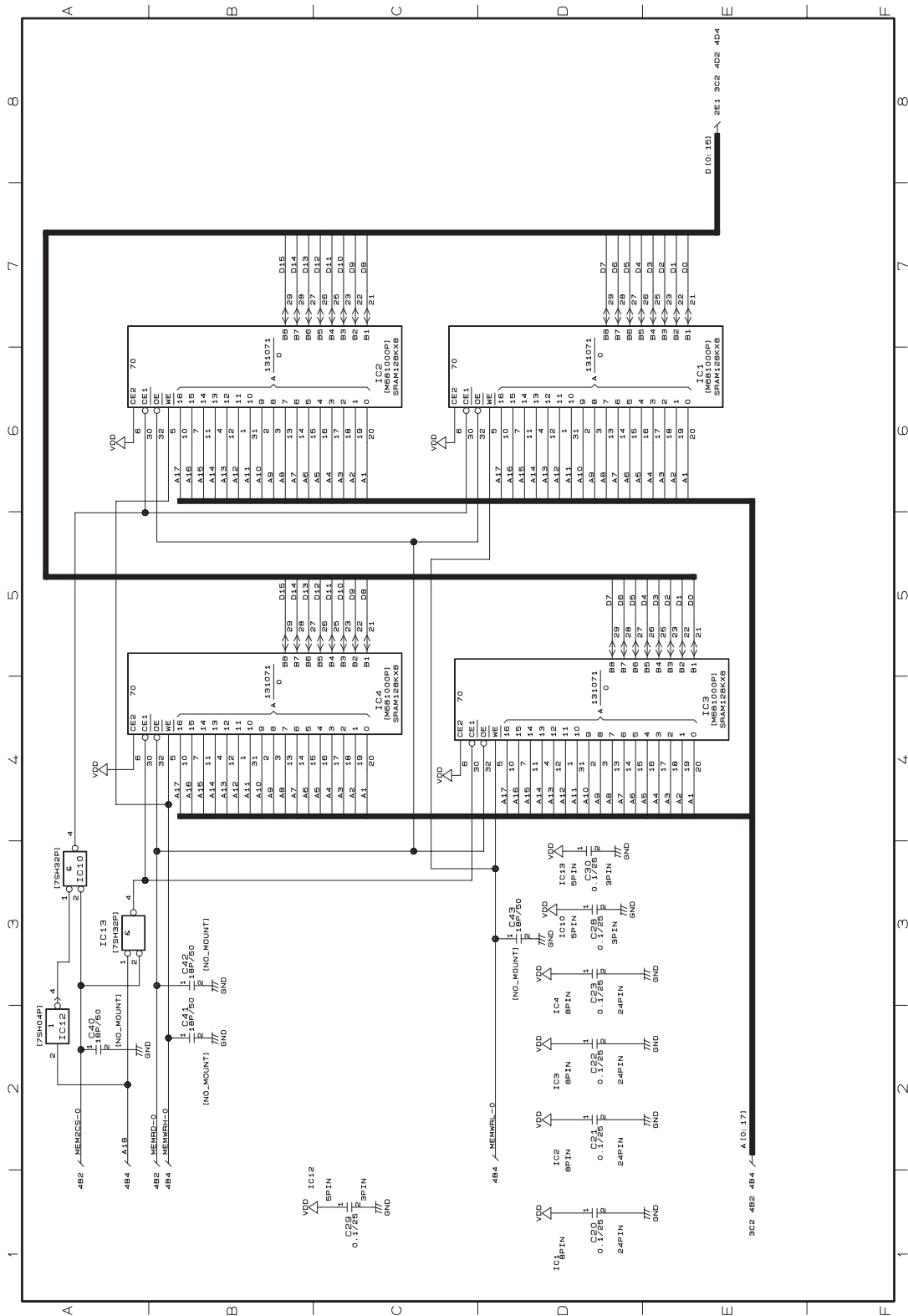


Fig. 3-76

MDM board 2/4

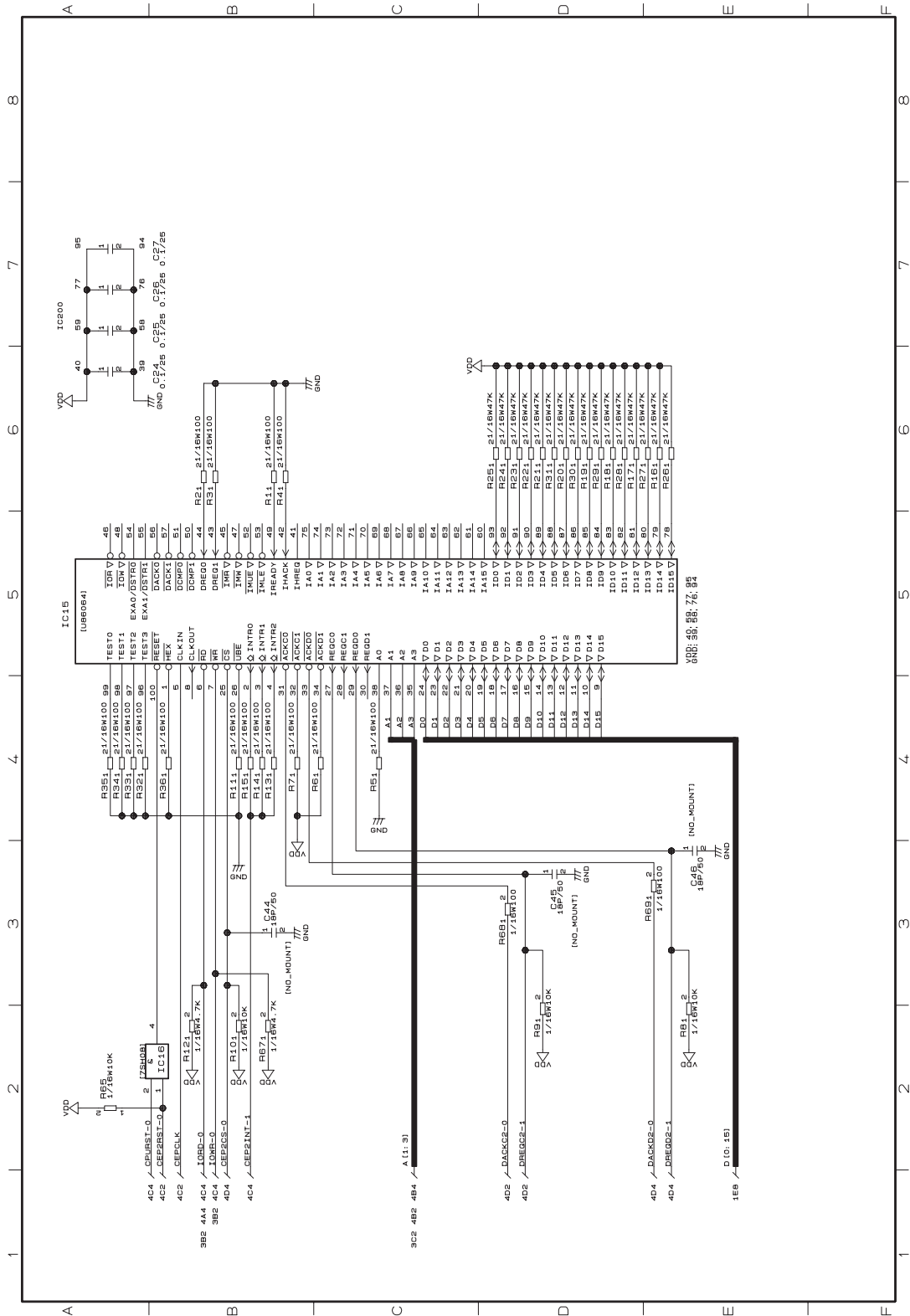


Fig. 3-77

MDM board 3/4

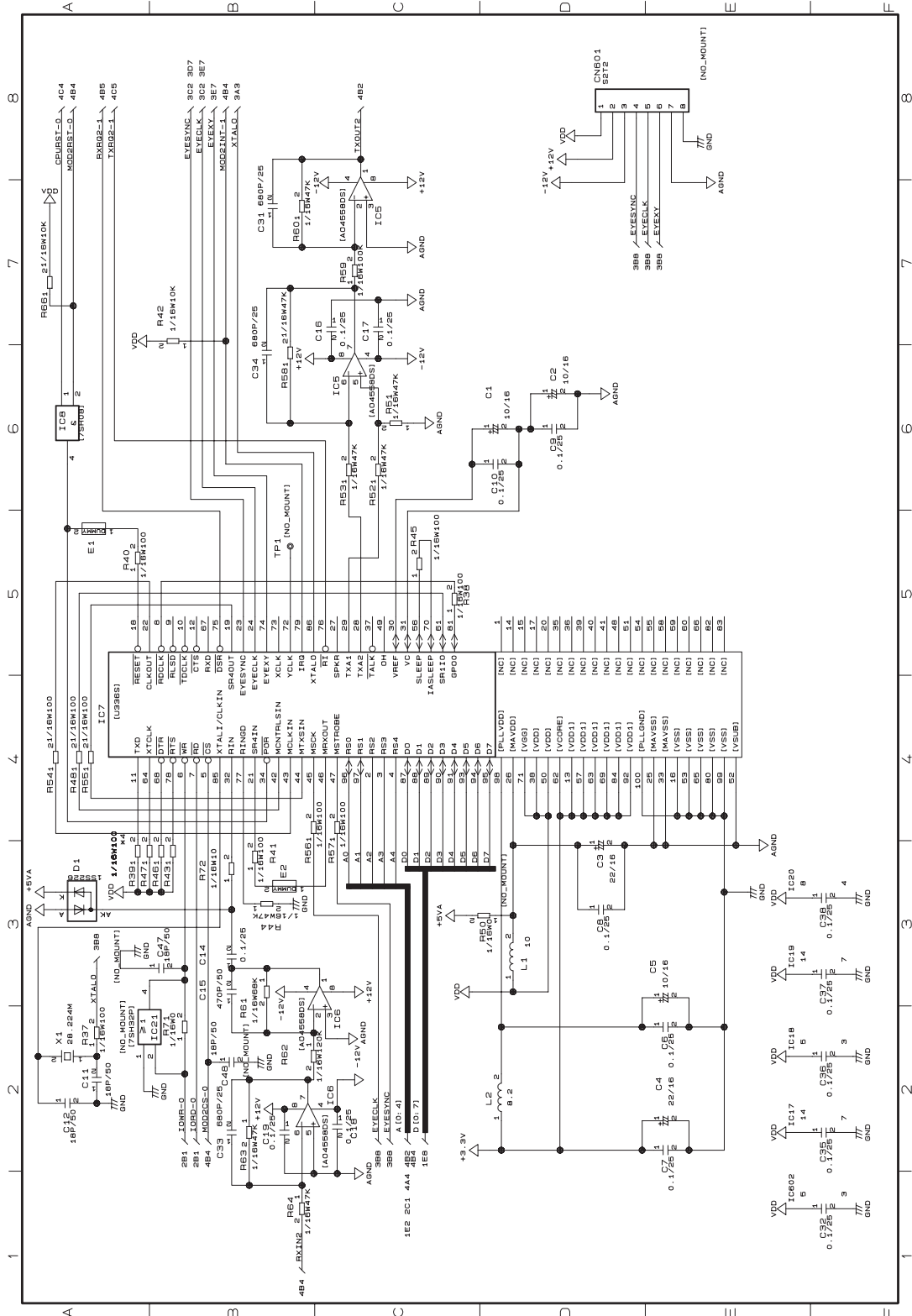


Fig. 3-78



MDM board 4/4

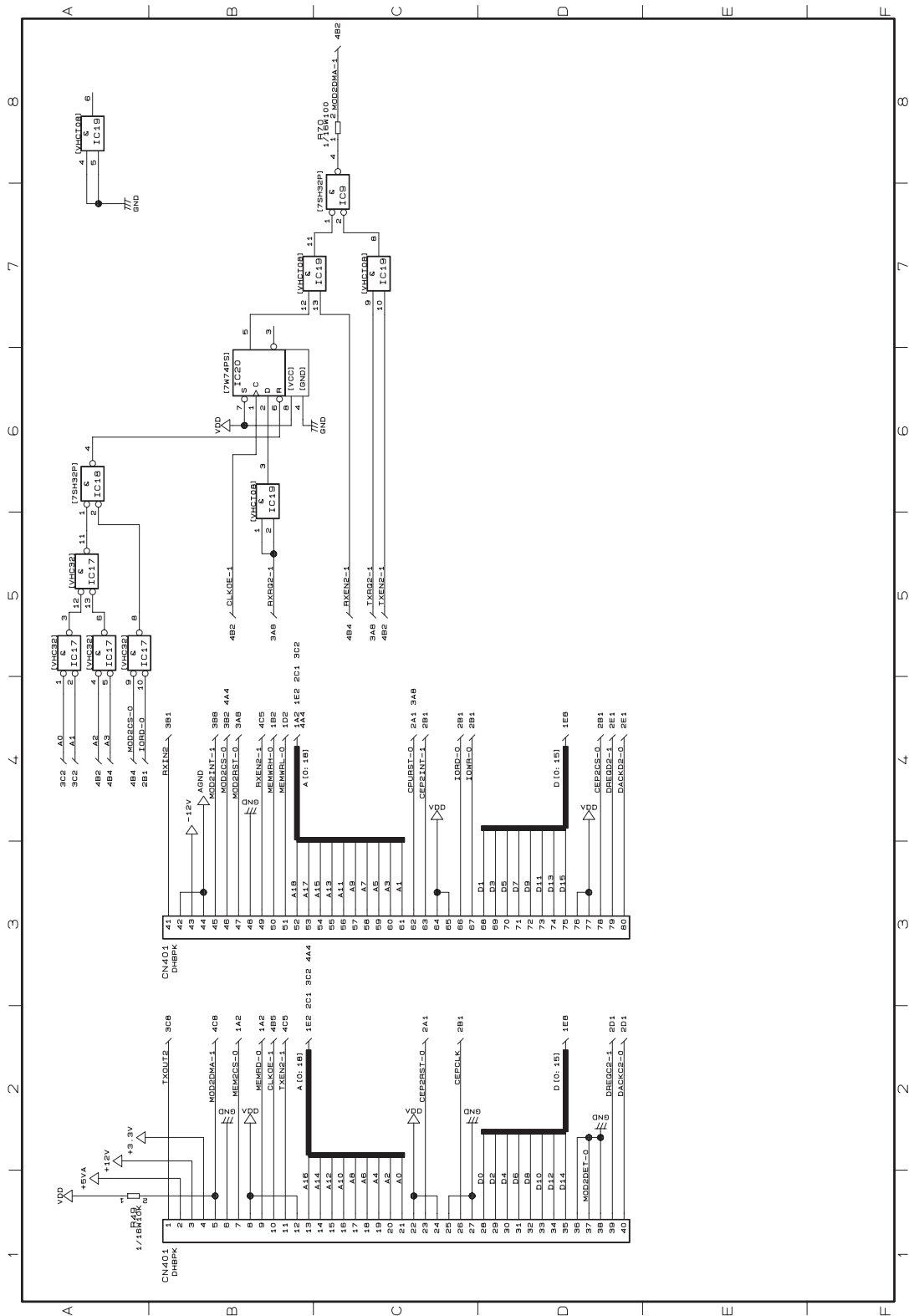


Fig. 3-79

3.14 Telephone line network control circuit (NCU board: GD-1150/1160) *Only for NA/TW model

NCU board 1/2

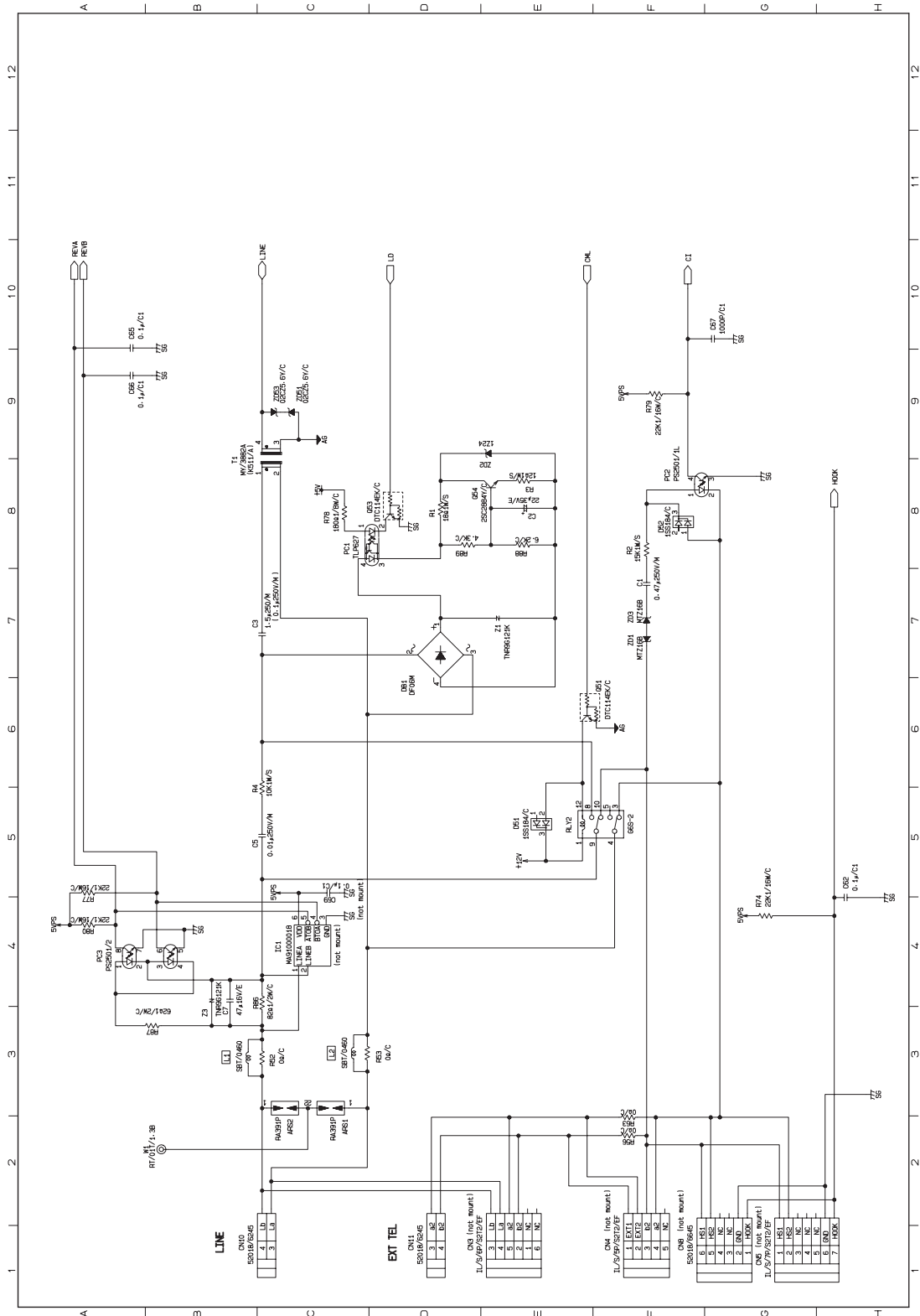


Fig. 3-80



NCU board 2/2 *Only for NA/TW models

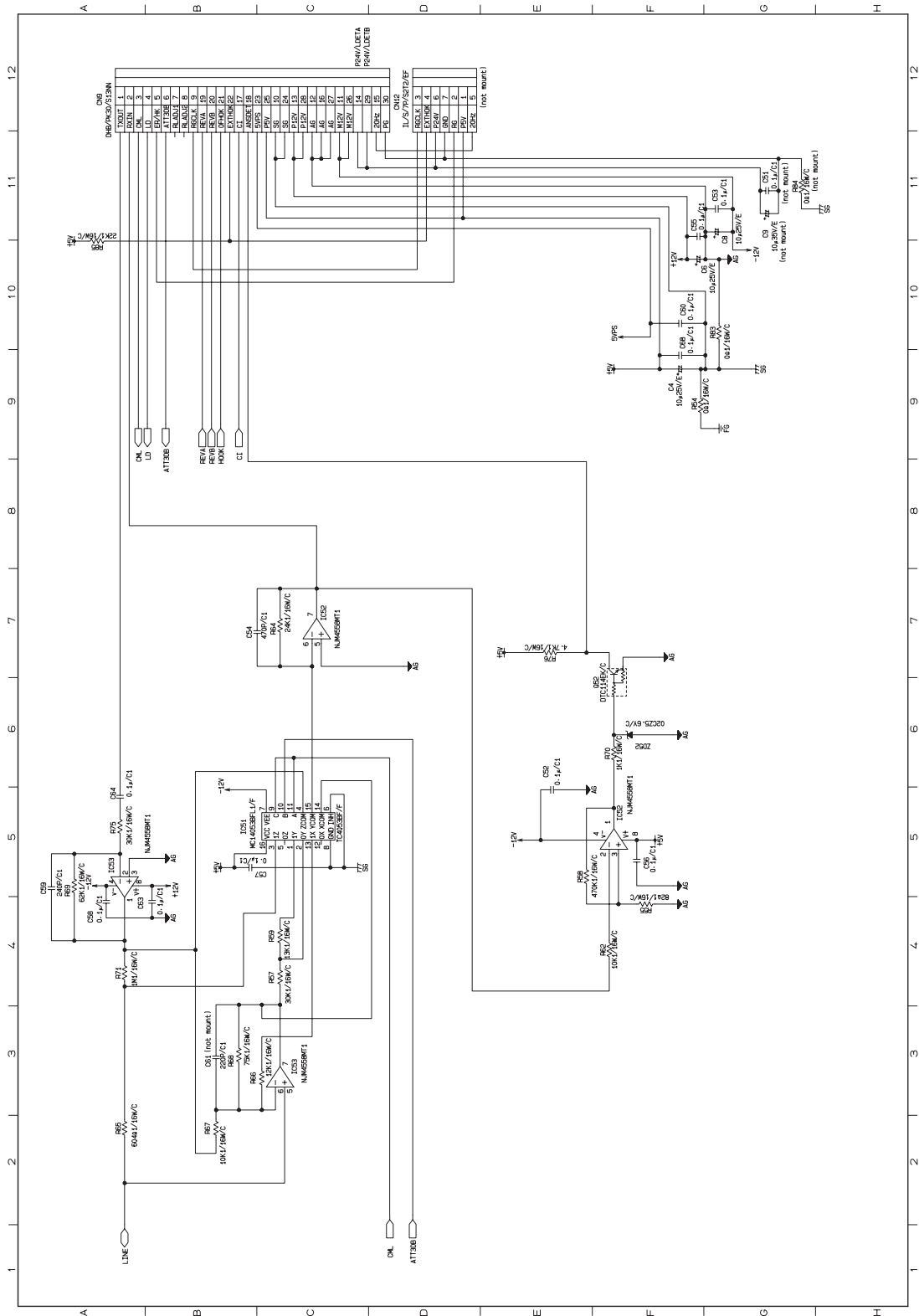


Fig. 3-81

3.15 Telephone line network control circuit (NCU board: GD-1150/1160) *Only for EU/AU/AS/C models

NCU board 1/2

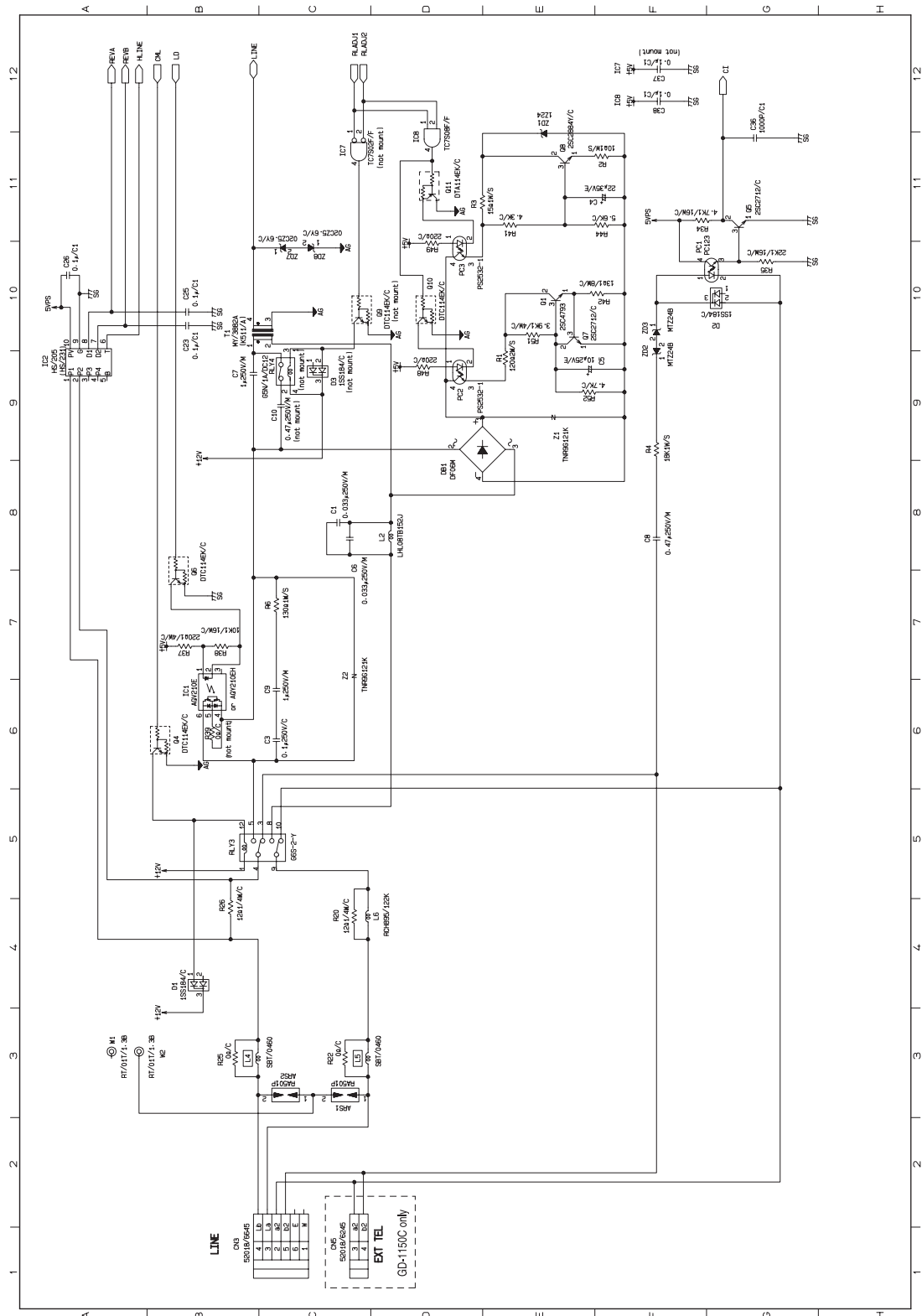


Fig. 3-82



NCU board 2/2 *Only for EU/AU/AS/C models

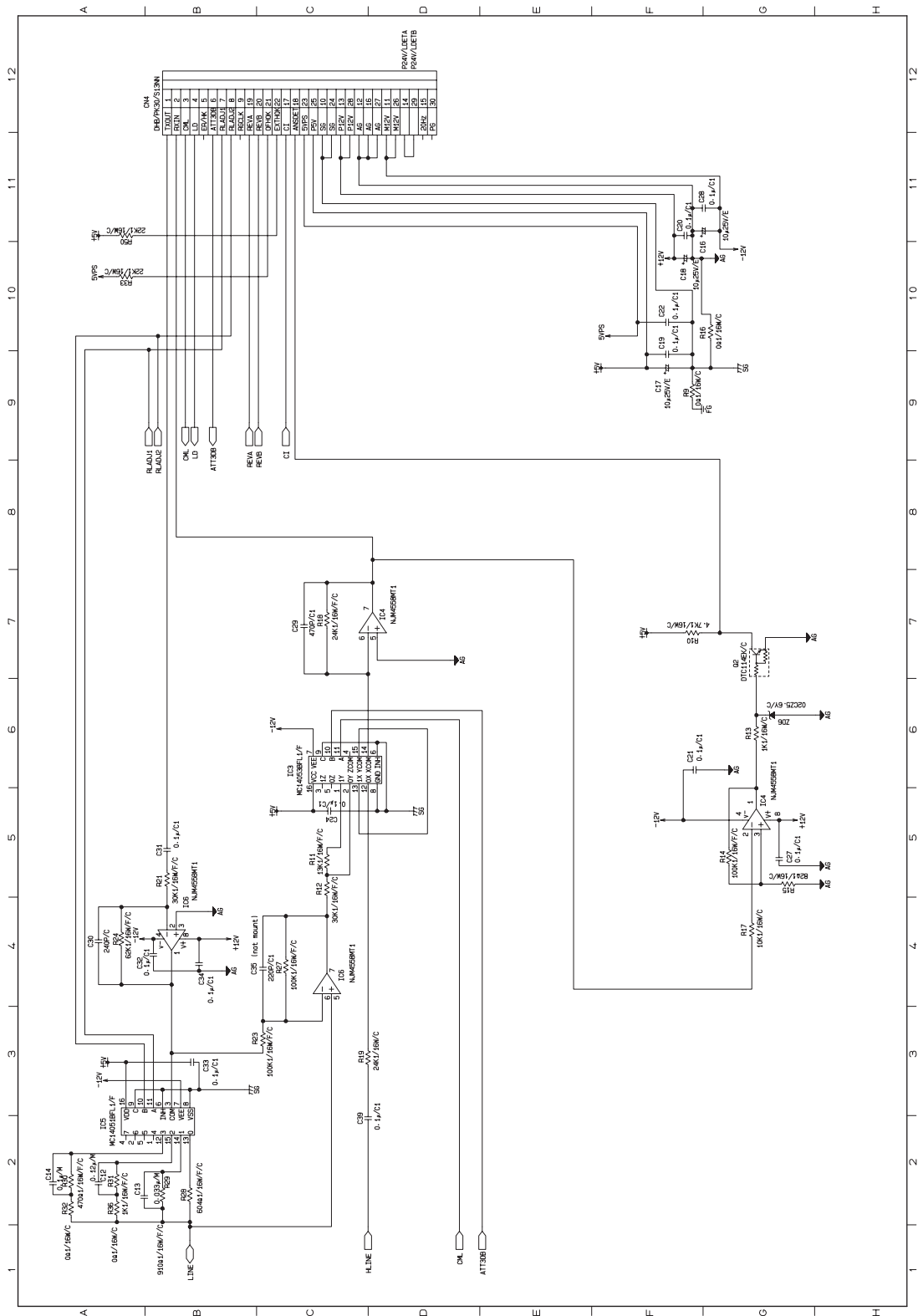


Fig. 3-83

TOSHIBA

TOSHIBA TEC CORPORATION

2-17-2, HIGASHIGOTANDA, SHINAGAWA-KU, TOKYO, 141-8664, JAPAN

WWW.SERVICE-MANUAL.NET