TOSHIBA

# PC BOARD REPAIR MANUAL

## MULTIFUNCTIONAL DIGITAL SYSTEMS

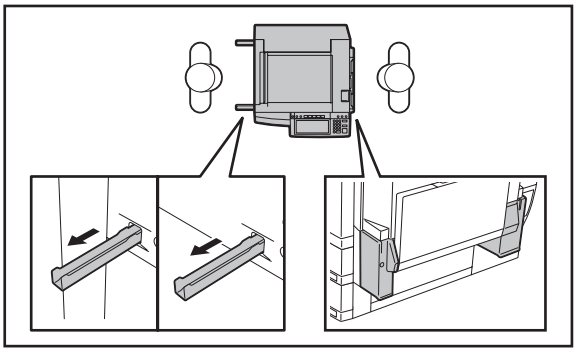
# e-STUDIO200L/230/280

File No. RME0400010A0
R04022143200-TTEC
Ver01_2004-09

# GENERAL PRECAUTIONS REGARDING THE SERVICE FOR e-STUDIO200L/230/280 SERIES

## The installation and service should be done by a qualified service technician.

1) **Transportation/Installation**
   - When transporting/installing the equipment, employ two persons and be sure to hold the positions as shown in the figure.
     The equipment is quite heavy and weighs approximately 75 kg (165.34 lb.) therefore pay full attention when handling it.



   - Be sure not to hold the movable parts or units (e.g. the control panel, ADU or RADF) when transporting the equipment.
   - Be sure to use a dedicated outlet with AC 110 V / 13.2 A, 115 V or 127 V / 12 A, 220-240 V or 240 V / 8 A for its power source.
   - The equipment must be grounded for safety.
   - Select a suitable place for installation. Avoid excessive heat, high humidity, dust, vibration and direct sunlight.
   - Provide proper ventilation since the equipment emits a slight amount of ozone.
   - To insure adequate working space for the copying operation, keep a minimum clearance of 80 cm (32”) on the left, 80 cm (32”) on the right and 10 cm (4”) on the rear.
   - The equipment shall be installed near the socket outlet and shall be accessible.

2) **General Precautions at Service**

- Be sure to turn the power OFF and unplug the power cable during service (except for the service should be done with the power turned ON).
- Unplug the power cable and clean the area around the prongs of the plug and socket outlet once a year or more. A fire may occur when dust lies on this area.
- When the parts are disassembled, reassembly is the reverse of disassembly unless otherwise noted in this manual or other related documents. Be careful not to install small parts such as screws, washers, pins, E-rings, star washers in the wrong places.
- Basically, the equipment should not be operated with any parts removed or disassembled.
- The PC board must be stored in an anti-electrostatic bag and handled carefully using a wristband since the ICs on it may be damaged due to static electricity.

  **Caution: Before using the wristband, unplug the power cable of the equipment and make sure that there are no charged objects which are not insulated in the vicinity.**

- Avoid expose to laser beam during service. This equipment uses a laser diode. Be sure not to expose your eyes to the laser beam. Do not insert reflecting parts or tools such as a screwdriver on the laser beam path. Remove all reflecting metals such as watches, rings, etc. before starting service.
- Be sure not to touch high-temperature sections such as the exposure lamp, fuser unit, damp heater and areas around them.
- Be sure not to touch high-voltage sections such as the chargers, developer, high-voltage transformer, exposure lamp control inverter, inverter for the LCD backlight and power supply unit. Especially, the board of these components should not be touched since the electric charge may remain in the capacitors, etc. on them even after the power is turned OFF.
- Make sure that the equipment will not operate before touching potentially dangerous places (e.g. rotating/operating sections such as gears, belts pulleys, fans and laser beam exit of the laser optical unit).
- Be careful when removing the covers since there might be the parts with very sharp edges underneath.
- When servicing the equipment with the power turned ON, be sure not to touch live sections and rotating/operating sections. Avoid exposing your eyes to laser beam.
- Use designated jigs and tools.
- Use recommended measuring instruments or equivalents.
- Return the equipment to the original state and check the operation when the service is finished.

3) **Important Service Parts for Safety**

- The breaker, door switch, fuse, thermostat, thermofuse, thermistor, IC-RAMs including lithium batteries, etc. are particularly important for safety. Be sure to handle/install them properly. If these parts are short-circuited and their functions become ineffective, they may result in fatal accidents such as burnout. Do not allow a short-circuit or do not use the parts not recommended by Toshiba TEC Corporation.

4) **Cautionary Labels**

- During servicing, be sure to check the rating plate and cautionary labels such as “Unplug the power cable during service”, “CAUTION. HOT”, “CAUTION. HIGH VOLTAGE”, “CAUTION. LASER BEAM”, etc. to see if there is any dirt on their surface and if they are properly stuck to the equipment.

5) **Disposal of the Equipment, Supplies, Packing Materials, Used Batteries and IC-RAMs**

- Regarding the recovery and disposal of the equipment, supplies, packing materials, used batteries and IC-RAMs including lithium batteries, follow the relevant local regulations or rules.

**Caution:**
Dispose of used batteries and IC-RAMs including lithium batteries according to this manual.
**Attention:**
Se débarrasser de batteries et IC-RAMs usés y compris les batteries en lithium selon ce manuel.
**Vorsicht:**
Entsorgung des gebrauchten Batterien und IC-RAMs (inclusive der Lithium-Batterie) nach diesem Handbuch.

# CONTENTS

# 1. SYSTEM BLOCK DIAGRAM

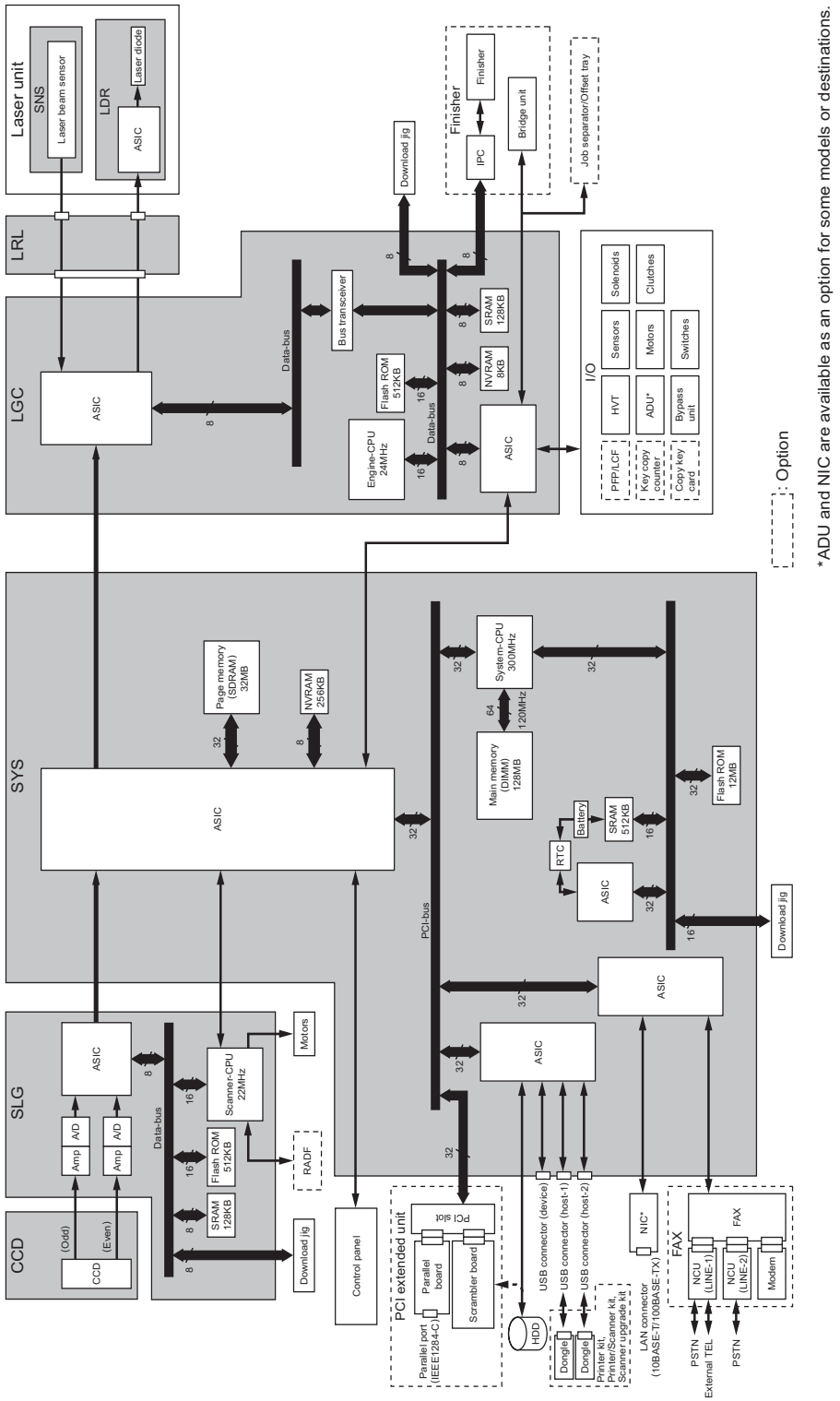



**Fig.1-1**

# 2. GENERAL DESCRIPTION OF MAIN IC

## 2.1 System CPU (TMPR4937)

### 2.1.1 Outline and features



The TMPR4937 is a standard microcontroller from Toshiba's 64-bit TX System RISC TX49 family, employing a TX49/H3 processor core that builds on MIPS III architecture of MIPS Technologies, Inc. In addition to TX49/H3 core, a set of peripheral circuits such as an external bus controller, a DMA controller, an SDRAM controller, a PCI controller, serial and parallel I/O ports, a timer/counter, and an AC-link controller are built-in for use in embedded applications of the microcontrollers. Especially, the SDRAM controller whose data bus width is maximum 64 bits and memory clock frequency is 133 MHz has realized a low memory access latency and a high memory bandwidth, and obtained better performance of this high-end CPU core.
The features of this device are as follows.

1) TX49/H3 core
   - Maximum operating frequency: 300 MHz
   - IEEE754-compliant single/double precision floating number point processing unit embedded
2) External bus controller (8 channels)
3) DMA (Direct Memory Access) controller (8 channels)
4) SDRAM controller (4 channels)
   - 64-bit data bus
   - Memory clock frequency 133 MHz
   - ECC/Parity support
   - Compliant with SyncFlash® memory
5) PCI controller
   - Compliant with PCI Local Bus Specification Revision 2.2
   - PCI bus clock frequency 66 MHz/33 MHz
6) Serial I/O port (2 channels)
7) Timer/counter (3 channels)
8) Parallel I/O port (Maximum 16 bits)
9) AC-link controller
10) Interrupt controller
11) Little-endian Mode or Big-endian Mode is selectable
12) Low power consumption
   - Internal logic section: 1.5 V, I/O section: 3.3 V operation, Supporting a low-power (Halt) mode
13) IEEE1149.1 (JTAG) support: Debugging support unit (Extended EJTAG)
14) Package: 484 pins, PBGA

## 2.1.2 Functions

The System CPU interfaces with the Engine CPU, Scanner CPU, HDD and control panel, and controls the whole system of the equipment such as each ASIC and memories (page memory and main memory) based on the command from the control panel. The System CPU also controls data communication with the external devices connected to the equipment (PC, FAX, etc.) through NIC board, FAX board, PCI expansion board and such.
These control programs of the System CPU are stored in the Flash ROM on the SYS board. These programs can be updated by downloading the new programs with the download jig, PC which is serially connected and so on. The adjustment/setting value related with the system control is stored in the removable NVRAM on the SYS board in order to prevent a data loss and simplify the data transfer process at the board replacement.

## 2.1.3 Pin assignment

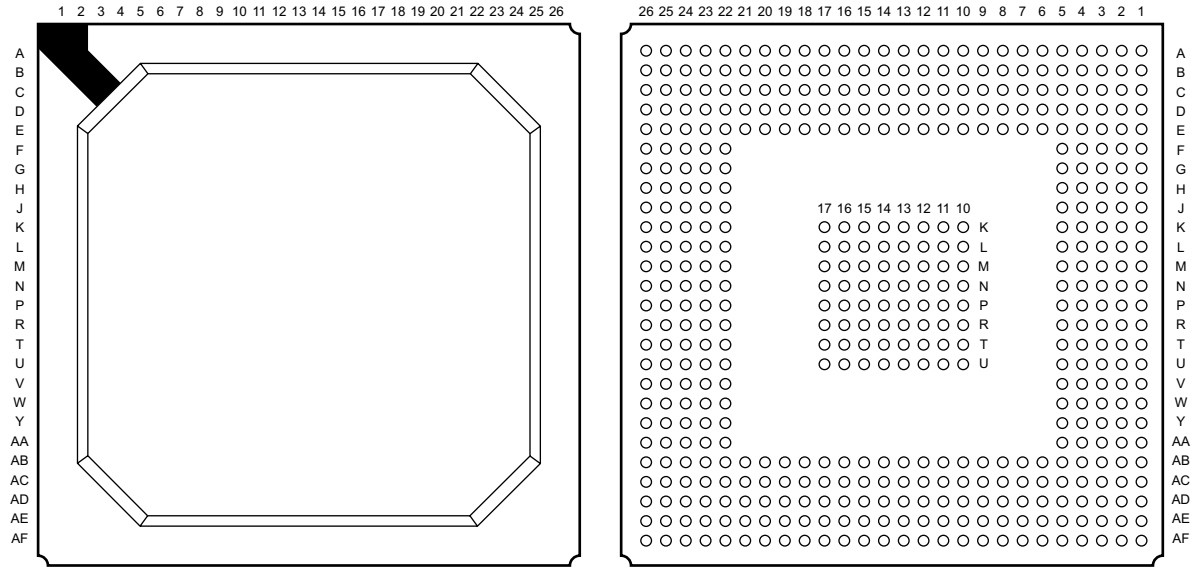



**Fig.2-1**

## 2.1.4 Signals

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| A01 | PIO1 | /LGCRST | O | LGC reset signal (Low-active) |
| A02 | PIO0 | /SFTRST | O | PCI reset signal (Low-active) |
| A03 | SWE | /WR | O | Write signal (Low-active) |
| A04 | CE7 | /CS[7] | O | Chip select signal [7] (Low-active)<br>* For Download jig |
| A05 | CE5 | /CS[5] | O | Chip select signal [5] (Low-active)<br>* For LED/DIP switch on SYS board |
| A06 | CE4 | /CS[4] | O | Chip select signal [4] (Low-active)<br>* For ASIC |
| A07 | DMAACK2 | DMAACK[2] | O | DMA acknowledge signal [2] |
| A08 | DMAACK1 | DMAACK[1] | O | DMA acknowledge signal [1] |
| A09 | BWE0 | /BWE[0] | O | Byte write enable signal [0] (Low-active) |
| A10 | BWE1 | /BWE[1] | O | Byte write enable signal [1] (Low-active) |
| A11 | EEPROM_DI | - | - | Not used (Open) |
| A12 | EEPROM_DO | - | - | Not used (Open) |
| A13 | VSS1 | SG | - | Signal ground |
| A14 | EEPROM_SK | - | - | Not used (Open) |
| A15 | EEPROM_CS | - | - | Not used (Open) |
| A16 | PCST3 | PCST[3] | O | PC trace status information [3] (for debug) |
| A17 | PCST01 | PCST[0] | O | PC trace status information [0] (for debug) |
| A18 | PCIAD2 | AD[2] | I/O | PCI address/data bus [2] |
| A19 | PCIAD5 | AD[5] | I/O | PCI address/data bus [5] |
| A20 | C_BE0 | /CBE[0] | I/O | PCI command/byte enable signal [0] |
| A21 | PCIAD11 | AD[11] | I/O | PCI address/data bus [11] |
| A22 | PCIAD15 | AD[15] | I/O | PCI address/data bus [15] |
| A23 | VSS2 | SG | - | Signal ground |
| A24 | VDDIO1 | +3.3V | - | +3.3V |
| A25 | IRDY | /IRDY | I/O | PCI initiator ready signal (Low-active) |
| A26 | C_BE2 | /CBE[2] | I/O | PCI command/byte enable signal [2] |
| B01 | PIO3 | /CPRST | O | Control panel reset signal (Low-active) |
| B02 | PIO2 | /SCNRST | O | Scanner reset signal (Low-active) |
| B03 | BUSSPRT | /BUSSPRT | O | Data bus separation control signal (Low-active) |
| B04 | CE6 | /CS[6] | O | Chip select signal [6] (Low-active)<br>* For Flash ROM (Boot) |
| B05 | VDDIO2 | +3.3V | - | +3.3V |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| B06 | CE3 | /CS[3] | O | Chip select signal [3] (Low-active)<br>* For SRAM |
| B07 | DMAACK3 | DMAACK[3] | O | DMA acknowledge signal [3] |
| B08 | DMAREQ2 | DMAREQ[2] | I | DMA request signal [2] |
| B09 | DMAREQ1 | DMAREQ[1] | I | DMA request signal [1] |
| B10 | BWE2 | /BWE[2] | O | Byte write enable signal [2] (Low-active) |
| B11 | TCK | TCK | I | JTAG test clock input (for debug) |
| B12 | DCLK | DCLK | O | Debug clock output (for debug) |
| B13 | TD0 | TDO | O | JTAG test data output (for debug) |
| B14 | PCST8 | PCST[8] | O | PC trace status information [8] (for debug) |
| B15 | PCST5 | PCST[5] | O | PC trace status information [5] (for debug) |
| B16 | PCST2 | PCST[2] | O | PC trace status information [2] (for debug) |
| B17 | PCIAD0 | AD[0] | I/O | PCI address/data bus [0] |
| B18 | PCIAD3 | AD[3] | I/O | PCI address/data bus [3] |
| B19 | PCIAD6 | AD[6] | I/O | PCI address/data bus [6] |
| B20 | PCIAD8 | AD[8] | I/O | PCI address/data bus [8] |
| B21 | PCIAD12 | AD[12] | I/O | PCI address/data bus [12] |
| B22 | C_BE1 | /CBE[1] | I/O | PCI command/byte enable signal [1] |
| B23 | PERR | /PERR | I/O | PCI data parity error signal (Low-active) |
| B24 | STOP | /STOP | I/O | PCI stop signal (Low-signal) |
| B25 | FRAME | /FRAME | I/O | PCI cycle frame signal (Low-active) |
| B26 | VSS3 | SG | - | Signal ground |
| C01 | PIO5 | /FXRST | O | FAX reset signal (Low-active) |
| C02 | PIO4 | - | - | Not used (Pull-up: +3.3V) |
| C03 | VDDIO3 | +3.3V | - | +3.3V |
| C04 | ACK | /ACK | I/O | Data acknowledge signal (Low-active) |
| C05 | ACE | /ACE | O | Address clock enable (Low-active) |
| C06 | CE2 | - | - | Not used (Open) |
| C07 | CE1 | /CS[1] | O | Chip select signal [1] (Low-active)<br>* For Flash ROM (Program) |
| C08 | DMAREQ3 | DMAREQ[3] | I | DMA request signal [3] |
| C09 | VDDIO4 | +3.3V | - | +3.3V |
| C10 | BWE3 | /BWE[3] | O | Byte write enable signal [3] (Low-active) |
| C11 | TDI | TDI | I | JTAG test data input (for debug) |
| C12 | TMS | TMS | I | JTAG test mode select input (for debug) |
| C13 | TPC3 | TPC[3] | O | PC trace output [3] (for debug) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| C14 | PCST7 | PCST[7] | O | PC trace status information [7] (for debug) |
| C15 | PCST4 | PCST[4] | O | PC trace status information [4] (for debug) |
| C16 | PCST1 | PCST[1] | O | PC trace status information [1] (for debug) |
| C17 | PCIAD1 | AD[1] | I/O | PCI address/data bus [1] |
| C18 | VDDIO5 | +3.3V | - | +3.3V |
| C19 | PCIAD7 | AD[7] | I/O | PCI address/data bus [7] |
| C20 | PCIAD9 | AD[9] | I/O | PCI address/data bus [9] |
| C21 | PCIAD13 | AD[13] | I/O | PCI address/data bus [13] |
| C22 | PAR | PAR | I/O | PCI parity signal |
| C23 | LOCK | /LOCK | I/O | PCI lock signal (Low-active) |
| C24 | DEVSEL | /DEVSEL | I/O | PCI device select signal (Low-active) |
| C25 | PCIAD17 | AD[17] | I/O | PCI address/data bus [17] |
| C26 | PCIAD16 | AD[16] | I/O | PCI address/data bus [16] |
| D01 | PIO7 | /EXSL | I | System/HDD download jig select signal (Low-active) |
| D02 | VSS4 | SG | - | Signal ground |
| D03 | PIO6 | /NICRST | O | NIC reset signal (Low-active) |
| D04 | VDDIN1 | +1.5VA | - | +1.5V |
| D05 | BYPASSPLL | - | - | Not used (Pull-up: +3.3V) |
| D06 | VSS5 | SG | - | Signal ground |
| D07 | CE0 | /CS[0] | O | Chip select signal [0] (Low-active)<br>* For Flash ROM (Boot) |
| D08 | VDDIN2 | +1.5VA | - | +1.5V |
| D09 | VSS6 | SG | - | Signal ground |
| D10 | VDDIN3 | +1.5VA | - | +1.5V |
| D11 | DMAACK0 | DMAACK[0] | O | DMA acknowledge signal [0] |
| D12 | VDDIO6 | +3.3V | - | +3.3V |
| D13 | TPC2 | TPC[2] | O | PC trace output [2] (for debug) |
| D14 | VDDIO7 | +3.3V | - | +3.3V |
| D15 | VDDIN4 | +1.5VA | - | +1.5V |
| D16 | VDDIO8 | +3.3V | - | +3.3V |
| D17 | VDDIN5 | +1.5VA | - | +1.5V |
| D18 | PCIAD4 | AD[4] | I/O | PCI address/data bus [4] |
| D19 | VDDIO9 | +3.3V | - | +3.3V |
| D20 | M66EN | /M66EN | I/O | PCI bus 66MHz clock enable signal |
| D21 | VDDIO10 | +3.3V | - | +3.3V |
| D22 | SERR | /SERR | I/O | PCI system error signal (Low-active) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| D23 | VDDIN6 | +1.5VA | - | +1.5V |
| D24 | TRDY | /TRDY | I/O | PCI target ready signal (Low-active) |
| D25 | VDDIO11 | +3.3V | - | +3.3V |
| D26 | PCIAD18 | AD[18] | I/O | PCI address/data bus [18] |
| E01 | TCLK | - | - | Not used (Open) |
| E02 | TIMER0 | - | - | Not used (Open) |
| E03 | TIMER1 | - | - | Not used (Open) |
| E04 | VDDIO12 | +3.3V | - | +3.3V |
| E05 | VSS7 | SG | - | Signal ground |
| E06 | SD[1] | - | - | Not used (Pull-up: +3.3V) |
| E07 | VDDIO13 | +3.3V | - | +3.3V |
| E08 | VSS8 | SG | - | Signal ground |
| E09 | DMADONE | /DMADONE | I/O | DMA done signal (Pull-up: +3.3V) |
| E10 | VSS9 | SG | - | Signal ground |
| E11 | DMAREQ0 | DMAREQ[0] | I | DMA request signal [0] |
| E12 | VSS10 | SG | - | Signal ground |
| E13 | TPC1 | TPC[1] | O | PC trace output [1] (for debug) |
| E14 | PCST6 | PCST[6] | O | PC trace status information [6] (for debug) |
| E15 | VSS11 | SG | - | Signal ground |
| E16 | TRST | /TRST | I | Test reset input (for debug) |
| E17 | VSS12 | SG | - | Signal ground |
| E18 | VSS13 | SG | - | Signal ground |
| E19 | VSS14 | SG | - | Signal ground |
| E20 | PCIAD10 | AD[10] | I/O | PCI address/data bus [10] |
| E21 | PCIAD14 | AD[14] | I/O | PCI address/data bus [14] |
| E22 | VSS15 | SG | - | Signal ground |
| E23 | PCIAD22 | AD[22] | I/O | PCI address/data bus [22] |
| E24 | PCIAD21 | AD[21] | I/O | PCI address/data bus [21] |
| E25 | PCIAD20 | AD[20] | I/O | PCI address/data bus [20] |
| E26 | PCIAD19 | AD[19] | I/O | PCI address/data bus [19] |
| F01 | INT2 | /GKINTA | I | ASIC interrupt request signal (Low-active) |
| F02 | INT1 | /DNICINT | I | PCI/ASIC interrupt request signal (Low-active) |
| F03 | INT0 | /PWRDN | I | Power down signal (Low-active) |
| F04 | NMI | /NMI | I | Non-maskable Interrupt signal (Pull-up: +3.3V) |
| F05 | VDDIN7 | +1.5VA | - | +1.5V |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| F22 | VDDIO14 | +3.3V | - | +3.3V |
| F23 | C_BE3 | /CBE[3] | I/O | PCI command/byte enable signal [3] |
| F24 | ID_SEL | ID_SEL | I | Initialization device select signal (Pull-down: signal ground) |
| F25 | VDDIO15 | +3.3V | - | +3.3V |
| F26 | PCIAD23 | AD[23] | I/O | PCI address/data bus [23] |
| G01 | INT5 | /INTS | I | ASIC interrupt request signal (Low-active) |
| G02 | INT4 | /INTP | I | ASIC interrupt request signal (Low-active) |
| G03 | INT3 | /PCIINT | I | PCI interrupt request signal [0] (Low-active) |
| G04 | RXD0 | RXD[0] | I | Serial I/O interface receive data |
| G05 | VDDIN8 | +1.5VA | - | +1.5V |
| G22 | PCIAD28 | AD[28] | I/O | PCI address/data bus [28] |
| G23 | PCIAD27 | AD[27] | I/O | PCI address/data bus [27] |
| G24 | PCIAD26 | AD[26] | I/O | PCI address/data bus [26] |
| G25 | PCIAD25 | AD[25] | I/O | PCI address/data bus [25] |
| G26 | PCIAD24 | AD[24] | I/O | PCI address/data bus [24] |
| H01 | TXD0 | TXD[0] | O | Serial I/O interface transmit data |
| H02 | RTS0 | - | - | Not used (Open) |
| H03 | CTS0 | - | - | Not used (Open) |
| H04 | VDDIO16 | +3.3V | - | +3.3V |
| H05 | VSS16 | SG | - | Signal ground |
| H22 | VSS17 | SG | - | Signal ground |
| H23 | VDDIN9 | +1.5VA | - | +1.5V |
| H24 | PCIAD29 | AD[29] | I/O | PCI address/data bus [29] |
| H25 | VDDIO17 | +3.3V | - | +3.3V |
| H26 | PCICLK0 | PCICLK[0] | O | PCI bus clock [0] |
| J01 | SCLK | - | - | Not used (Open) |
| J02 | TXD1 | - | - | Not used (Open) |
| J03 | RTS1 | - | - | Not used (Open) |
| J04 | CTS1 | - | - | Not used (Open) |
| J05 | RXD1 | - | - | Not used (Open) |
| J22 | PCIAD31 | AD[31] | I/O | PCI address/data bus [31] |
| J23 | VSS18 | SG | - | Signal ground |
| J24 | PCIAD30 | AD[30] | I/O | PCI address/data bus [30] |
| J25 | GNT0 | /GNT[0] | O | PCI bus grant signal [0] (Low-active) |
| J26 | PCICLK1 | PCICLK[1] | O | PCI bus clock [1] |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| K01 | RESET | /RESET | I | Reset input (Low-active) |
| K02 | TEST0 | - | - | Not used (Open) |
| K03 | HALTDONE | - | - | Not used (Open) |
| K04 | VDDIN10 | +1.5VA | - | +1.5V |
| K05 | VSS19 | SG | - | Signal ground |
| K10 | SB1 | SG | - | Signal ground |
| K11 | SB2 | SG | - | Signal ground |
| K12 | SB3 | SG | - | Signal ground |
| K13 | SB4 | SG | - | Signal ground |
| K14 | SB5 | SG | - | Signal ground |
| K15 | SB6 | SG | - | Signal ground |
| K16 | SB7 | SG | - | Signal ground |
| K17 | SB8 | SG | - | Signal ground |
| K22 | VSS20 | SG | - | Signal ground |
| K23 | VDDIN11 | +1.5VA | - | +1.5V |
| K24 | GNT1 | /GNT[1] | O | PCI bus grant signal [1] (Low-active) |
| K25 | REQ0 | /REQ[0] | I | PCI bus request signal [0] (Low-active) |
| K26 | PCICLK2 | PCICLK[5] | O | PCI bus clock [5] |
| L01 | SYSCLK | SYSCLK | O | System clock output |
| L02 | TEST4 | - | - | Not used (Open) |
| L03 | TEST3 | - | - | Not used (Open) |
| L04 | TEST2 | - | - | Not used (Open) |
| L05 | TEST1 | - | - | Not used (Pull-down: signal ground) |
| L10 | SB9 | SG | - | Signal ground |
| L11 | SB10 | SG | - | Signal ground |
| L12 | SB11 | SG | - | Signal ground |
| L13 | SB12 | SG | - | Signal ground |
| L14 | SB13 | SG | - | Signal ground |
| L15 | SB14 | SG | - | Signal ground |
| L16 | SB15 | SG | - | Signal ground |
| L17 | SB16 | SG | - | Signal ground |
| L22 | REQ1 | /REQ[1] | I | PCI bus request signal [1] (Low-active) |
| L23 | VSS21 | SG | - | Signal ground |
| L24 | REQ2 | /REQ[2] | I | PCI bus request signal [2] (Low-active) |
| L25 | GNT2 | /GNT[2] | O | PCI bus grant signal [2] (Low-active) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| L26 | PCICLK3 | PCICLK[2] | O | PCI bus clock [2] |
| M01 | OE | /RD | O | Read signal (Low-active) |
| M02 | WDRST | /WDRST | O | Watchdog reset signal (Low-active) |
| M03 | VDDIO18 | +3.3V | - | +3.3V |
| M04 | VDDIN12 | +1.5VA | - | +1.5V |
| M05 | VSS22 | SG | - | Signal ground |
| M10 | SB17 | SG | - | Signal ground |
| M11 | SB18 | SG | - | Signal ground |
| M12 | SB19 | SG | - | Signal ground |
| M13 | SB20 | SG | - | Signal ground |
| M14 | SB21 | SG | - | Signal ground |
| M15 | SB22 | SG | - | Signal ground |
| M16 | SB23 | SG | - | Signal ground |
| M17 | SB24 | SG | - | Signal ground |
| M22 | VSS23 | SG | - | Signal ground |
| M23 | VDDIO19 | +3.3V | - | +3.3V |
| M24 | REQ3 | /REQ[3] | I | PCI bus request signal [3] (Low-active) |
| M25 | GNT3 | /GNT[3] | O | PCI bus grant signal [3] (Low-active) |
| M26 | PCICLK4 | PCICLK[3] | O | PCI bus clock [3] |
| N01 | DATA1 | DATA[1] | I/O | System data bus [1] |
| N02 | DATA32 | DATA[32] | I/O | System data bus [32] |
| N03 | DATA0 | DATA[0] | I/O | System data bus [0] |
| N04 | VSS24 | SG | - | Signal ground |
| N05 | VDDIO20 | +3.3V | - | +3.3V |
| N10 | SB25 | SG | - | Signal ground |
| N11 | SB26 | SG | - | Signal ground |
| N12 | SB27 | SG | - | Signal ground |
| N13 | SB28 | SG | - | Signal ground |
| N14 | SB29 | SG | - | Signal ground |
| N15 | SB30 | SG | - | Signal ground |
| N16 | SB31 | SG | - | Signal ground |
| N17 | SB32 | SG | - | Signal ground |
| N22 | PME | /PME | I | PCI power management event signal (Low-active) |
| N23 | VDDIO21 | +3.3V | - | +3.3V |
| N24 | VSS25 | SG | - | Signal ground |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| N25 | DATA63 | DATA[63] | I/O | System data bus [63] |
| N26 | PCICLK5 | PCICLK[4] | O | PCI bus clock [4] |
| P01 | DATA2 | DATA[2] | I/O | System data bus [2] |
| P02 | VSS26 | SG | - | Signal ground |
| P03 | DATA33 | DATA[33] | I/O | System data bus [33] |
| P04 | VSS27 | SG | - | Signal ground |
| P05 | VDDIO22 | +3.3V | - | +3.3V |
| P10 | SB33 | SG | - | Signal ground |
| P11 | SB34 | SG | - | Signal ground |
| P12 | SB35 | SG | - | Signal ground |
| P13 | SB36 | SG | - | Signal ground |
| P14 | SB37 | SG | - | Signal ground |
| P15 | SB38 | SG | - | Signal ground |
| P16 | SB39 | SG | - | Signal ground |
| P17 | SB40 | SG | - | Signal ground |
| P22 | VDDIN13 | +1.5VA | - | +1.5V |
| P23 | CGRESET | /CGRST | I | Configuration reset signal (Low-active) |
| P24 | PLL2VDD_A | +1.5VA | - | +1.5V |
| P25 | PLL2VSS_A | SG | - | Signal ground |
| P26 | PCICLKIN | PCICLKIN | I | PCI feedback bus clock |
| R01 | DATA35 | DATA[35] | I/O | System data bus [35] |
| R02 | DATA3 | DATA[3] | I/O | System data bus [3] |
| R03 | DATA34 | DATA[34] | I/O | System data bus [34] |
| R04 | VDDIO23 | +3.3V | - | +3.3V |
| R05 | VSS28 | SG | - | Signal ground |
| R10 | SB41 | SG | - | Signal ground |
| R11 | SB42 | SG | - | Signal ground |
| R12 | SB43 | SG | - | Signal ground |
| R13 | SB44 | SG | - | Signal ground |
| R14 | SB45 | SG | - | Signal ground |
| R15 | SB46 | SG | - | Signal ground |
| R16 | SB47 | SG | - | Signal ground |
| R17 | SB48 | SG | - | Signal ground |
| R22 | VSS29 | SG | - | Signal ground |
| R23 | VDDIN14 | +1.5VA | - | +1.5V |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| R24 | PLL1VDD_A | +1.5VA | - | +1.5V |
| R25 | PLL1VSS_A | SG | - | Signal ground |
| R26 | MASTERCLK | MASTERCLK | I | Master clock input (33.3333MHz) |
| T01 | VSS30 | SG | - | Signal ground |
| T02 | DATA5 | DATA[5] | I/O | System data bus [5] |
| T03 | DATA36 | DATA[36] | I/O | System data bus [36] |
| T04 | VDDIO24 | +3.3V | - | +3.3V |
| T05 | DATA4 | DATA[4] | I/O | System data bus [4] |
| T10 | SB49 | SG | - | Signal ground |
| T11 | SB50 | SG | - | Signal ground |
| T12 | SB51 | SG | - | Signal ground |
| T13 | SB52 | SG | - | Signal ground |
| T14 | SB53 | SG | - | Signal ground |
| T15 | SB54 | SG | - | Signal ground |
| T16 | SB55 | SG | - | Signal ground |
| T17 | SB56 | SG | - | Signal ground |
| T22 | DATA30 | DATA[30] | I/O | System data bus [30] |
| T23 | DATA62 | DATA[62] | I/O | System data bus [62] |
| T24 | VDDIO25 | +3.3V | - | +3.3V |
| T25 | DATA31 | DATA[31] | I/O | System data bus [31] |
| T26 | VSS31 | SG | - | Signal ground |
| U01 | DATA38 | DATA[38] | I/O | System data bus [38] |
| U02 | DATA6 | DATA[6] | I/O | System data bus [6] |
| U03 | DATA37 | DATA[37] | I/O | System data bus [37] |
| U04 | VDDIN15 | +1.5VA | - | +1.5V |
| U05 | VSS32 | SG | - | Signal ground |
| U10 | SB57 | SG | - | Signal ground |
| U11 | SB58 | SG | - | Signal ground |
| U12 | SB59 | SG | - | Signal ground |
| U13 | SB60 | SG | - | Signal ground |
| U14 | SB61 | SG | - | Signal ground |
| U15 | SB62 | SG | - | Signal ground |
| U16 | SB63 | SG | - | Signal ground |
| U17 | SB64 | SG | - | Signal ground |
| U22 | VSS33 | SG | - | Signal ground |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| U23 | VDDIN16 | +1.5VA | - | +1.5V |
| U24 | VDDIO26 | +3.3V | - | +3.3V |
| U25 | DATA61 | DATA[61] | I/O | System data bus [61] |
| U26 | VSS34 | SG | - | Signal ground |
| V01 | VSS35 | SG | - | Signal ground |
| V02 | VSS36 | SG | - | Signal ground |
| V03 | VDDIO27 | +3.3V | - | +3.3V |
| V04 | VDDIO28 | +3.3V | - | +3.3V |
| V05 | DATA7 | DATA[7] | I/O | System data bus [7] |
| V22 | VDDIO29 | +3.3V | - | +3.3V |
| V23 | DATA28 | DATA[28] | I/O | System data bus [28] |
| V24 | VSS37 | SG | - | Signal ground |
| V25 | DATA60 | DATA[60] | I/O | System data bus [60] |
| V26 | DATA29 | DATA[29] | I/O | System data bus [29] |
| W01 | DATA8 | DATA[8] | I/O | System data bus [8] |
| W02 | DATA39 | DATA[39] | I/O | System data bus [39] |
| W03 | VSS38 | SG | - | Signal ground |
| W04 | VDDIN17 | +1.5VA | - | +1.5V |
| W05 | VSS39 | SG | - | Signal ground |
| W22 | VSS40 | SG | - | Signal ground |
| W23 | VDDIO30 | +3.3V | - | +3.3V |
| W24 | VSS41 | SG | - | Signal ground |
| W25 | DATA27 | DATA[27] | I/O | System data bus [27] |
| W26 | DATA59 | DATA[59] | I/O | System data bus [59] |
| Y01 | DATA10 | DATA[10] | I/O | System data bus [10] |
| Y02 | DATA41 | DATA[41] | I/O | System data bus [41] |
| Y03 | VSS42 | SG | - | Signal ground |
| Y04 | DATA9 | DATA[9] | I/O | System data bus [9] |
| Y05 | DATA40 | DATA[40] | I/O | System data bus [40] |
| Y22 | VDDIO31 | +3.3V | - | +3.3V |
| Y23 | DATA25 | DATA[25] | I/O | System data bus [25] |
| Y24 | DATA57 | DATA[57] | I/O | System data bus [57] |
| Y25 | DATA26 | DATA[26] | I/O | System data bus [26] |
| Y26 | DATA58 | DATA[58] | I/O | System data bus [58] |
| AA01 | DATA43 | DATA[43] | I/O | System data bus [43] |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| AA02 | DATA11 | DATA[11] | I/O | System data bus [11] |
| AA03 | VDDIO32 | +3.3V | - | +3.3V |
| AA04 | VSS43 | SG | - | Signal ground |
| AA05 | DATA42 | DATA[42] | I/O | System data bus [42] |
| AA22 | DATA23 | DATA[23] | I/O | System data bus [23] |
| AA23 | VSS44 | SG | - | Signal ground |
| AA24 | DATA55 | DATA[55] | I/O | System data bus [55] |
| AA25 | DATA24 | DATA[24] | I/O | System data bus [24] |
| AA26 | DATA56 | DATA[56] | I/O | System data bus [56] |
| AB01 | DATA45 | DATA[45] | I/O | System data bus [45] |
| AB02 | DATA13 | DATA[13] | I/O | System data bus [13] |
| AB03 | DATA44 | DATA[44] | I/O | System data bus [44] |
| AB04 | DATA12 | DATA[12] | I/O | System data bus [12] |
| AB05 | VSS45 | SG | - | Signal ground |
| AB06 | DQM0 | DQM[0] | O | Output disable/write mask [0] for DIMM |
| AB07 | VDDIO33 | +3.3V | - | +3.3V |
| AB08 | VSS46 | SG | - | Signal ground |
| AB09 | ADDR3 | ADDR[3] | O | System address bus [3] |
| AB10 | VSS47 | SG | - | Signal ground |
| AB11 | ADDR7 | ADDR[7] | O | System address bus [7] |
| AB12 | VSS48 | SG | - | Signal ground |
| AB13 | VSS49 | SG | - | Signal ground |
| AB14 | VSS50 | SG | - | Signal ground |
| AB15 | VSS51 | SG | - | Signal ground |
| AB16 | ADDR17 | ADDR[17] | O | System address bus [17] |
| AB17 | VSS52 | SG | - | Signal ground |
| AB18 | SDCS3 | - | O | Not used (open) |
| AB19 | VSS53 | SG | - | Signal ground |
| AB20 | DQM7 | DQM[7] | O | Output disable/write mask [7] for DIMM |
| AB21 | CB3 | - | - | Not used (Pull-up: +3.3V) |
| AB22 | VSS54 | SG | - | Signal ground |
| AB23 | VDDIO34 | +3.3V | - | +3.3V |
| AB24 | VSS55 | SG | - | Signal ground |
| AB25 | DATA54 | DATA[54] | I/O | System data bus [54] |
| AB26 | VSS56 | SG | - | Signal ground |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| AC01 | DATA14 | DATA[14] | I/O | System data bus [14] |
| AC02 | VSS57 | SG | - | Signal ground |
| AC03 | VSS58 | SG | - | Signal ground |
| AC04 | VDDIN18 | +1.5VA | - | +1.5V |
| AC05 | VDDIO35 | +3.3V | - | +3.3V |
| AC06 | VSS59 | SG | - | Signal ground |
| AC07 | SDCS0 | /SDCS[0] | O | Chip select signal for DIMM (Low-active) |
| AC08 | VDDIO36 | +3.3V | - | +3.3V |
| AC09 | VDDIO37 | +3.3V | - | +3.3V |
| AC10 | VDDIN19 | +1.5VA | - | +1.5V |
| AC11 | ADDR8 | ADDR[8] | O | System address bus [8] |
| AC12 | VDDIN20 | +1.5VA | - | +1.5V |
| AC13 | VDDIO38 | +3.3V | - | +3.3V |
| AC14 | VDDIO39 | +3.3V | - | +3.3V |
| AC15 | VDDIO40 | +3.3V | - | +3.3V |
| AC16 | VDDIO41 | +3.3V | - | +3.3V |
| AC17 | VDDIN21 | +1.5VA | - | +1.5V |
| AC18 | DQM2 | DQM[2] | O | Output disable/write mask [2] for DIMM |
| AC19 | VDDIN22 | +1.5VA | - | +1.5V |
| AC20 | CB2 | /INT-FACT[2] | I | PCI interrupt request signal [2] (Low-active) |
| AC21 | VSS60 | SG | - | Signal ground |
| AC22 | DATA48 | DATA[48] | I/O | System data bus [48] |
| AC23 | VDDIN23 | +1.5VA | - | +1.5V |
| AC24 | VSS61 | SG | - | Signal ground |
| AC25 | DATA53 | DATA[53] | I/O | System data bus [53] |
| AC26 | DATA22 | DATA[22] | I/O | System data bus [22] |
| AD01 | VDDIO42 | +3.3V | - | +3.3V |
| AD02 | DATA46 | DATA[46] | I/O | System data bus [46] |
| AD03 | CB0 | /FXWUP | I | FAX wake-up request signal (Low-active) |
| AD04 | VSS62 | SG | - | Signal ground |
| AD05 | VSS63 | SG | - | Signal ground |
| AD06 | DQM4 | DQM[4] | O | Output disable/write mask [4] for DIMM |
| AD07 | SDCS1 | - | O | Not used (open) |
| AD08 | VSS64 | SG | - | Signal ground |
| AD09 | VSS65 | SG | - | Signal ground |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| AD10 | ADDR5 | ADDR[5] | O | System address bus [5] |
| AD11 | VSS66 | SG | - | Signal ground |
| AD12 | ADDR10 | ADDR[10] | O | System address bus [10] |
| AD13 | ADDR12 | ADDR[12] | O | System address bus [12] |
| AD14 | ADDR14 | ADDR[14] | O | System address bus [14] |
| AD15 | ADDR15 | ADDR[15] | O | System address bus [15] |
| AD16 | ADDR18 | ADDR[18] | O | System address bus [18] |
| AD17 | CKE | /CKE | O | Clock enable signal for DIMM |
| AD18 | DQM6 | DQM[6] | O | Output disable/write mask [6] for DIMM |
| AD19 | VSS67 | SG | - | Signal ground |
| AD20 | VSS68 | SG | - | Signal ground |
| AD21 | CB7 | /PELINT | I | ASIC interrupt request signal (Low-active) |
| AD22 | DATA17 | DATA[17] | I/O | System data bus [17] |
| AD23 | VSS69 | SG | - | Signal ground |
| AD24 | DATA50 | DATA[50] | I/O | System data bus [50] |
| AD25 | DATA52 | DATA[52] | I/O | System data bus [52] |
| AD26 | DATA21 | DATA[21] | I/O | System data bus [21] |
| AE01 | DATA15 | DATA[15] | I/O | System data bus [15] |
| AE02 | VDDIO43 | +3.3V | - | +3.3V |
| AE03 | CB4 | - | - | Not used (Pull-up: +3.3V) |
| AE04 | CB5 | - | - | Not used (Pull-up: +3.3V) |
| AE05 | WE | /WE | O | Write enable signal for DIMM (Low-active) |
| AE06 | DQM1 | DQM[1] | O | Output disable/write mask [1] for DIMM |
| AE07 | RAS | /RAS | O | Row address strobe signal for DIMM (Low-active) |
| AE08 | ADDR1 | ADDR[1] | O | System address bus [1] |
| AE09 | ADDR4 | ADDR[4] | O | System address bus [4] |
| AE10 | ADDR6 | ADDR[6] | O | System address bus [6] |
| AE11 | ADDR9 | ADDR[9] | O | System address bus [9] |
| AE12 | VSS70 | SG | - | Signal ground |
| AE13 | ADDR13 | ADDR[13] | O | System address bus [13] |
| AE14 | VSS71 | SG | - | Signal ground |
| AE15 | ADDR16 | ADDR[16] | O | System address bus [16] |
| AE16 | ADDR19 | ADDR[19] | O | System address bus [19] |
| AE17 | SDCS2 | - | O | Not used (open) |
| AE18 | VSS72 | SG | - | Signal ground |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| AE19 | DQM3 | DQM[3] | O | Output disable/write mask [3] for DIMM |
| AE20 | CB6 | /PWREN | O | Power output enable signal (Low-active) |
| AE21 | VDDIO44 | +3.3V | - | +3.3V |
| AE22 | DATA49 | DATA[49] | I/O | System data bus [49] |
| AE23 | VSS73 | SG | - | Signal ground |
| AE24 | VDDIO45 | +3.3V | - | +3.3V |
| AE25 | DATA20 | DATA[20] | I/O | System data bus [20] |
| AE26 | VDDIO46 | +3.3V | - | +3.3V |
| AF01 | VSS74 | SG | - | Signal ground |
| AF02 | DATA47 | DATA[47] | I/O | System data bus [47] |
| AF03 | CB1 | /INT-FACT[1] | I | PCI interrupt request signal [1] (Low-active) |
| AF04 | CAS | /CAS | O | Column address strobe signal for DIMM (Low-active) |
| AF05 | VSS75 | SG | - | Signal ground |
| AF06 | DQM5 | DQM[5] | O | Output disable/write mask [5] for DIMM |
| AF07 | ADDR0 | ADDR[0] | O | System address bus [0] |
| AF08 | ADDR2 | ADDR[2] | O | System address bus [2] |
| AF09 | VDDIO47 | +3.3V | - | +3.3V |
| AF10 | VSS76 | SG | - | Signal ground |
| AF11 | VDDIO48 | +3.3V | - | +3.3V |
| AF12 | ADDR11 | ADDR[11] | O | System address bus [11] |
| AF13 | SDCLK2 | SDCLK[2] | O | Pseudo clock signal output for DIMM control |
| AF14 | SDCLK0 | SDCLK[0] | O | Clock signal [0] output for DIMM |
| AF15 | SDCLKIN | SDCLKIN | I | Pseudo clock signal input for DIMM control |
| AF16 | VSS77 | SG | - | Signal ground |
| AF17 | SDCLK3 | - | - | Not used (Open) |
| AF18 | VSS78 | SG | - | Signal ground |
| AF19 | SDCLK1 | SDCLK[1] | O | Clock signal [1] output for DIMM |
| AF20 | VDDIO49 | +3.3V | - | +3.3V |
| AF21 | DATA16 | DATA[16] | I/O | System data bus [16] |
| AF22 | DATA18 | DATA[18] | I/O | System data bus [18] |
| AF23 | VDDIO50 | +3.3V | - | +3.3V |
| AF24 | DATA19 | DATA[19] | I/O | System data bus [19] |
| AF25 | DATA51 | DATA[51] | I/O | System data bus [51] |
| AF26 | VSS79 | SG | - | Signal ground |

## 2.2 Scanner CPU (TMP95C063F)

### 2.2.1 Outline and features

The TMP95C063F is developed as a high-speed, advanced 16-bit microcontroller for a range of mid to large-scale equipment.
This device is presented in a 144-pin plastic flat package. Its features are as follows.



1) Original high-speed 16-bit CPU (900H_CPU)
   - Instruction mnemonics upwardly compatible with TLCS-90/900
   - 16-Mbyte linear address space
   - General-purpose registers using register bank system
   - 16-bit multiplication/division instructions, bit transfer/arithmetic instructions
   - Micro DMA: 4 channels (640 ns/2 bytes at 25 MHz)
2) Minimum instruction execution time: 160 ns (at 25 MHz)
3) Internal RAM: No
   Internal ROM: No
4) External memory expansion
   - Expandable up to 16 Mbytes (common to programs and data)
   - External data bus width selection pin (AM8/$\overline{16}$)
   - Can use both 8- and 16-bit external buses
     ... Dynamic data bus sizing
5) Internal DRAM controller: 2 channels
   - 2$\overline{CAS}$/2$\overline{WE}$ selectable
6) 8-bit timer: 8 channels
7) 16-bit timer: 2 channels
8) Pattern generator: 4 bits, 2 channels
9) General-purpose serial interface: 2 channels
   - Baud rate generated by external clock
10) 10-bit A/D converter: 8 channels
11) 8-bit D/A converter: 2 channels
12) Watchdog timer
13) Chip selector, wait controller: 4 blocks
14) Interrupt function:
   - CPU interrupts: 2 (software interrupt instructions, illegal instructions)
   - Internal interrupts: 22 (7 priority levels available)
   - External interrupts: 11 (7 priority levels available)
15) Input/output ports
   - 91 pins
16) Standby function
   - 3 HALT modes (RUN, IDLE, STOP)

## 2.2.2 Functions

The Scanner CPU interfaces with the System CPU and RADF, and controls the whole system of the scanning section such as the scan motor, APS sensor, exposure lamp and such. The Scanner CPU also sets the parameter of each image processing ASIC. These control programs of the Scanner CPU are stored in the Flash ROM on the SLG board. These programs can be updated by downloading the new programs with the download jig, PC which is serially connected and so on.

## 2.2.3 Pin assignment

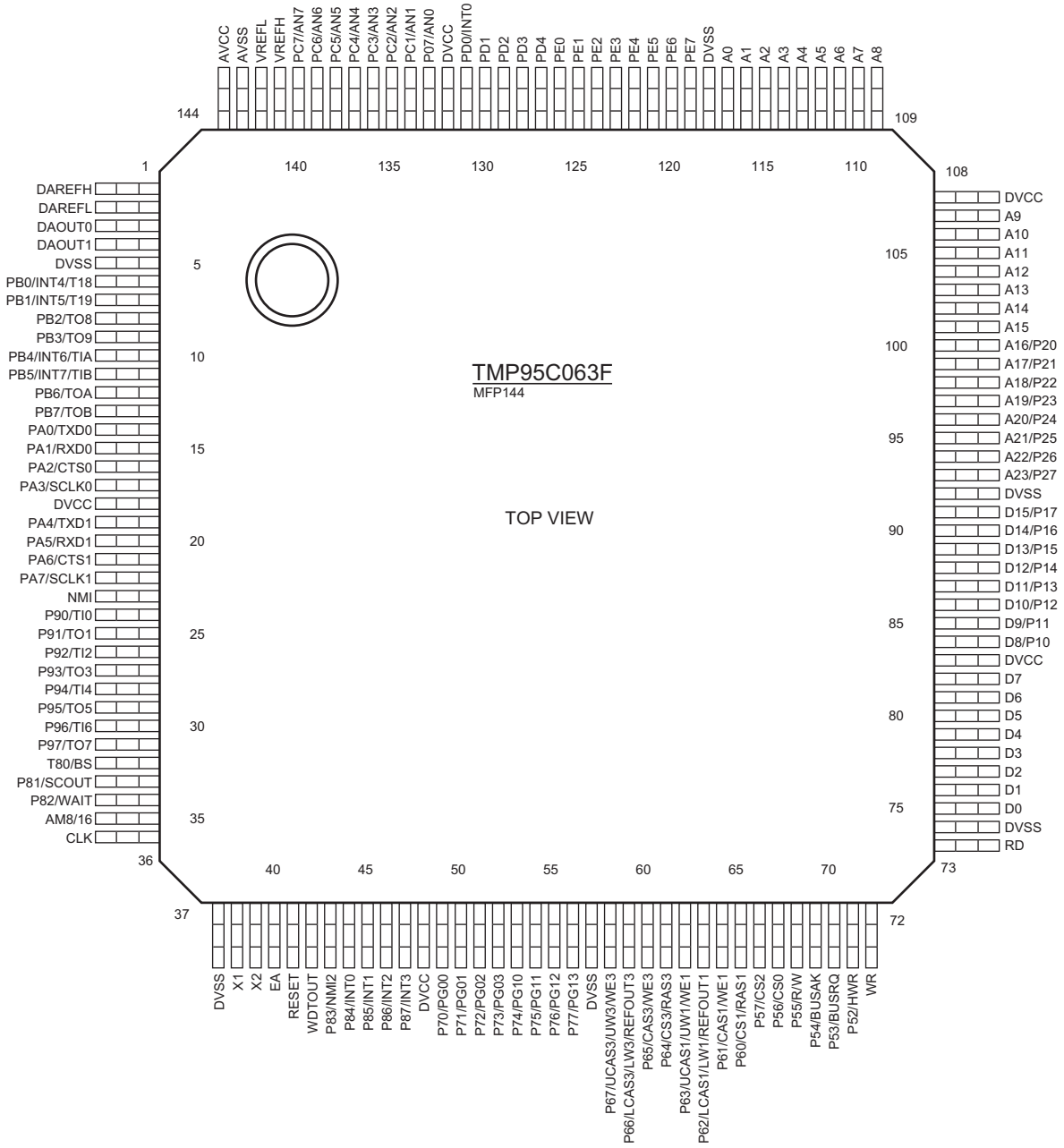



**Fig.2-2**

## 2.2.4 Signals

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 1 | DAREFH | DAREFH | I | Reference voltage (H) for D/A converter (+5V) |
| 2 | DAREFL | DAREFL | I | Reference voltage (L) for D/A converter (Signal ground) |
| 3 | DAOUT0 | MOTREF | O | Reference voltage for scan motor |
| 4 | DAOUT1 | - | - | Not used (Open) |
| 5 | DVSS1 | SG | - | Signal ground |
| 6 | PB0/INT4/TI8 | DFSCST | I | RADF scanning start signal |
| 7 | PB1/INT5/TI9 | - | - | Not used (Open) |
| 8 | PB2/TO8 | DFRAK | I | RADF acknowledge signal: SLG board <- RADF |
| 9 | PB3/TO9 | EEMCLK | O | EEPROM clock |
| 10 | PB4/INT6/TIA | DFRRQ | I | RADF request signal: SLG board <- RADF |
| 11 | PB5/INT7/TIB | - | - | Not used (Open) |
| 12 | PB6/TOA | PNCNT | I | Debug panel connection signal (L: connected) (for debug) |
| 13 | PB7/TOB | SSW | I | Debug panel SW status signal (for debug) |
| 14 | PA0/TXD0 | SRXD | O | Reception data: SLG board -> SYS board |
| 15 | PA1/RXD0 | STXDA | I | Transmission data: SLG board <- SYS board |
| 16 | PA2/$\overline{\text{CTS0}}$ | SRTSA | I | Transmission request signal: SLG board <- SYS board |
| 17 | PA3/SCLK0 | SCTS | O | Transmission clear signal: SLG board -> SYS board |
| 18 | DVCC1 | DVCC | - | +5V |
| 19 | PA4/TXD1 | DFTXD | O | Transmission data: SLG board -> RADF |
| 20 | PA5/RXD1 | DFRXD | I | Reception data: SLG <- RADF |
| 21 | PA6/$\overline{\text{CTS1}}$ | DFAK | O | Acknowledge signal: SLG board -> RADF |
| 22 | PA7/SCLK1 | DFRQ | O | Request signal: SLG -> RADF |
| 23 | $\overline{\text{NMI}}$ | /NMI | I | Non-maskable Interrupt signal (Pull-up: +5V) |
| 24 | P90/TI0 | EEMCS | O | EEPROM chip select signal |
| 25 | P91/TO1 | MOTCLK | O | Scan motor drive clock |
| 26 | P92/TI2 | - | - | Not used (Open) |
| 27 | P93/TO3 | LED | O | Download jig LED drive signal |
| 28 | P94/TI4 | EEMDTIN | I | EEPROM read data |
| 29 | P95/TO5 | EEMDTOUT | O | EEPROM write data |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 30 | P96/TI6 | 3BAPS1 | O | Not used |
| 31 | P97/TO7 | 3BAPS2 | O | Not used |
| 32 | P80/BS | 3BAPS3 | O | Not used |
| 33 | P81/SCOUT | - | - | Not used (Open) |
| 34 | P82/$\overline{\text{WAIT}}$ | - | - | Not used (Open) |
| 35 | AM8/$\overline{16}$ | WORD | I | Bus width selection signal<br>(H: 8-bit fixed, L: 8/16-bit coexisting) |
| 36 | CLK | - | - | Not used (Open) |
| 37 | DVSS2 | SG | - | Signal ground |
| 38 | X1 | X1 | I | Clock input (22MHz) |
| 39 | X2 | X2 | O | Clock output (22MHz) |
| 40 | $\overline{\text{EA}}$ | /EA | I | Pull-down: signal ground |
| 41 | $\overline{\text{RESET}}$ | MRST | I | Reset signal (Low-active) |
| 42 | $\overline{\text{WDTOUT}}$ | WDTOUT | O | Watchdog output signal<br>(H: CPU is normal, L: CPU is out of control) |
| 43 | P83/$\overline{\text{NMI2}}$ | - | - | Not used (Open) |
| 44 | P84/INT0 | - | - | Not used (Open) |
| 45 | P85/INT1 | - | - | Not used (Open) |
| 46 | P86/INT2 | DFCOPY | - | Not used (Open) |
| 47 | P87/INT3 | VSYNC | - | Not used (Open) |
| 48 | DVCC2 | +5V | - | +5V |
| 49 | P70/PG00 | DEBUG0 | O | Debug signal [0] |
| 50 | P71/PG01 | DEBUG1 | O | Debug signal [1] |
| 51 | P72/PG02 | DEBUG2 | O | Debug signal [2] |
| 52 | P73/PG03 | DEBUG3 | O | Debug signal [3] |
| 53 | P74/PG10 | DEBUG4 | O | Debug signal [4] |
| 54 | P75/PG11 | DEBUG5 | O | Debug signal [5] |
| 55 | P76/PG12 | DEBUG6 | O | Debug signal [6] |
| 56 | P77/PG13 | DEBUG7 | O | Debug signal [7] |
| 57 | DVSS3 | SG | - | Signal ground |
| 58 | P67/$\overline{\text{UCAS3}}$/$\overline{\text{UW3}}$/<br>$\overline{\text{WE3}}$ | - | - | Not used (Open) |
| 59 | P66/$\overline{\text{LCAS3}}$/$\overline{\text{LW3}}$/<br>$\overline{\text{REFOUT3}}$ | FANON | O | Not used |
| 60 | P65/$\overline{\text{CAS3}}$/$\overline{\text{WE3}}$ | FANCHG | O | Not used |
| 61 | P64/$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$ | CS3 | O | Chip select signal [3] (Low-active)<br>* For Flash (When PC download mode) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 62 | P63/$\overline{\text{UCAS}}$/$\overline{\text{UW1}}$/ $\overline{\text{WE}}$ | - | - | Not used (Open) |
| 63 | P62/$\overline{\text{LCAS}}$/$\overline{\text{LW1}}$/ $\overline{\text{REFOUT1}}$ | LMPON | O | Exposure lamp ON signal (L: ON) |
| 64 | P61/$\overline{\text{CAS1}}$/$\overline{\text{WE1}}$ | CCDPSOFF | - | Not used (Open) |
| 65 | P60/$\overline{\text{CS1}}$/$\overline{\text{RAS1}}$ | CS1 | O | Chip select signal [1] (Low-active)<br>* For SRAM |
| 66 | P57/$\overline{\text{CS2}}$ | CS2 | O | Chip select signal [2] (Low-active)<br>* For Flash ROM |
| 67 | P56/$\overline{\text{CS0}}$ | CS0 | O | Chip select signal [0] (Low-active)<br>* For ASIC |
| 68 | P55/R/$\overline{\text{W}}$ | ASICWR | O | ASIC data bus input/output switching signal (H: input, L: output) |
| 69 | P54/$\overline{\text{BUSAK}}$ | PGNCNT | I | Not used |
| 70 | P53/$\overline{\text{BUSRQ}}$ | TSTSEL | I | Not used |
| 71 | P52/$\overline{\text{HWR}}$ | - | - | Not used (Open) |
| 72 | $\overline{\text{WR}}$ | MWR | O | Write signal (Low-active) |
| 73 | $\overline{\text{RD}}$ | MRD | O | Read signal (Low-active) |
| 74 | DVSS4 | SG | - | Signal ground |
| 75 | D0 | MDT[0] | I/O | Data bus [0] |
| 76 | D1 | MDT[1] | I/O | Data bus [1] |
| 77 | D2 | MDT[2] | I/O | Data bus [2] |
| 78 | D3 | MDT[3] | I/O | Data bus [3] |
| 79 | D4 | MDT[4] | I/O | Data bus [4] |
| 80 | D5 | MDT[5] | I/O | Data bus [5] |
| 81 | D6 | MDT[6] | I/O | Data bus [6] |
| 82 | D7 | MDT[7] | I/O | Data bus [7] |
| 83 | DVCC3 | +5V | - | +5V |
| 84 | D8/P10 | MDT[8] | I/O | Data bus [8] |
| 85 | D9/P11 | MDT[9] | I/O | Data bus [9] |
| 86 | D10/P12 | MDT[10] | I/O | Data bus [10] |
| 87 | D11/P13 | MDT[11] | I/O | Data bus [11] |
| 88 | D12/P14 | MDT[12] | I/O | Data bus [12] |
| 89 | D13/P15 | MDT[13] | I/O | Data bus [13] |
| 90 | D14/P16 | MDT[14] | I/O | Data bus [14] |
| 91 | D15/P17 | MDT[15] | I/O | Data bus [15] |
| 92 | DVSS5 | SG | - | Signal ground |
| 93 | A23/P27 | DWNLD | O | PC download enable signal (Low-active) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 94 | A22/P26 | 5VSWON | O | 5VSW power supply signal (Low-active) |
| 95 | A21/P25 | PNGT | O | Debug panel control signals ON/OFF signal (for debug) |
| 96 | A20/P24 | - | - | Not used (Open) |
| 97 | A19/P23 | SLEEP | O | ASIC sleep mode control signal (H: sleep mode) |
| 98 | A18/P22 | MAD[18] | O | Address bus [18] |
| 99 | A17/P21 | MAD[17] | O | Address bus [17] |
| 100 | A16/P20 | MAD[16] | O | Address bus [16] |
| 101 | A15 | MAD[15] | O | Address bus [15] |
| 102 | A14 | MAD[14] | O | Address bus [14] |
| 103 | A13 | MAD[13] | O | Address bus [13] |
| 104 | A12 | MAD[12] | O | Address bus [12] |
| 105 | A11 | MAD[11] | O | Address bus [11] |
| 106 | A10 | MAD[10] | O | Address bus [10] |
| 107 | A9 | MAD[9] | O | Address bus [9] |
| 108 | DVCC4 | +5V | - | +5V |
| 109 | A8 | MAD[8] | O | Address bus [8] |
| 110 | A7 | MAD[7] | O | Address bus [7] |
| 111 | A6 | MAD[6] | O | Address bus [6] |
| 112 | A5 | MAD[5] | O | Address bus [5] |
| 113 | A4 | MAD[4] | O | Address bus [4] |
| 114 | A3 | MAD[3] | O | Address bus [3] |
| 115 | A2 | MAD[2] | O | Address bus [2] |
| 116 | A1 | MAD[1] | O | Address bus [1] |
| 117 | A0 | MAD[0] | O | Address bus [0] |
| 118 | DVSS6 | SG | - | Signal ground |
| 119 | PE7 | PSYNC | O | Not used |
| 120 | PE6 | APSON | O | APS sensor power supply control signal (H: supply, L: cut off) |
| 121 | PE5 | - | - | Not used (Open) |
| 122 | PE4 | MOTMD3 | O | Scan motor control data [3] |
| 123 | PE3 | MOTMD2 | O | Scan motor control data [2] |
| 124 | PE2 | MOTMD1 | O | Scan motor control data [1] |
| 125 | PE1 | MOTDIR | O | Scan motor rotational direction switch signal (H: CCW, L: CW) |
| 126 | PE0 | MOTEN | O | Scan motor hold ON/OFF signal (H: ON, L: OFF) |
| 127 | PD4 | ROMDT | I | Download jig connection signal (L: connected) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 128 | PD3 | DFCNT | I | RADF connection signal (L: connected) |
| 129 | PD2 | APS3 | I | APS-3 sensor output signal (Low-active) |
| 130 | PD1 | APS2 | I | APS-2 sensor output signal (Low-active) |
| 131 | PD0/INT8 | APS1 | I | APS-1 sensor output signal (Low-active) |
| 132 | DVCC5 | +5V | - | +5V |
| 133 | PC0/AN0 | TSTMEM | I | Not used |
| 134 | PC1/AN1 | 3BAPSIN | I | Not used |
| 135 | PC2/AN2 | +24VCHK | I | +24V voltage check |
| 136 | PC3/AN3 | - | - | Signal ground |
| 137 | PC4/AN4 | HOME | I | Carriage home position sensor detect signal (H: home position) |
| 138 | PC5/AN5 | PLTN | I | Platen sensor detect signal (H: closed L: open) |
| 139 | PC6/AN6 | APSC | I | APS-C sensor output signal (Low-active) |
| 140 | PC7/AN7 | APSR | I | APS-R sensor output signal (Low-active) |
| 141 | VREFH | VREFH | I | Reference voltage (H) for A/D converter (+5V) |
| 142 | VREFL | VREFL | I | Reference voltage (L) for A/D converter (Signal ground) |
| 143 | AVSS | AVSS | I | A/D converter ground (Signal ground) |
| 144 | AVCC | AVCC | I | A/D converter power supply (+5V) |

## 2.3 Engine CPU (TMP95C063F)

### 2.3.1 Outline and features

The Engine CPU employs the same elemental devices as those of the Scanner CPU. Refer to the following pages for the outline and features of these elemental devices.📖 P.2-17 "2.2.1 Outline and features"

### 2.3.2 Functions

The Engine CPU interfaces with the System CPU, gate array, laser unit and finisher controller PC board (IPC board), and controls the whole system of the printer engine section. These control programs of the Engine CPU are stored in the Flash ROM on the LGC board. These programs can be updated by downloading the new programs with the download jig, PC which is serially connected and so on. The adjustment/setting value related with the control of engine section is stored in the removable NVRAM on the LGC board in order to prevent a data loss and simplify the data transfer process at the board replacement.

### 2.3.3 Pin assignment

The Engine CPU employs the same elemental devices as those of the Scanner CPU. Refer to the following pages for the pin assignment of these elemental devices.📖 P.2-18 "2.2.3 Pin assignment"

## 2.3.4 Signals

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 1 | DAREFH | DAREFH | I | Reference voltage (H) for D/A converter (+5V) |
| 2 | DAREFL | DAREFL | I | Reference voltage (L) for D/A converter (Signal ground) |
| 3 | DAOUT0 | ADUVR-1 | O | Reference voltage for ADU motor current restriction |
| 4 | DAOUT1 | ATSVR-1 | O | Reference voltage for Auto-toner sensor |
| 5 | DVSS1 | SG | - | Signal ground |
| 6 | PB0/INT4/TI8 | HTRSTOP-1 | I | Fuser unit abnormality control signal (H: heater abnormal, L: normal) |
| 7 | PB1/INT5/TI9 | OVERHEAT-1 | I | Fuser unit overheating detection signal (H: overheated, L: normal) |
| 8 | PB2/TO8 | PLLENM-0 | O | Phase locked loop control enable signal for main clock (H: enable) |
| 9 | PB3/TO9 | PLLENP-0 | O | Phase locked loop control enable signal for printer clock (H: enable) |
| 10 | PB4/INT6/TIA | SCOUT-1 | I | Timer clock input<br>* From pin33 |
| 11 | PB5/INT7/TIB | HVSDWN-1A | I | High-voltage transformer leakage detection signal (H: high-voltage transformer abnormal, L: normal) |
| 12 | PB6/TOA | POMCK-0 | O | Polygonal motor reference clock |
| 13 | PB7/TOB | PS12NG-1 | I | +12V supervisory signal (H: +12V abnormal L: normal) |
| 14 | PA0/TXD0 | - | O | Not used (Open) |
| 15 | PA1/RXD0 | - | O | Not used (Open) |
| 16 | PA2/$\overline{CTS0}$ | - | O | Not used (Open) |
| 17 | PA3/SCLK0 | - | I | Not used |
| 18 | DVCC1 | DVCC | - | +5V |
| 19 | PA4/TXD1 | - | O | Not used (Open) |
| 20 | PA5/RXD1 | - | O | Not used |
| 21 | PA6/$\overline{CTS1}$ | LED-1 | O | Download jig LED drive signal (L: LED ON) |
| 22 | PA7/SCLK1 | FMBSY-0 | I | Flash ROM status signal (H: ready, L: busy) |
| 23 | $\overline{NMI}$ | /NMI | I | Non-maskable Interrupt signal (Pull-up: +5V) |
| 24 | P90/TI0 | - | I | Not used (Open) |
| 25 | P91/TO1 | - | I | Not used (Open) |
| 26 | P92/TI2 | - | I | Not used |
| 27 | P93/TO3 | YDRV-0 | O | Not used |
| 28 | P94/TI4 | SCOUT-1 | I | Timer clock input<br>* From pin33 |
| 29 | P95/TO5 | - | - | Not used (Open) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 30 | P96/TI6 | - | - | - |
| 31 | P97/TO7 | - | - | - |
| 32 | P80/BS | PS5SNG-1 | I | +5VSW supervisory signal<br>(H: +5VSW abnormal, L: normal) |
| 33 | P81/SCOUT | SCOUT | O | Timer clock output<br>* To pins10 and 28 |
| 34 | P82/$\overline{\text{WAIT}}$ | YFAN2L-0 | O | Not used |
| 35 | AM8/$\overline{16}$ | ROMDT-1 | I | Bus width selection signal<br>(H: 8-bit fixed, L: 8/16-bit coexisting) |
| 36 | CLK | - | - | Not used (Open) |
| 37 | DVSS2 | SG | - | Signal ground |
| 38 | X1 | X1 | I | Clock input (24MHz) |
| 39 | X2 | X2 | O | Clock output (24MHz) |
| 40 | $\overline{\text{EA}}$ | /EA | I | Pull-down: signal ground |
| 41 | $\overline{\text{RESET}}$ | CPURST-0 | I | Reset signal (Low-active) |
| 42 | $\overline{\text{WDTOUT}}$ | WDT-0 | O | Watchdog output signal<br>(H: CPU is normal, L: CPU is out of control) |
| 43 | P83/$\overline{\text{NMI2}}$ | YFAN2H-0 | O | Not used |
| 44 | P84/INT0 | STINT-1 | I | Transmission interrupt signal:<br>LGC board -> SYS board |
| 45 | P85/INT1 | HSCTCP-1A | I | H-sync counter coincidence status signal<br>(H: coincided, L: not coincided) |
| 46 | P86/INT2 | CMINT-1 | I | Reception interrupt signal:<br>LGC board <- SYS board |
| 47 | P87/INT3 | PDWN-1 | I | Switching regulator power down signal<br>(H: regulator ON or OFF, L: normal) |
| 48 | DVCC2 | +5V | - | +5V |
| 49 | P70/PG00 | ADUM1A-0 | O | ADU motor drive signal [phase-A] (Low-active) |
| 50 | P71/PG01 | ADUM1B-0 | O | ADU motor drive signal [phase-B] (Low-active) |
| 51 | P72/PG02 | ADUM1C-0 | O | ADU motor drive signal [phase-C] (Low-active) |
| 52 | P73/PG03 | ADUM1D-0 | O | ADU motor drive signal [phase-D] (Low-active) |
| 53 | P74/PG10 | EXTMA-0 | O | Exit motor drive signal [phase-A] (Low-active) |
| 54 | P75/PG11 | EXTMB-0 | O | Exit motor drive signal [phase-B] (Low-active) |
| 55 | P76/PG12 | EXTMC-0 | O | Exit motor drive signal [phase-C] (Low-active) |
| 56 | P77/PG13 | EXTMD-0 | O | Exit motor drive signal [phase-D] (Low-active) |
| 57 | DVSS3 | SG | - | Signal ground |
| 58 | P67/$\overline{\text{UCAS3}}$/$\overline{\text{UW3}}$/<br>$\overline{\text{WE3}}$ | PWRFNL-0 | O | Internal cooling fan-2 low speed drive signal |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 59 | P66/$\overline{\text{LCAS3}}$/$\overline{\text{LW3}}$/ $\overline{\text{REFOUT3}}$ | PWRFNH-0 | O | Internal cooling fan-2 high speed drive signal<br>PWRFNH-0 PWRFNL-0 Status<br>L L High speed drive<br>L H High speed drive<br>H L Low speed drive<br>H H Stop |
| 60 | P65/$\overline{\text{CAS3}}$/$\overline{\text{WE3}}$ | RSTSW1-0 | O | Main switch reset signal<br>(H: normal L: reset (power is turn OFF)) |
| 61 | P64/$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$ | CS3-0 | O | Chip select signal [3] (Low-active)<br>* For SRAM |
| 62 | P63/$\overline{\text{UCAS}}$/$\overline{\text{UW1}}$/ $\overline{\text{WE}}$ | ERSLP-0 | O | Discharger LED drive signal (L: ON) |
| 63 | P62/$\overline{\text{LCAS}}$/$\overline{\text{LW1}}$/ $\overline{\text{REFOUT1}}$ | CLNFNL-0 | O | Internal cooling fan-1 low speed drive signal |
| 64 | P61/$\overline{\text{CAS1}}$/$\overline{\text{WE1}}$ | CLNFNH-0 | O | Internal cooling fan-1 high speed drive signal<br>CLNFNH-0 CLNFNL-0 Status<br>L L High speed drive<br>L H High speed drive<br>H L Low speed drive<br>H H Stop |
| 65 | P60/$\overline{\text{CS1}}$/$\overline{\text{RAS1}}$ | CS1-0 | O | Chip select signal [1] (Low-active)<br>* For Gate Array (EC/N075: IC24) |
| 66 | P57/$\overline{\text{CS2}}$ | CS2-0 | O | Chip select signal [2] (Low-active)<br>* For Flash ROM |
| 67 | P56/$\overline{\text{CS0}}$ | CS0-0 | O | Chip select signal [0] (Low-active)<br>* For ASIC |
| 68 | P55/R/$\overline{\text{W}}$ | RW-0 | O | Read/write signal (H: read, L: write)<br>* For IPC bus direction |
| 69 | P54/$\overline{\text{BUSAK}}$ | POMON-0 | O | Polygonal motor drive signal (H: OFF, L: ON) |
| 70 | P53/$\overline{\text{BUSRQ}}$ | POMPL-0 | I | Polygonal motor phase locked loop control signal<br>(H: stop or error, L: uniform speed driving) |
| 71 | P52/$\overline{\text{HWR}}$ | POMDT-0 | I | Download jig connection signal (L: connected) |
| 72 | $\overline{\text{WR}}$ | WR-0 | O | Write signal (Low-active) |
| 73 | $\overline{\text{RD}}$ | RD-0 | O | Read signal (Low-active) |
| 74 | DVSS4 | SG | - | Signal ground |
| 75 | D0 | D[0] | I/O | Data bus [0] |
| 76 | D1 | D[1] | I/O | Data bus [1] |
| 77 | D2 | D[2] | I/O | Data bus [2] |
| 78 | D3 | D[3] | I/O | Data bus [3] |
| 79 | D4 | D[4] | I/O | Data bus [4] |
| 80 | D5 | D[5] | I/O | Data bus [5] |
| 81 | D6 | D[6] | I/O | Data bus [6] |
| 82 | D7 | D[7] | I/O | Data bus [7] |
| 83 | DVCC3 | +5V | - | +5V |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 84 | D8/P10 | D[8] | I/O | Data bus [8] |
| 85 | D9/P11 | D[9] | I/O | Data bus [9] |
| 86 | D10/P12 | D[10] | I/O | Data bus [10] |
| 87 | D11/P13 | D[11] | I/O | Data bus [11] |
| 88 | D12/P14 | D[12] | I/O | Data bus [12] |
| 89 | D13/P15 | D[13] | I/O | Data bus [13] |
| 90 | D14/P16 | D[14] | I/O | Data bus [14] |
| 91 | D15/P17 | D[15] | I/O | Data bus [15] |
| 92 | DVSS5 | SG | - | Signal ground |
| 93 | A23/P27 | A[23] | O | Address bus [23]<br>* For generation of Flash ROM chip select signal |
| 94 | A22/P26 | A[22] | O | Address bus [22]<br>* For generation of Flash ROM chip select signal |
| 95 | A21/P25 | - | - | Not used (Open) |
| 96 | A20/P24 | - | - | Not used (Open) |
| 97 | A19/P23 | WDE-0 | O | Watchdog enable signal (H: enable) |
| 98 | A18/P22 | A[18] | O | Address bus [18] |
| 99 | A17/P21 | A[17] | O | Address bus [17] |
| 100 | A16/P20 | A[16] | O | Address bus [16] |
| 101 | A15 | A[15] | O | Address bus [15] |
| 102 | A14 | A[14] | O | Address bus [14] |
| 103 | A13 | A[13] | O | Address bus [13] |
| 104 | A12 | A[12] | O | Address bus [12] |
| 105 | A11 | A[11] | O | Address bus [11] |
| 106 | A10 | A[10] | O | Address bus [10] |
| 107 | A9 | A[9] | O | Address bus [9] |
| 108 | DVCC4 | +5V | - | +5V |
| 109 | A8 | A[8] | O | Address bus [8] |
| 110 | A7 | A[7] | O | Address bus [7] |
| 111 | A6 | A[6] | O | Address bus [6] |
| 112 | A5 | A[5] | O | Address bus [5] |
| 113 | A4 | A[4] | O | Address bus [4] |
| 114 | A3 | A[3] | O | Address bus [3] |
| 115 | A2 | A[2] | O | Address bus [2] |
| 116 | A1 | A[1] | O | Address bus [1] |
| 117 | A0 | A[0] | O | Address bus [0] |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 118 | DVSS6 | SG | - | Signal ground |
| 119 | PE7 | LDOFF-0 | O | Enforced laser OFF signal<br>(H: normal, L: laser turn OFF) |
| 120 | PE6 | LE-0 | O | Laser enable signal<br>(H: laser turn ON disable, L: laser turn ON enable) |
| 121 | PE5 | GCCTCP-1A | I | Pixel counter coincidence status signal<br>(H: coincided, L: not coincided) |
| 122 | PE4 | EWSCN-0 | I | Not used |
| 123 | PE3 | BUSEN-1 | O | Not used |
| 124 | PE2 | CSCHG-0 | O | Chip select circuit switch signal<br>(H: ASIC selected, L: normal) |
| 125 | PE1 | FCOVSW-1 | I | Front cover opening/closing switch detection signal<br>(H: opened, L: closed) |
| 126 | PE0 | PSTPSW-1 | I | Registration sensor detection signal<br>(H: paper transport, L: none) |
| 127 | PD4 | MVDEN-0 | O | Paper transport signal<br>(H: standby, L: paper transport) |
| 128 | PD3 | PVDEN-0A | I | VDEN signal (H: standby, L: printing) |
| 129 | PD2 | ERR1-1A | I | H-Sync/PWM calibration error detection signal<br>(H: error) |
| 130 | PD1 | LDON-0 | O | Laser ON signal (H: OFF, L: ON) |
| 131 | PD0/INT8 | CSTCSW-1 | I | Side cover opening/closing sensor detection signal<br>(H: opened, L: closed) |
| 132 | DVCC5 | +5V | - | +5V |
| 133 | PC0/AN0 | HMS-1 | I | Temperature/humidity sensor detection signal<br>(Analog signal)<br>* humidity detection |
| 134 | PC1/AN1 | TEMP-1 | I | Temperature/humidity sensor detection signal<br>(Analog signal)<br>* temperature detection |
| 135 | PC2/AN2 | DRTH-1 | I | Drum thermistor detection signal<br>(Analog signal) |
| 136 | PC3/AN3 | FCOV2-1 | I | Cover opening/closing status detection signal<br>(Analog signal)<br>* +24V(+24VD2) supply status detection |
| 137 | PC4/AN4 | MTH--1A | I | Center thermistor detection signal<br>(Analog signal) |
| 138 | PC5/AN5 | STH--1A | I | Side thermistor detection signal<br>(Analog signal) |
| 139 | PC6/AN6 | ETH--1A | I | Edge thermistor detection signal<br>(Analog signal) |
| 140 | PC7/AN7 | ATS-1 | I | Auto-toner sensor detection signal<br>(Analog signal) |
| 141 | VREFH | VREFH | I | Reference voltage (H) for A/D converter (+5V) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 142 | VREFL | VREFL | I | Reference voltage (L) for A/D converter (Signal ground) |
| 143 | AVSS | AVSS | I | A/D converter ground (Signal ground) |
| 144 | AVCC | AVCC | I | A/D converter power supply (+5V) |

## 2.4 Gate Array (EC/N075)

### 2.4.1 Functions

The gate array is controlled by command from the Engine CPU and the logic circuit inside the gate array. The primary functions of the gate array are as follows.

- I/O control of each electrical part (motor, sensor, switch, electromagnetic spring clutch, solenoid, etc.)
- Interface to control the bypass unit and ADU
- Interface to control the high-voltage transformer
- Interface to control the PFP, LCF and finisher
- Interface to control the NVRAM on the LGC board
  (An erroneous data loss is prevented with a key circuit provided when the CPU is running away.)

### 2.4.2 Pin assignment

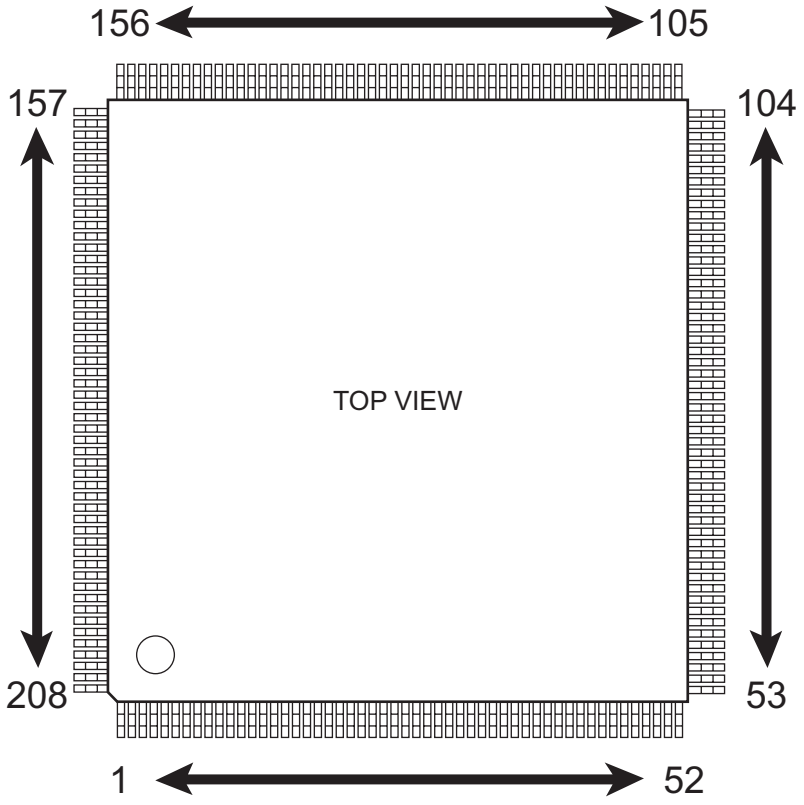



**Fig.2-3**

## 2.4.3 Signals

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 1 | LVDD1 | +3.3V | - | +3.3V |
| 2 | PA4 | - | O | Upper transport clutch drive request signal<br>(H: OFF, L: ON)<br>* To pin202 |
| 3 | PA5 | 1STCLL-0 | O | Middle transport clutch drive signal (H: OFF, L: ON)<br>* It is also a middle transport clutch drive request signal (To pin203) |
| 4 | PA6 | CLTRM-0 | O | Tray-up motor control signal [1] |
| 5 | PA7 | CLTRM-1 | O | Tray-up motor control signal [2]<br>CLTRM-1 CLTRM-0 Status<br>L L OFF<br>L H CCW<br>H L CW<br>H H Break |
| 6 | HVSS1 | SG | - | Signal ground |
| 7 | PB0 | ATSCNT-1 | I | Auto-toner sensor connection signal<br>(L: connected) |
| 8 | PB1 | HTBOXSW-1 | I | Not used |
| 9 | PB2 | TNFULL-1 | I | Auger lock switch detection signal<br>(H: full of recycled toner, L: normal) |
| 10 | PB3 | TNRSW-1 | I | Toner cartridge installation switch detection signal<br>(H: cartridge absence, L: cartridge presence) |
| 11 | HVSS2 | SG | - | Signal ground |
| 12 | PB4 | MAMPL-1 | I | Main motor phase locked loop control signal<br>(H: stop or error, L: uniform speed driving) |
| 13 | PB5 | 1STFED-1 | I | 1st transport sensor detection signal<br>(H: paper transport L: none) |
| 14 | PB6 | 2NDFED-1 | I | 2nd transport sensor detection signal<br>(H: paper transport L: none) |
| 15 | PB7 | SDCSW-1 | I | Transfer cover opening/closing switch detection signal (H: opened, L: closed) |
| 16 | HVDD | +5V | - | +5V |
| 17 | PC0 | TNRM-0 | O | Toner motor control signal [1] |
| 18 | PC1 | TNRM-1 | O | Toner motor control signal [2]<br>TNRM-1 TNRM-0 Status<br>L L OFF<br>L H CCW<br>H L CW<br>H H Break |
| 19 | PC2 | RGTCL-0 | O | Registration roller clutch drive signal<br>(H: OFF, L: ON) |
| 20 | PC3 | MAMON-0 | O | Main motor ON signal (H: OFF, L: ON) |
| 21 | HVSS3 | SG | - | Signal ground |
| 22 | PC4 | MAMBK-0 | O | Main motor brake signal (L: brake) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 23 | PC5 | MAMCW-1 | O | Main motor rotational direction switch signal (H: CCW, L: CW) |
| 24 | PC6 | CLKB-1 | O | PFP/LCF signal output switch signal [1] (Up-edge trigger) |
| 25 | PC7 | CLKC-1 | O | PFP/LCF signal output switch signal [2] (Up-edge trigger) |
| 26 | LVSS1 | SG | - | Signal ground |
| 27 | LVDD2 | +3.3V | - | +3.3V |
| 28 | HVDD2 | +5V | - | +5V |
| 29 | A0 | A[0] | I | Address bus [0] |
| 30 | A1 | A[1] | I | Address bus [1] |
| 31 | A2 | A[2] | I | Address bus [2] |
| 32 | A3 | A[3] | I | Address bus [3] |
| 33 | A4 | A[4] | I | Address bus [4] |
| 34 | A5 | A[5] | I | Address bus [5] |
| 35 | HVSS4 | SG | - | Signal ground |
| 36 | A6 | A[6] | I | Address bus [6] |
| 37 | A7 | A[7] | I | Address bus [7] |
| 38 | A12 | A[12] | I | Address bus [12] |
| 39 | A13 | A[13] | I | Address bus [13] |
| 40 | A14 | A[14] | I | Address bus [14] |
| 41 | HVDD3 | +5V | - | +5V |
| 42 | D0 | D[0] | I/O | Data bus [0] |
| 43 | D1 | D[1] | I/O | Data bus [1] |
| 44 | D2 | D[2] | I/O | Data bus [2] |
| 45 | D3 | D[3] | I/O | Data bus [3] |
| 46 | HVSS5 | SG | - | Signal ground |
| 47 | D4 | D[4] | I/O | Data bus [4] |
| 48 | D5 | D[5] | I/O | Data bus [5] |
| 49 | D6 | D[6] | I/O | Data bus [6] |
| 50 | D7 | D[7] | I/O | Data bus [7] |
| 51 | HVSS6 | SG | - | Signal ground |
| 52 | LVSS2 | SG | - | Signal ground |
| 53 | LVDD3 | +3.3V | - | +3.3V |
| 54 | RD | RD-0 | I | Read signal (Low-active) |
| 55 | WR | WR-0 | I | Write signal (Low-active) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 56 | CS | CS1-0 | I | Chip select signal [1] (Low-active)<br>* For Gate Array (EC/N075: IC24) |
| 57 | HVSS7 | SG | - | Signal ground |
| 58 | CTS | - | - | Pull-up: +5V |
| 59 | RXD | - | - | Pull-up: +5V |
| 60 | CBSY | CBSY-0 | I | System interface command busy signal |
| 61 | CMD | CMD-0 | I | System interface received data signal |
| 62 | SACK | SACK-0 | I | System interface status acknowledge signal |
| 63 | SERR | SERR-0 | I | System interface status error signal |
| 64 | HVDD4 | +5V | - | +5V |
| 65 | RXDINT | - | - | Not used (Open) |
| 66 | TXDINT | - | - | Not used (Open) |
| 67 | CMDINT | CMINT-1 | O | System interface reception interrupt signal |
| 68 | STSINT | STINT-1 | O | System interface transmission interrupt signal |
| 69 | RTS | - | - | Not used (Open) |
| 70 | HVSS8 | SG | - | Signal ground |
| 71 | TXD | - | - | Not used (Open) |
| 72 | SBSY | SBSY-0 | O | System interface status busy signal |
| 73 | STS | STS | O | System interface transmitted data signal |
| 74 | CACK | CACK-0 | O | System interface command acknowledge signal |
| 75 | CERR | CERR-0 | O | System interface command error signal |
| 76 | HVSS9 | SG | - | Signal ground |
| 77 | SCLK | - | - | Pull-up: +5V |
| 78 | HVDD5 | +5V | - | +5V |
| 79 | RESET | GARST-0 | I | Reset signal (Low-active) |
| 80 | HVSS10 | SG | - | Signal ground |
| 81 | CNTRST | - | - | Pull-up: +5V |
| 82 | TESTSW | - | - | Pull-down: signal ground |
| 83 | TSTEN | - | - | Pull-down: signal ground |
| 84 | LVSS3 | SG | - | Signal ground |
| 85 | PD0 | TSIZE0-1 | O | Paper size signal [0] for copy key card |
| 86 | PD1 | TSIZE1-1 | O | Paper size signal [1] for copy key card |
| 87 | PD2 | TSIZE2-1 | O | Paper size signal [2] for copy key card |
| 88 | PD3 | TSIZE3-1 | O | Paper size signal [3] for copy key card |
| 89 | LVDD4 | +3.3V | - | +3.3V |
| 90 | PD4 | FLCTR-0 | O | Back-side printing count signal for copy key card |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 91 | PD5 | MNCTR-0 | O | Mono color printing count signal for copy key card |
| 92 | PD6 | BKCTR-0 | O | Black printing count signal for copy key card |
| 93 | PD7 | EXTCTR-0 | O | Paper exit signal for coin controller |
| 94 | HVSS11 | SG | - | Signal ground |
| 95 | PE0 | MCRUN-0 | O | Equipment operation status signal for copy key card |
| 96 | PE1 | CTRON-0 | O | Total count signal for copy key card |
| 97 | PE2 | KCTRON-0 | O | ON signal for key copy counter |
| 98 | PE3 | HVTM-0 | O | Charger/grid bias ON signal (L: ON) |
| 99 | HVSS12 | SG | - | Signal ground |
| 100 | PE4 | HVTT-0 | O | Transfer bias ON signal (L: ON) |
| 101 | PE5 | HVTAC-0 | O | Developer AC bias ON signal (L: ON) |
| 102 | PE6 | HVTSP-0 | O | Separation bias ON signal (L: ON) |
| 103 | PE7 | HVTGB-0 | O | Transfer guide bias ON signal (L: ON) |
| 104 | HVDD6 | +5V | - | +5V |
| 105 | HVSS13 | SG | - | Signal ground |
| 106 | OSC1 | OSC1 | I | Clock input (8.334MHz) |
| 107 | HVDD7 | +5V | - | +5V |
| 108 | OSC2 | OSC2 | O | Clock output (8.334MHz) |
| 109 | HVSS14 | SG | - | Signal ground |
| 110 | DICH1 | DADAT1-1 | O | D/A converter serial data |
| 111 | LDCH1 | DALTH1-1 | O | D/A converter latch signal |
| 112 | CLKCH1 | DACLK1-1 | O | D/A converter serial data transfer clock |
| 113 | DICH2 | - | - | Not used (Open) |
| 114 | LDCH2 | - | - | Not used (Open) |
| 115 | CLKCH2 | - | - | Not used (Open) |
| 116 | HVDD8 | +5V | - | +5V |
| 117 | PF0 | YSNR1-1 | I | Not used |
| 118 | PF1 | CTRCNT2-0 | I | Copy enable signal for copy key card / coin controller |
| 119 | PF2 | CKCTR0-0 | I | Not used |
| 120 | PF3 | KCTRC-0 | I | Key copy counter connection signal (L: connected) |
| 121 | LVSS4 | SG | - | Signal ground |
| 122 | PF4 | YSNR2-1 | I | Not used |
| 123 | PF5 | IPCSW-0 | I | IPC board (finisher controller) connection signal (L: connected) |
| 124 | PF6 | EXTSW-1 | I | Exit sensor detection signal (H: paper transport L: none) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 125 | PF7 | FUSCNT-1 | I | Fuser unit connection signal (L: connected) |
| 126 | HVSS15 | SG | - | Signal ground |
| 127 | PG0 | VCMFNH-0 | O | Exhaust fan high speed drive signal |
| 128 | PG1 | VCMFNL-0 | O | Exhaust fan low speed drive signal<br>VCMFNH-0 VCMFNL-0 Status<br>L L High speed drive<br>L H High speed drive<br>H L Low speed drive<br>H H Stop |
| 129 | PG2 | HTRMODE-1 | O | Fuser unit operation mode signal<br>(H: warming-up, L: normal) |
| 130 | PG3 | GASOL-0 | O | Gate solenoid drive signal for option (H: OFF, L: ON)<br>• Bridge unit (H: to finisher, L: to inner receiving tray)<br>• Job separator (H: to upper tray, L: to lower tray)<br>• Offset tray (H: to ADU pass, L: to OCT pass) |
| 131 | LVDD5 | +3.3V | - | +3.3V |
| 132 | PG4 | OFFSET1 | O | OCT motor control signal [1]<br>* For offset tray |
| 133 | PG5 | OFFSET2 | O | OCT motor control signal [2]<br>* For offset tray<br>OFFSET1 OFFSET2<br>L L OFF<br>L H Paper exit to front side<br>H L Paper exit to rear side<br>H H Break |
| 134 | PG6 | YFAN1H-0 | O | Not used |
| 135 | PG7 | YFAN1L-0 | O | Not used |
| 136 | HVSS16 | SG | - | Signal ground |
| 137 | PH0 | SFBCL1-0 | O | Bypass feed clutch drive signal (H: OFF, L: ON) |
| 138 | PH1 | SFBCL2-0 | O | Bypass pickup solenoid drive signal<br>(H: OFF, L: ON (pickup)) |
| 139 | PH2 | ADUCL-0 | O | ADU clutch drive signal (H: OFF, L: ON) |
| 140 | PH3 | HTR1ON-0 | O | Center heater lamp control signal (H: OFF, L: ON) |
| 141 | HVDD9 | +5V | - | +5V |
| 142 | PH4 | HTR2ON-0 | O | Side heater lamp control signal (H: OFF, L: ON) |
| 143 | PH5 | 2NDCL-0 | O | Lower transport clutch drive signal (H: OFF, L: ON) |
| 144 | PH6 | CURGC-0 | O | Upper drawer feed clutch drive signal<br>(H: OFF, L: ON) |
| 145 | PH7 | CLRGC-0 | O | Lower drawer feed clutch drive signal<br>(H: OFF, L: ON) |
| 146 | HVSS17 | SG | - | Signal ground |
| 147 | PI0 | SFBCNT-1 | I | Bypass unit connection signal (L: connected) |
| 148 | PI1 | SFBEMP-1 | I | Bypass paper sensor detection signal<br>(H: paper absence L: paper presence) |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 149 | PI2 | SFBTRY-1 | I | Not used |
| 150 | PI3 | LCCNT-0 | I | PFP/LCF connection signal (L: connected) |
| 151 | HVSS18 | SG | - | Signal ground |
| 152 | PI4 | SIZE[0] | I | Paper/drawer detection sensor/switch detection signal [0]<br>* Refer to Appendix. [1] |
| 153 | PI5 | SIZE[1] | I | Paper/drawer detection sensor/switch detection signal [1]<br>* Refer to Appendix. [1] |
| 154 | PI6 | SIZE[2] | I | Paper/drawer detection sensor/switch detection signal [2]<br>* Refer to Appendix. [1] |
| 155 | PI7 | SIZE[3] | I | Paper/drawer detection sensor/switch detection signal [3]<br>* Refer to Appendix. [1] |
| 156 | HVSS19 | SG | - | Signal ground |
| 157 | HVDD10 | +5V | - | +5V |
| 158 | DCCLK1 | MAMCK-1 | O | Main motor reference clock |
| 159 | DCCLK2 | HVCLK-1 | O | Not used (Open) |
| 160 | DCCLK3 | - | - | Not used (Open) |
| 161 | DCCLK4 | - | - | Not used (Open) |
| 162 | HVSS20 | SG | - | Signal ground |
| 163 | SM_A | - | - | Not used (Open) |
| 164 | SM_B | - | - | Not used (Open) |
| 165 | SM_NA | - | - | Not used (Open) |
| 166 | SM_NB | - | - | Not used (Open) |
| 167 | HVSS21 | SG | - | Signal ground |
| 168 | SMCLK | - | - | Pull-up: +5V |
| 169 | HVDD11 | +5V | - | +5V |
| 170 | PJ0 | DRV[0] | O | PFP/LCF output signal [0]<br>* Refer to Appendix. [2] |
| 171 | PJ1 | DRV[1] | O | PFP/LCF output signal [1]<br>* Refer to Appendix. [2] |
| 172 | PJ2 | DRV[2] | O | PFP/LCF output signal [2]<br>* Refer to Appendix. [2] |
| 173 | PJ3 | DRV[3] | O | PFP/LCF output signal [3]<br>* Refer to Appendix. [2] |
| 174 | HVSS22 | SG | - | Signal ground |
| 175 | PJ4 | DRV[4] | O | PFP/LCF output signal [4]<br>* Refer to Appendix. [2] |
| 176 | PJ5 | DRV[5] | O | PFP/LCF output signal [5]<br>* Refer to Appendix. [2] |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 177 | PJ6 | DRV[6] | O | PFP/LCF output signal [6]<br>* Refer to Appendix. [2] |
| 178 | PJ7 | DRV[7] | O | PFP/LCF output signal [7]<br>* Refer to Appendix. [2] |
| 179 | HVSS23 | SG | - | Signal ground |
| 180 | MWR | WRRAM-0 | O | Write enable signal for NVRAM (Low-active) |
| 181 | SMINT | - | - | Not used (Open) |
| 182 | LVDD6 | +3.3V | - | +3.3V |
| 183 | CS0 | - | - | Not used (Open) |
| 184 | CS1 | CSRAM-0 | O | Chip select signal [1] (Low-active)<br>* For NVRAM |
| 185 | CS2 | - | - | Not used (Open) |
| 186 | CS3 | CSIPC-0 | O | Chip select signal [3] (Low-active)<br>* For IPC board (finisher controller) |
| 187 | CS4 | - | - | Not used (Open) |
| 188 | CS5 | - | - | Not used (Open) |
| 189 | HVSS24 | SG | - | Signal ground |
| 190 | PK0 | RETS[0] | I | Paper feeding section / PFP / LCF input signal [0]<br>* Refer to Appendix. [3] |
| 191 | PK1 | RETS[1] | I | Paper feeding section / PFP / LCF input signal [1]<br>* Refer to Appendix. [3] |
| 192 | PK2 | RETS[2] | I | Paper feeding section / PFP / LCF input signal [2]<br>* Refer to Appendix. [3] |
| 193 | PK3 | RETS[3] | I | Paper feeding section / PFP / LCF input signal [3]<br>* Refer to Appendix. [3] |
| 194 | LVSS5 | SG | - | Signal ground |
| 195 | PK4 | RETS[4] | I | Paper feeding section / PFP / LCF input signal [4]<br>* Refer to Appendix. [3] |
| 196 | PK5 | RETS[5] | I | Paper feeding section / PFP / LCF input signal [5]<br>* Refer to Appendix. [3] |
| 197 | PK6 | RETS[6] | I | Paper feeding section / PFP / LCF input signal [6]<br>* Refer to Appendix. [3] |
| 198 | PK7 | RETS[7] | I | Paper feeding section / PFP / LCF input signal [7]<br>* Refer to Appendix. [3] |
| 199 | HVDD12 | +5V | - | +5V |
| 200 | MULTD0 | - | - | Pull-up: +5V |
| 201 | MULTD1 | - | I | Upper transport clutch drive request signal input<br>* From pin2 |
| 202 | MULTA | 1STCLL-0 | I | Middle transport clutch drive request signal input<br>* From pin3 |

| Pin No. | Port name | Signal name | I/O | Function |
|---|---|---|---|---|
| 203 | MULTY | 1STCLH-0 | O | Upper transport clutch drive signal (H: OFF, L: ON)<br>* The drive conditions of the upper transport clutch are as follows.<br>Pin201 Pin202 Upper transport clutch<br>L L OFF<br>L H ON |
| 204 | PA0 | SCSWA-0 | O | Paper feeding section bus buffer enable signal [A] (Low-active)<br>* For bypass unit and bridge unit / job separator / offset tray section |
| 205 | PA1 | SCSWB-0 | O | Paper feeding section bus buffer enable signal [B] (Low-active)<br>* For PFP/LCF section |
| 206 | PA2 | SCSWC-0 | O | Paper feeding section bus buffer enable signal [C] (Low-active)<br>* For PFP/LCF section |
| 207 | PA3 | SCSWD-0 | O | Paper feeding section bus buffer enable signal [D] (Low-active)<br>* For ADU and upper/lower drawer section |
| 208 | LVSS6 | SG | - | Signal ground |

## [ 1 ] Description of signals SIZE [0]-[3]

The following functions are assigned to the signals SIZE [0]-[3] depending on each status of SCSWA-D-0 signals.

### [ 1-1 ] When SCSWA-0 = Low:

| Signal name | Function |
|---|---|
| SIZE[0] | Bypass unit slide guide width detection signal [0] (Low-active) |
| SIZE[1] | Bypass unit slide guide width detection signal [1] (Low-active) |
| SIZE[2] | Bypass unit slide guide width detection signal [2] (Low-active) |
| SIZE[3] | Not used |

### [ 1-2 ] When SCSWB-0 = Low:

| Signal name | Function |
|---|---|
| SIZE[0] | PFP upper drawer detection switch detection signal<br>(H: drawer opened, L: drawer closed) |
| SIZE[1] | Not used |
| SIZE[2] | Not used |
| SIZE[3] | Not used |

### [ 1-3 ] When SCSWC-0 = Low:

| Signal name | Function |
|---|---|
| SIZE[0] | PFP lower drawer detection switch detection signal<br>(H: drawer opened, L: drawer closed) |
| SIZE[1] | Not used |
| SIZE[2] | Not used |
| SIZE[3] | Not used |

### [ 1-4 ] When SCSWD-0 = Low:

| Signal name | Function |
|---|---|
| SIZE[0] | ADU entrance sensor detection signal (H: paper transport, L: none) |
| SIZE[1] | ADU exit sensor detection signal (H: paper transport, L: none) |
| SIZE[2] | ADU opening/closing switch detection signal (H: ADU opened L: ADU closed) |
| SIZE[3] | ADU connection signal (L: connected) |

## [ 2 ] Description of signals DRV [0]-[7]

The following functions are assigned to the signals DRV [0]-[7] depending on the installation status of the PFP and LCF. These signals are latched by the up-edge trigger of the CLKB-1 or CLKC-1 signal.

### [ 2-1 ] When CLKB-1 = Up-edge trigger and PFP is installed:

| Signal name | Function |
|---|---|
| DRV[0] | PFP motor drive signal [A] |
| DRV[1] | PFP motor drive signal [B]<br>DRV[1] DRV[0] Status<br>L L Break<br>L H ON<br>H L Not used<br>H H OFF |
| DRV[2] | Not used |
| DRV[3] | Not used |
| DRV[4] | PFP upper drawer feed clutch drive signal (H: OFF, L: ON) |
| DRV[5] | PFP lower drawer feed clutch drive signal (H: OFF, L: ON) |
| DRV[6] | PFP transport clutch drive signal (H: OFF, L: ON) |
| DRV[7] | Not used |

### [ 2-2 ] When CLKB-1 = Up-edge trigger and LCF is installed:

| Signal name | Function |
|---|---|
| DRV[0] | LCF transport motor drive signal (H: ON) |
| DRV[1] | LCF transport motor speed switch signal (H: low speed drive, L: high speed drive) |
| DRV[2] | LCF transport clutch drive signal (H: OFF, L: ON) |
| DRV[3] | LCF feed clutch drive signal (H: OFF, L: ON) |
| DRV[4] | LCF pickup solenoid drive signal (H: OFF, L: ON) |
| DRV[5] | Not used |
| DRV[6] | Not used |
| DRV[7] | Not used |

### [ 2-3 ] When CLKC-1 = Up-edge trigger and PFP is installed:

| Signal name | Function |
|---|---|
| DRV[0] | PFP upper drawer tray-up motor drive signal [A] |
| DRV[1] | PFP upper drawer tray-up motor drive signal [B]<br>DRV[1] DRV[0] Status<br>L L OFF<br>L H Up<br>H L Down<br>H H Break |
| DRV[2] | PFP lower drawer tray-up motor drive signal [A] |
| DRV[3] | PFP lower drawer tray-up motor drive signal [B]<br>DRV[3] DRV[2] Status<br>L L OFF<br>L H Up<br>H L Down<br>H H Break |
| DRV[4] | Not used |
| DRV[5] | Not used |
| DRV[6] | Not used |
| DRV[7] | Not used |

### [ 2-4 ] When CLKC-1 = Up-edge trigger and LCF is installed:

| Signal name | Function |
|---|---|
| DRV[0] | LCF tray-up motor drive signal [A] |
| DRV[1] | LCF tray-up motor drive signal [B]<br>DRV[1] DRV[0] Status<br>L L OFF<br>L H Up<br>H L Down<br>H H Break |
| DRV[2] | LCF end fence motor drive signal [A] |
| DRV[3] | LCF end fence motor drive signal [B]<br>DRV[3] DRV[2] Status<br>L L OFF<br>L H Transfer<br>H L Reverse<br>H H Break |
| DRV[4] | LCF end fence solenoid drive signal (H: OFF, L: ON) |
| DRV[5] | Not used |
| DRV[6] | Not used |
| DRV[7] | Not used |

## [ 3 ] Description of signals RETS [0]-[7]

The following functions are assigned to the signals RETS [0]-[7] depending on each status of the signals SCSWA-D-0 and installation status of the PFP and LCF.

### [ 3-1 ] When SCSWA-0 = Low:

| Signal name | Function |
|---|---|
| RETS[0] | Sensor detection signal for option<br>• Bridge unit: paper full detection sensor detection signal (H: normal, L: full)<br>• Job separator: JSP stack sensor (lower) detection signal (H: full, L: normal)<br>• Offset tray: OCT stack sensor detection signal (H: full, L: normal) |
| RETS[1] | Option detection signal (H: offset tray, L: job separator or bridge unit) |
| RETS[2] | Cover opening/closing sensor detection signal for option<br>• Bridge unit: transport cover opening/closing sensor detection signal (H: opened, L: closed)<br>• Job separator: JSP cover switch detection signal (H: opened, L: closed)<br>• Offset tray: OCT cover switch detection signal (H: opened, L: closed) |
| RETS[3] | Sensor detection signal for option<br>• Bridge unit: bridge unit transport sensor-2 (exit side) detection signal (H: paper transport, L: none)<br>• Job separator: JSP feed sensor detection signal (H: paper transport, L: none) |
| RETS[4] | Sensor detection signal for option<br>• Bridge unit: bridge unit transport sensor-1 (entrance side) detection signal (H: paper transport, L: none)<br>• Offset tray: OCT feed sensor detection signal (H: paper transport, L: none) |
| RETS[5] | Option detection signal (H: bridge unit, L: job separator or offset tray) |
| RETS[6] | Sensor detection signal for option<br>• Job separator: JSP stack sensor (upper) detection signal (H: full, L: normal)<br>• Offset tray: OCT separate sensor detection signal (H: home position) |
| RETS[7] | Bridge unit / job separator / offset tray connection signal (L: connected) |

* The relations between the connection status of options (Bridge Unit, Job Separator and Offset Tray) and RETS signals ([1], [4] and [7]) are as follows.

| RETS[1] | RETS[4] | RETS[7] | Options to connect |
|---|---|---|---|
| L | L | L | Job Separator |
| L | H | L | Bridge Unit |
| H | H | L | Offset Tray |
| - | - | H | None |

### [ 3-2 ] When SCSWB-0 = Low and PFP is installed:

| Signal name | Function |
|---|---|
| RETS[0] | PFP upper drawer tray-up sensor detection signal (H: top position, L: normal) |
| RETS[1] | PFP upper drawer empty sensor detection signal (H: paper presence, L: paper absence) |
| RETS[2] | PFP side cover opening/closing switch detection signal (H: opened L: closed) |
| RETS[3] | PFP connection signal (L: connected) |
| RETS[4] | PFP upper drawer feed sensor detection signal (H: paper transport, L: none) |
| RETS[5] | PFP upper drawer paper stock sensor detection signal<br>(H: paper absence L: paper presence) |
| RETS[6] | Not used |
| RETS[7] | Not used |

### [ 3-3 ] When SCSWB-0 = Low and LCF is installed:

| Signal name | Function |
|---|---|
| RETS[0] | LCF feeding side paper stock sensor detection signal<br>(H: paper presence L: paper absence) |
| RETS[1] | Not used |
| RETS[2] | Not used |
| RETS[3] | Not used |
| RETS[4] | Not used |
| RETS[5] | Not used |
| RETS[6] | LCF feeding side paper mis-stacking sensor detection signal<br>(H: lever to detect mis-stacking is opened) |
| RETS[7] | LCF tray bottom sensor detection signal (H: bottom position, L: normal) |

### [ 3-4 ] When SCSWC-0 = Low and PFP is installed:

| Signal name | Function |
|---|---|
| RETS[0] | PFP lower drawer tray-up sensor detection signal (H: top position, L: normal) |
| RETS[1] | PFP lower drawer empty sensor detection signal (H: paper presence, L: paper absence) |
| RETS[2] | Not used |
| RETS[3] | PFP motor phase locked loop control signal (H: stop or error, L: uniform speed driving) |
| RETS[4] | PFP lower drawer feed sensor detection signal (H: paper transport, L: none) |
| RETS[5] | PFP lower drawer paper stock sensor detection signal<br>(H: paper absence L: paper presence) |
| RETS[6] | Not used |
| RETS[7] | Not used |

### [ 3-5 ] When SCSWC-0 = Low and LCF is installed:

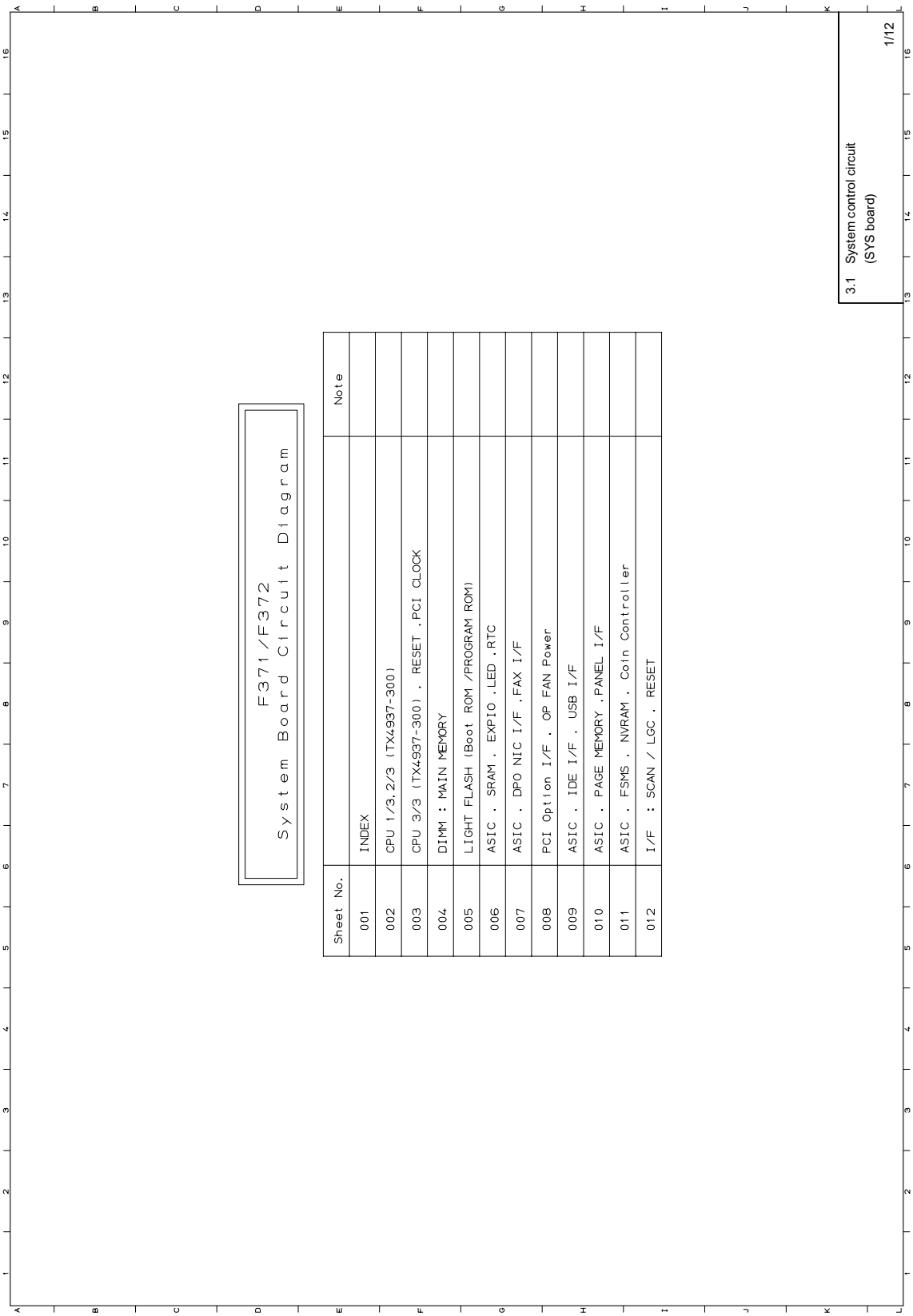
| Signal name | Function |
|---|---|
| RETS[0] | LCF feeding side paper empty sensor detection signal<br>(H: paper presence L: paper absence) |
| RETS[1] | LCF drawer feed sensor detection signal (H: none, L: paper transport) |
| RETS[2] | LCF tray-up sensor detection signal (H: top position, L: normal) |
| RETS[3] | LCF transport motor LD signal (H: stop, L: rotation) |
| RETS[4] | LCF side cover opening/closing switch detection signal (H: closed L: opened) |
| RETS[5] | LCF standby side paper empty sensor detection signal<br>(H: paper absence L: paper presence) |
| RETS[6] | LCF end fence stop position sensor detection signal (H: stop position) |
| RETS[7] | LCF end fence home position sensor detection signal (H: home position) |

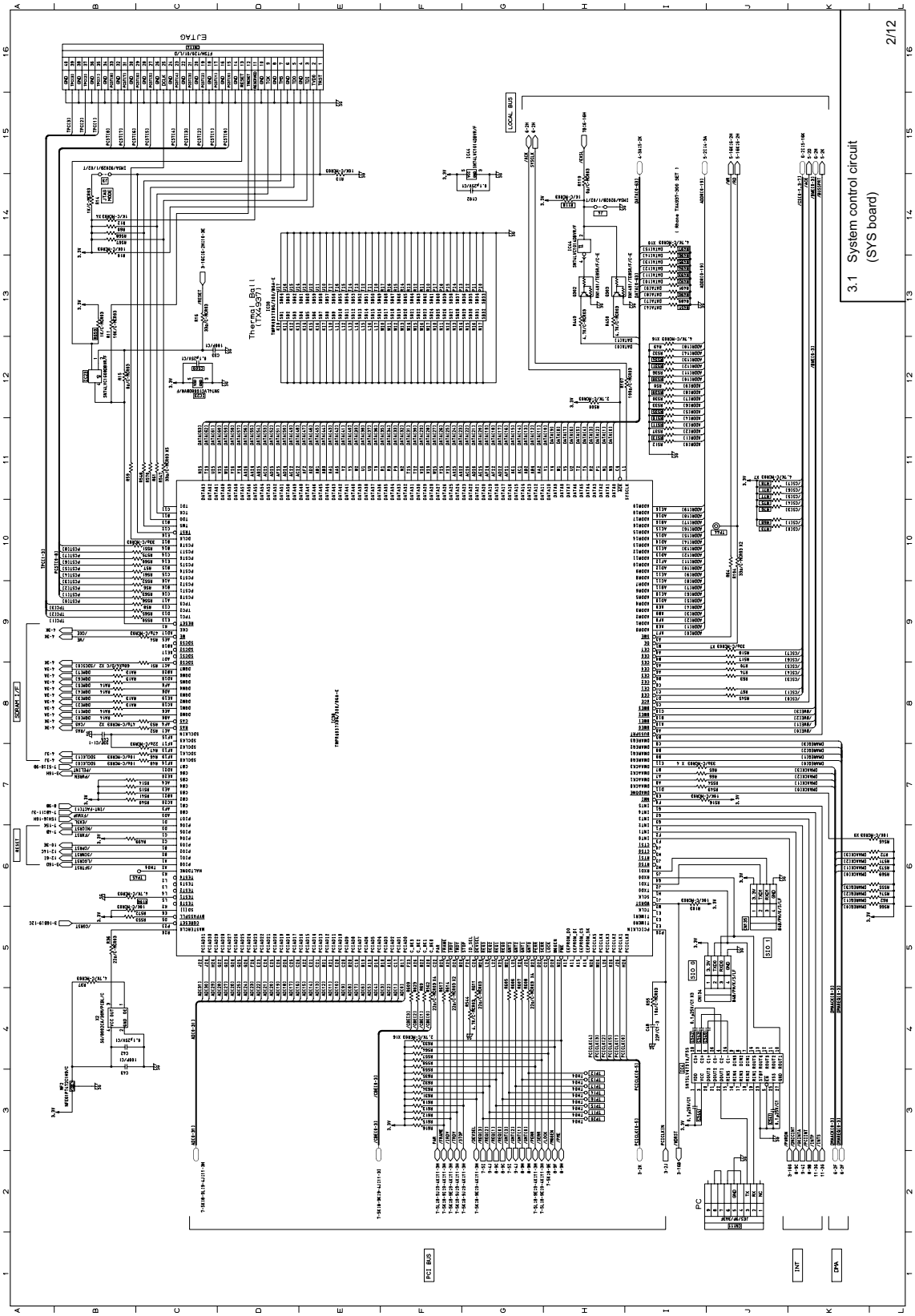
### [ 3-6 ] When SCSWD-0 = Low:

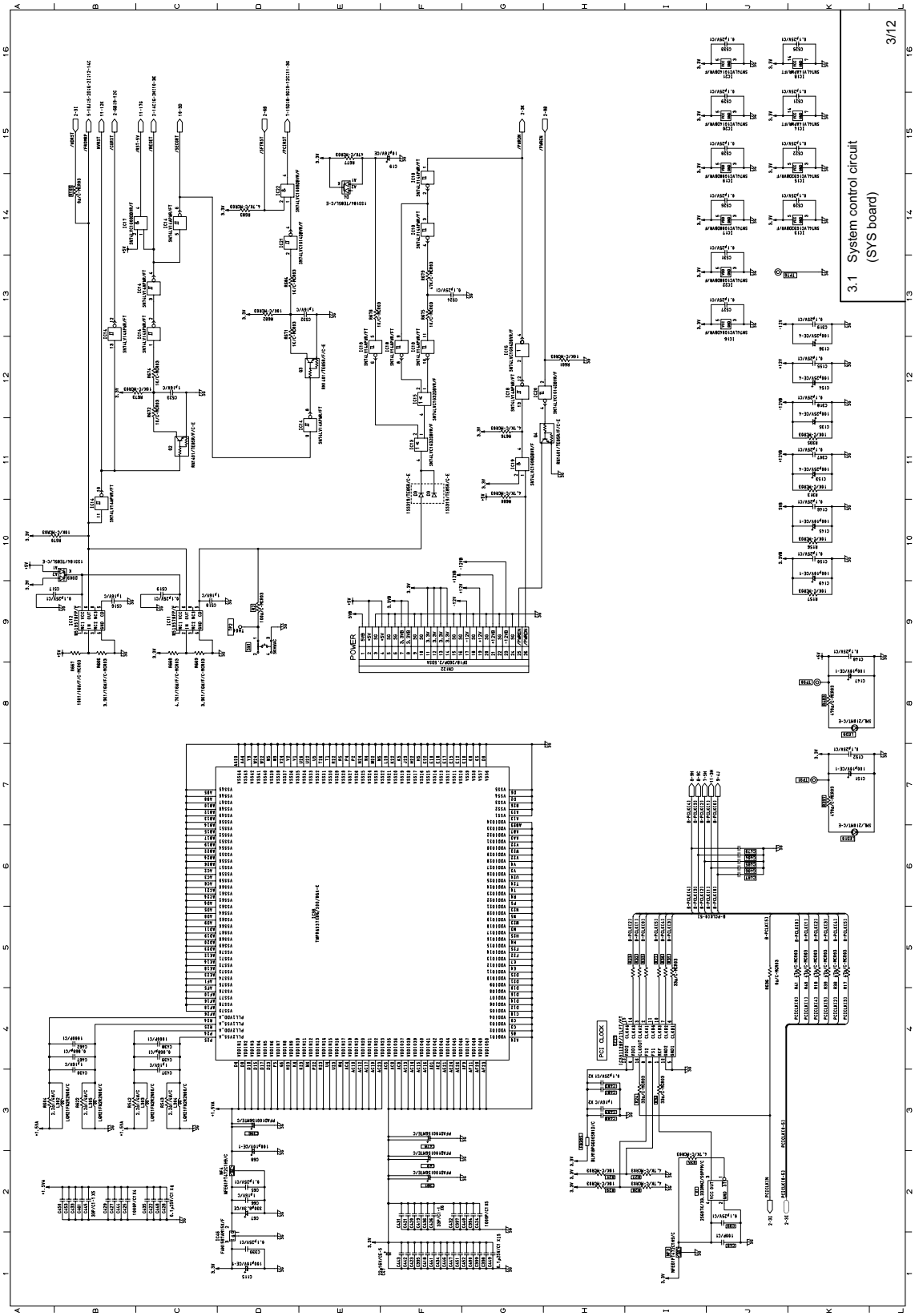
| Signal name | Function |
|---|---|
| RETS[0] | Upper drawer tray-up sensor detection signal (H: top position, L: normal) |
| RETS[1] | Upper drawer empty sensor detection signal (H: paper presence, L: paper absence) |
| RETS[2] | Upper drawer paper stock sensor detection signal (H: paper absence, L: paper presence) |
| RETS[3] | Upper drawer detection switch detection signal (H: drawer opened, L: drawer closed) |
| RETS[4] | Lower drawer tray-up sensor detection signal (H: top position, L: normal) |
| RETS[5] | Lower drawer empty sensor detection signal (H: paper presence, L: paper absence) |
| RETS[6] | Lower drawer paper stock sensor detection signal (H: paper absence, L: paper presence) |
| RETS[7] | Lower drawer detection switch detection signal (H: drawer opened, L: drawer closed) |

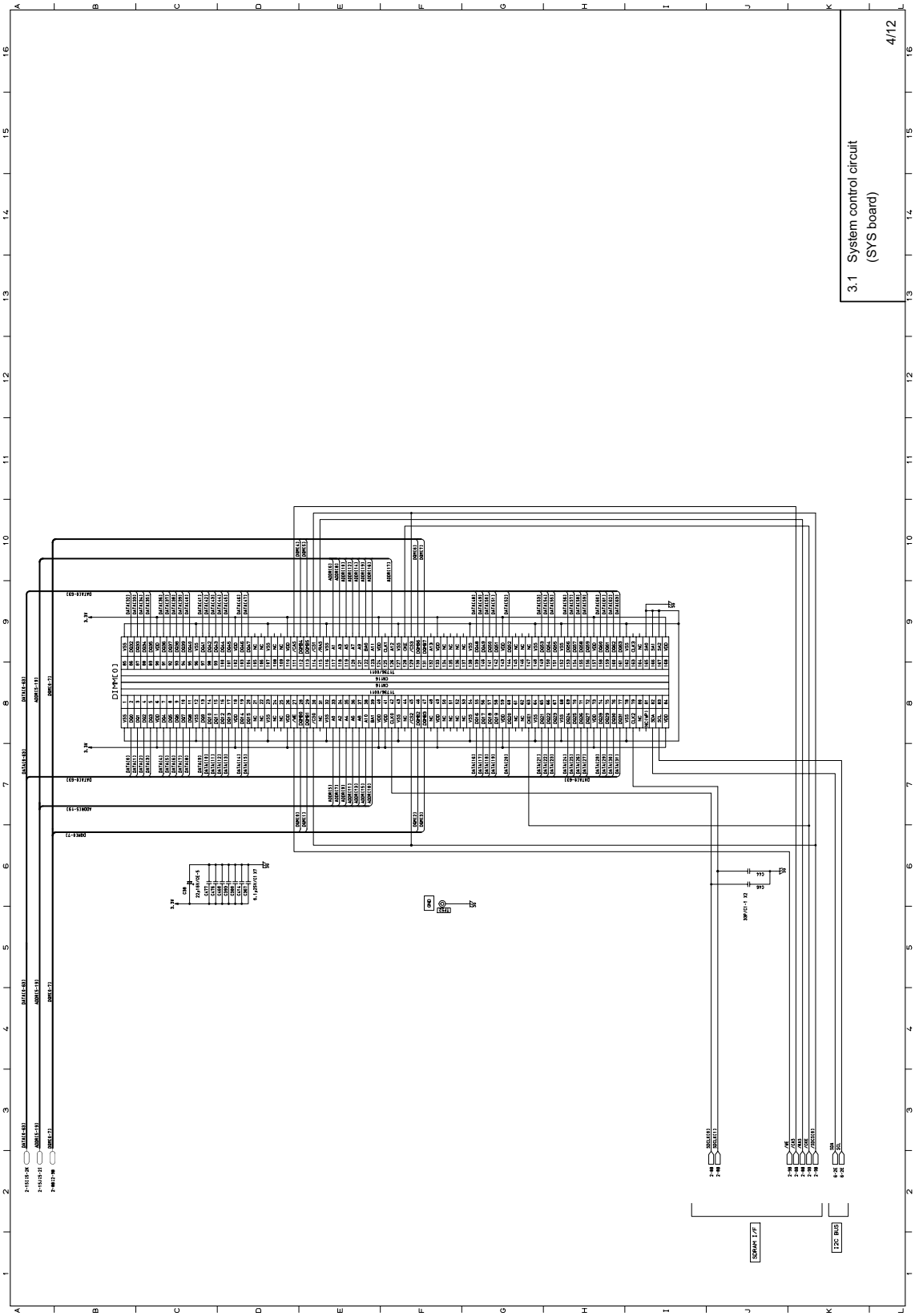
# 3. ELECTRIC CIRCUIT DIAGRAMS

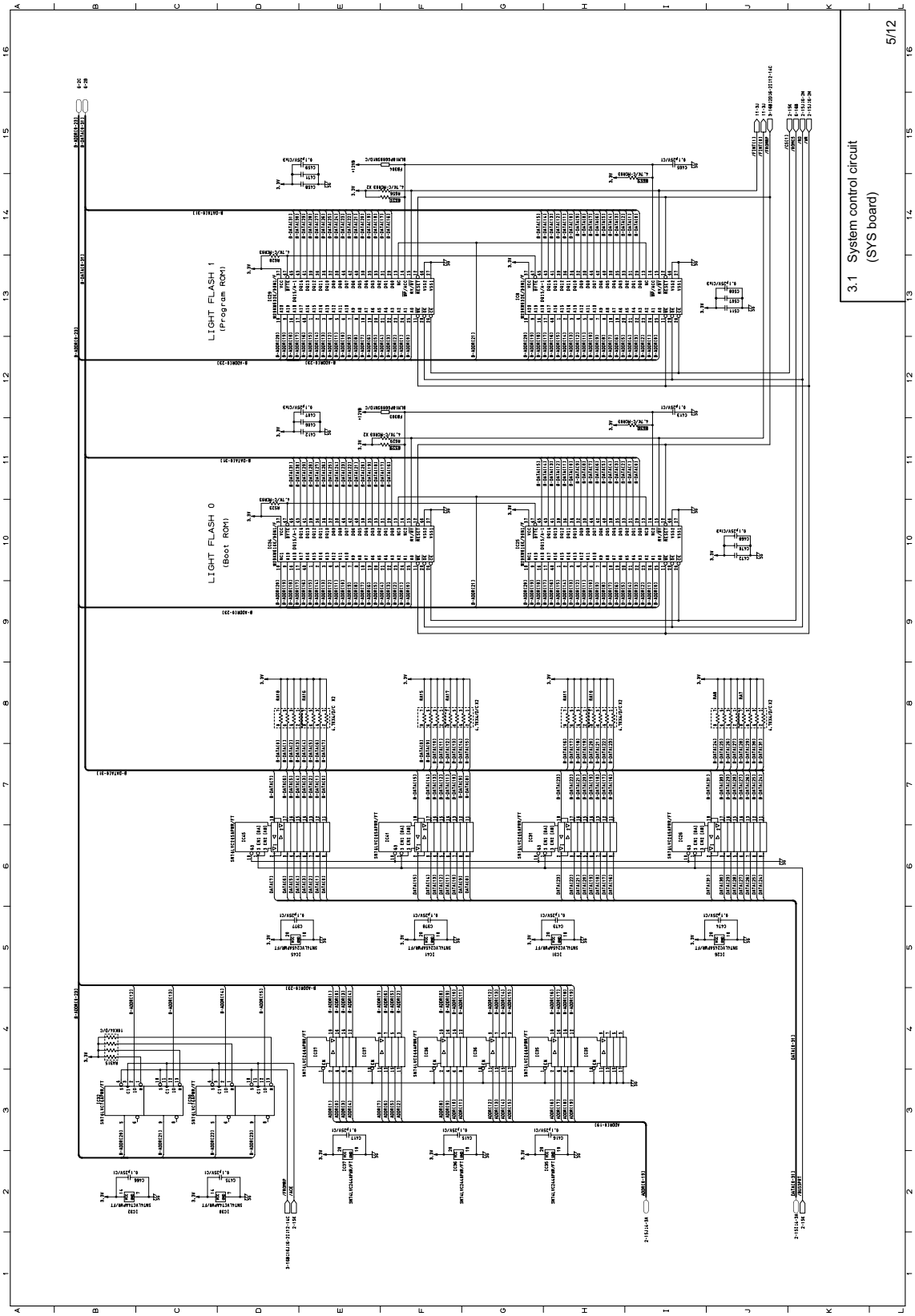
# 3.1 System control circuit (SYS board)

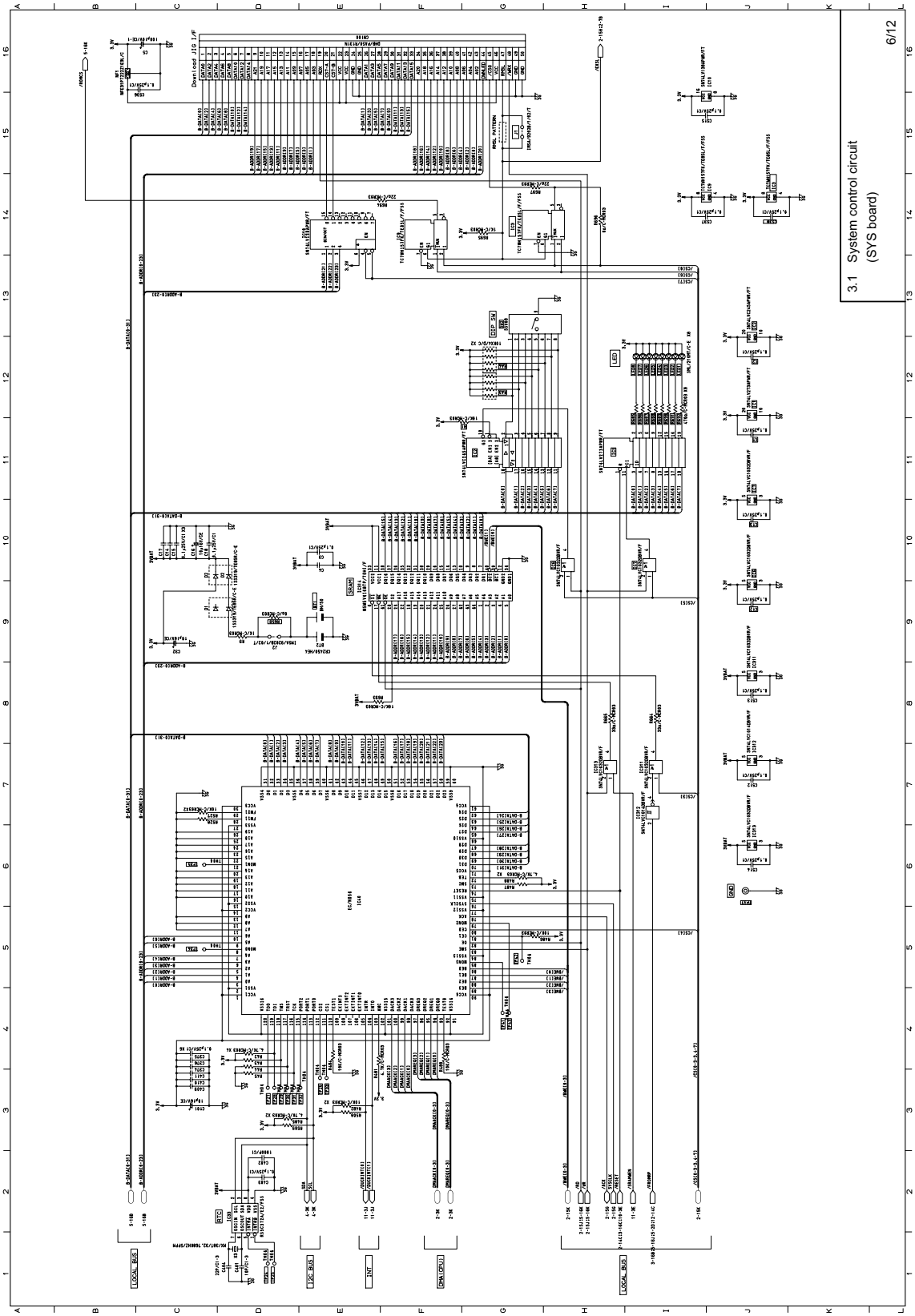


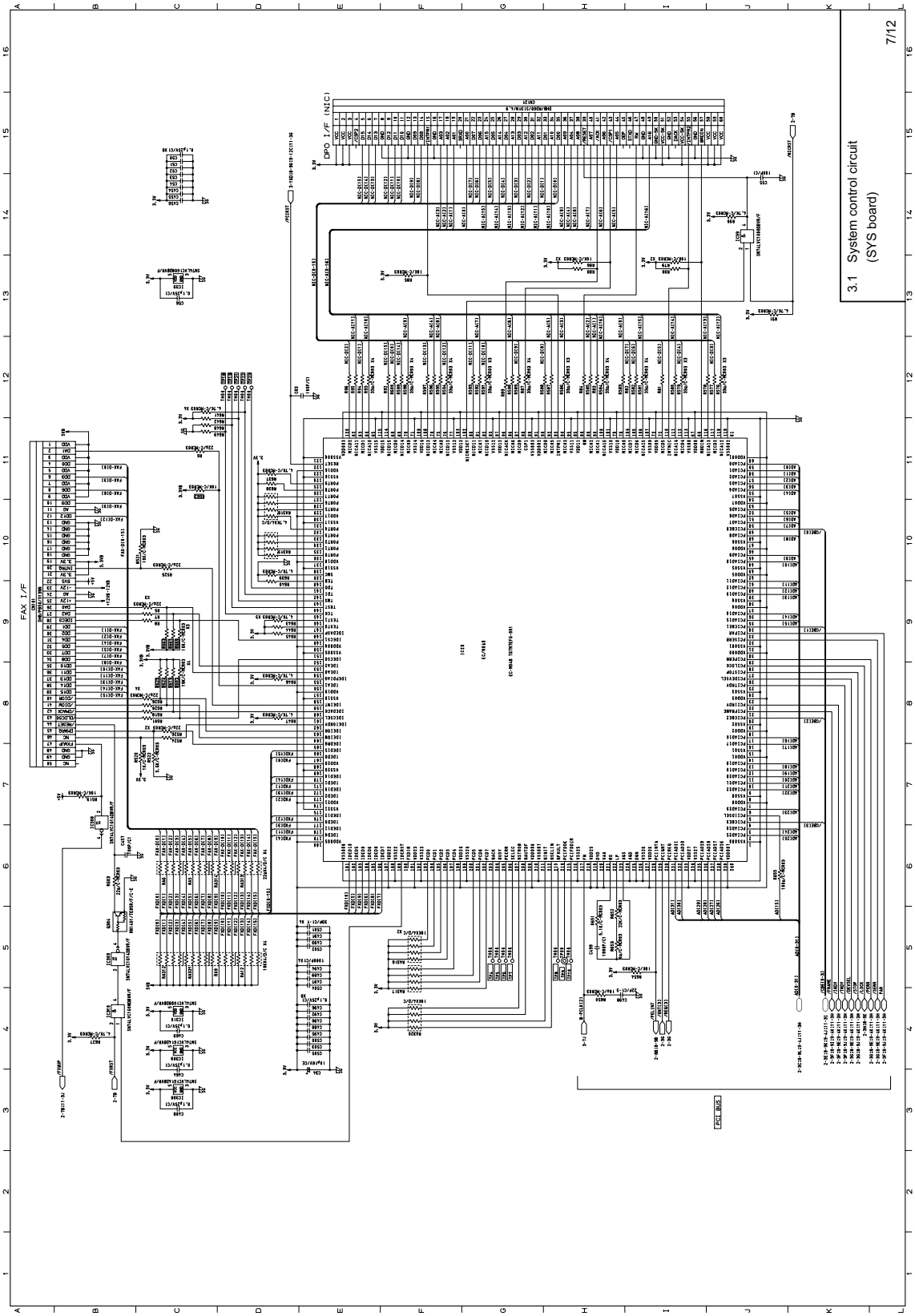


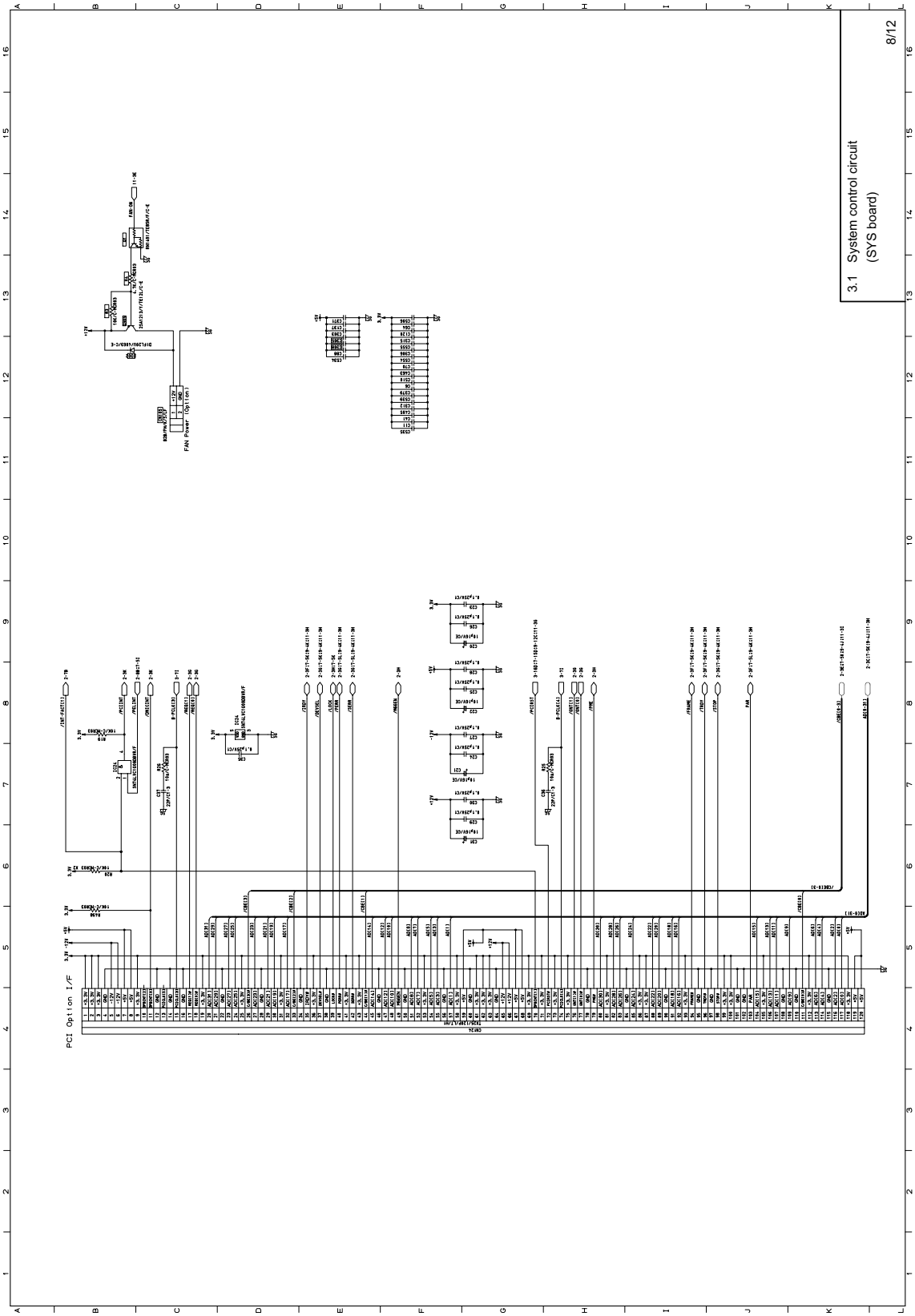


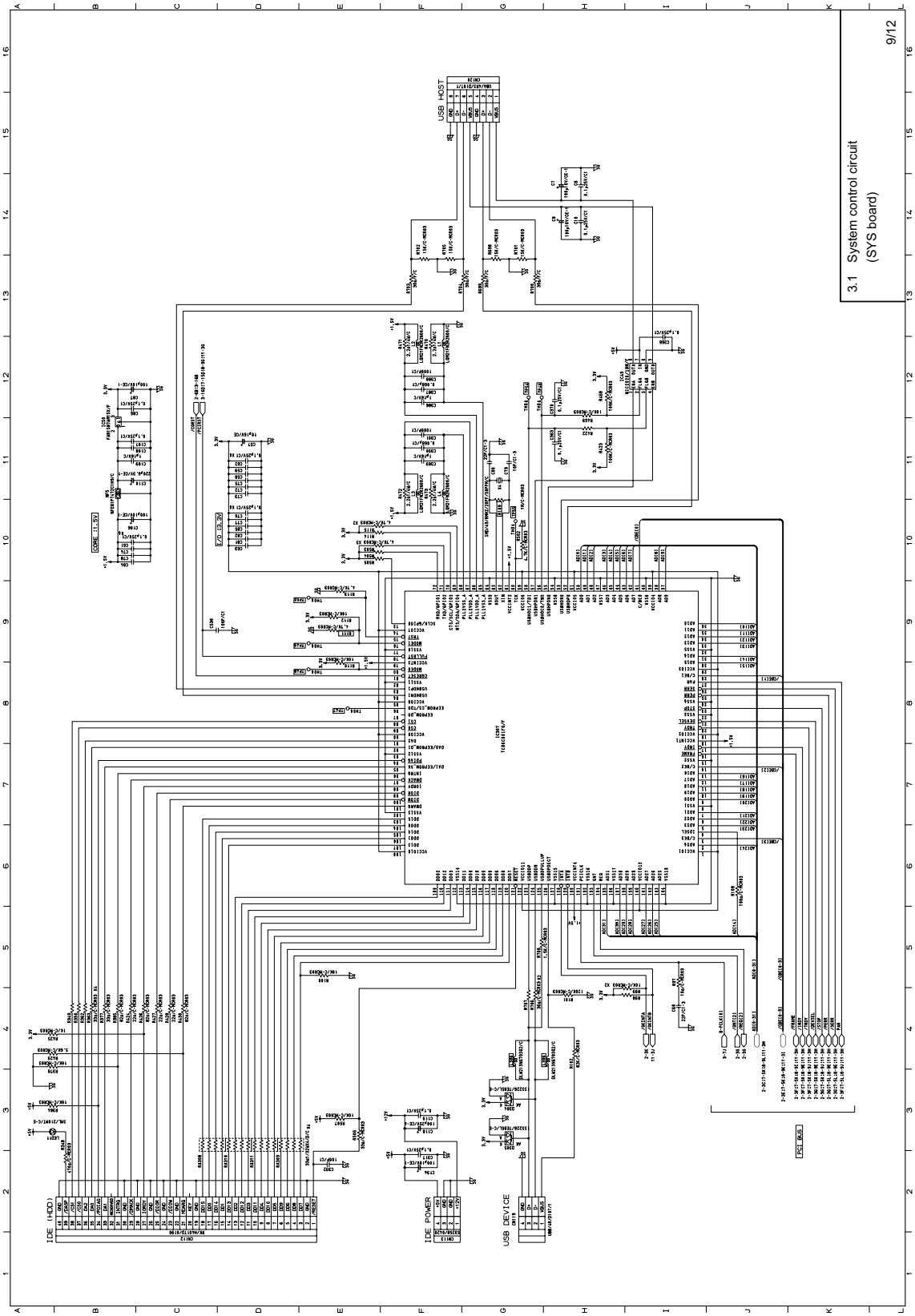


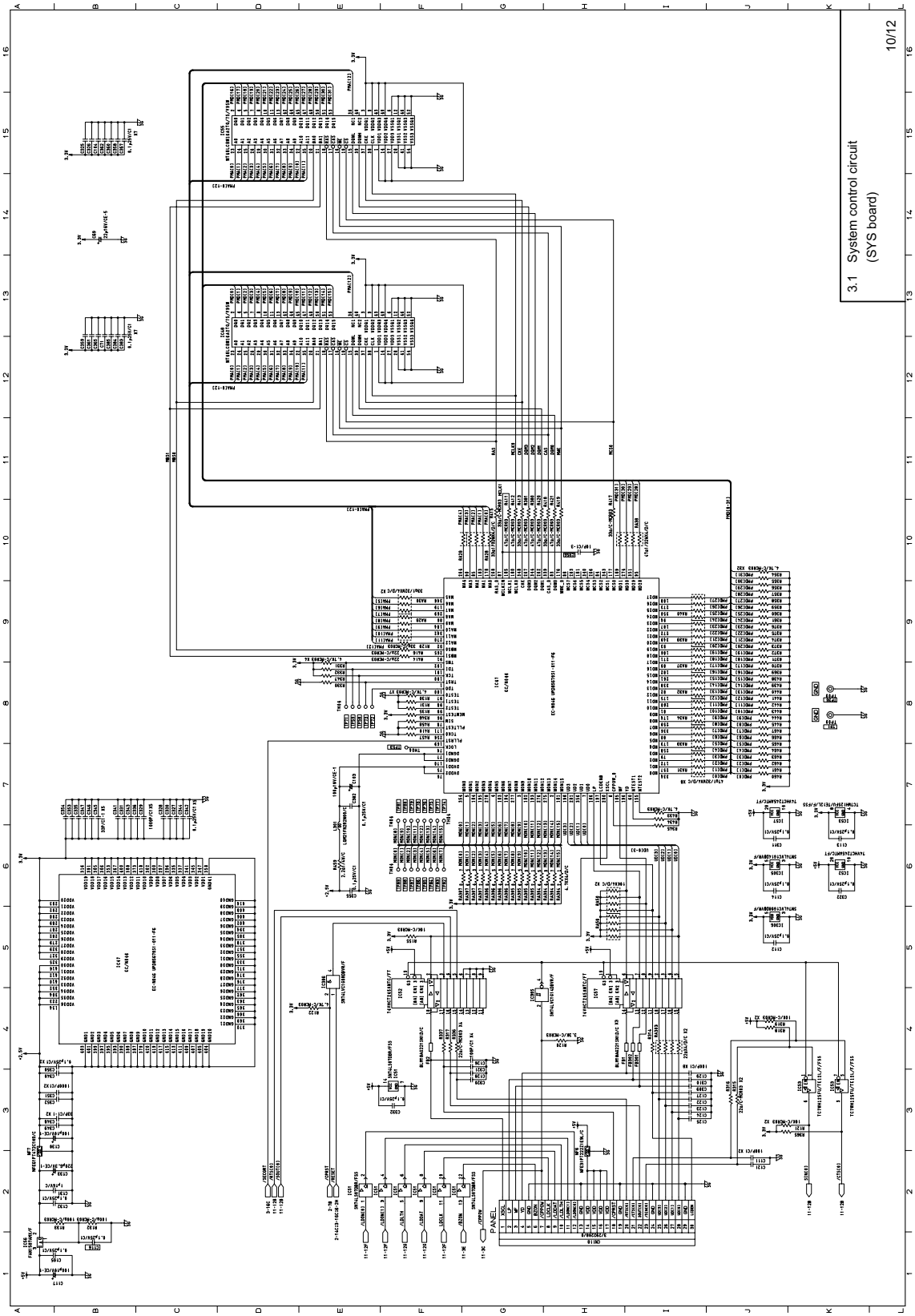


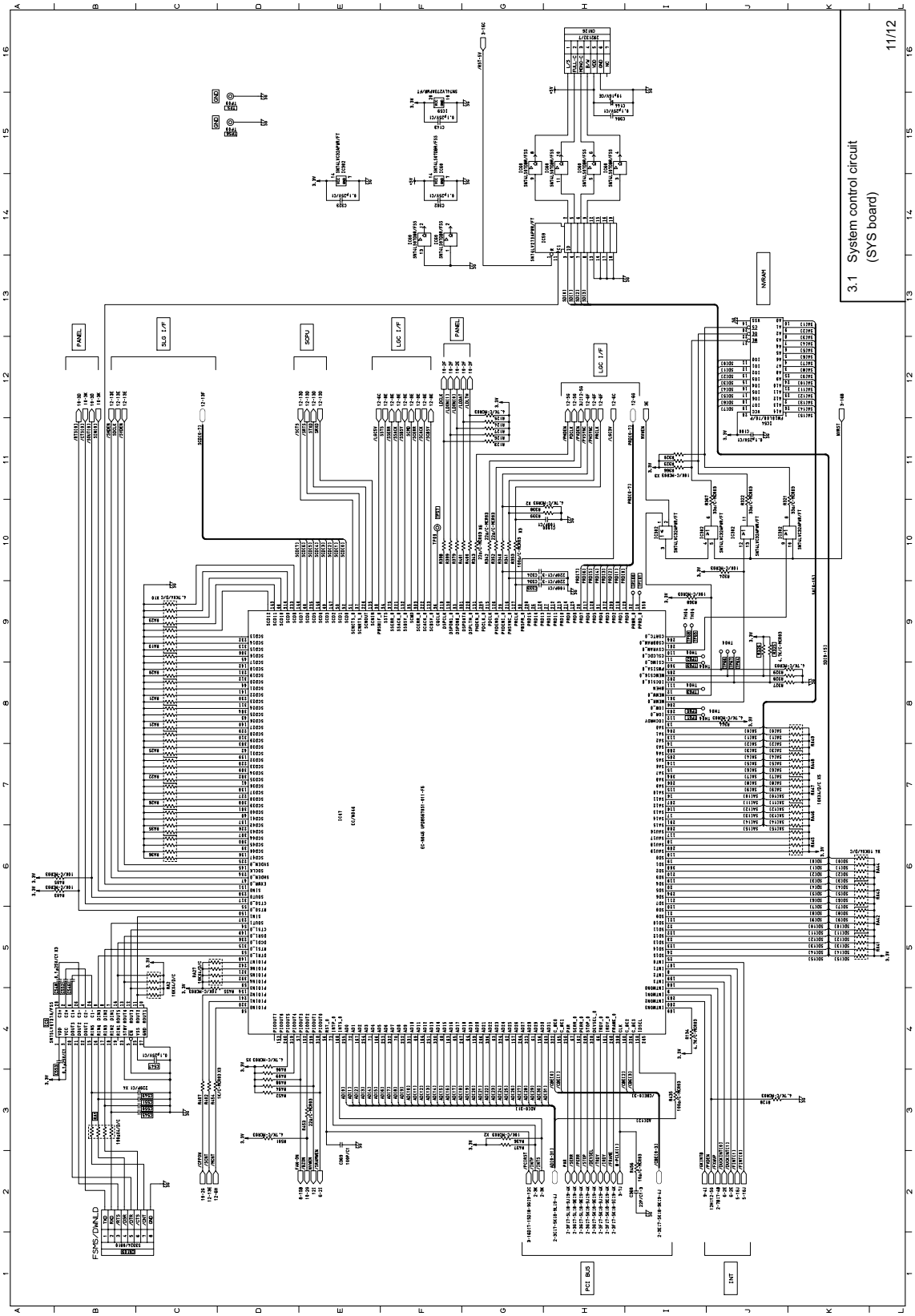


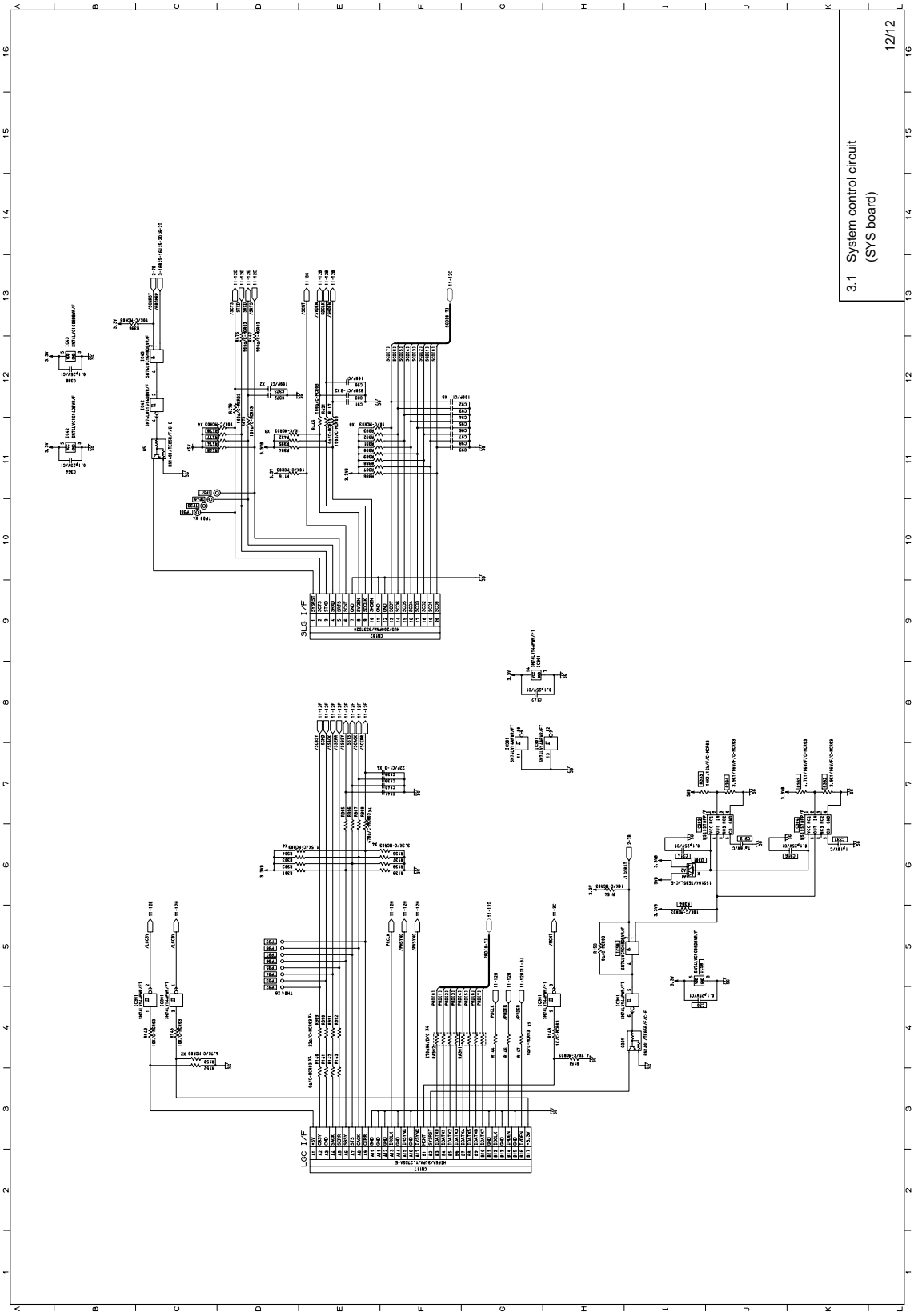




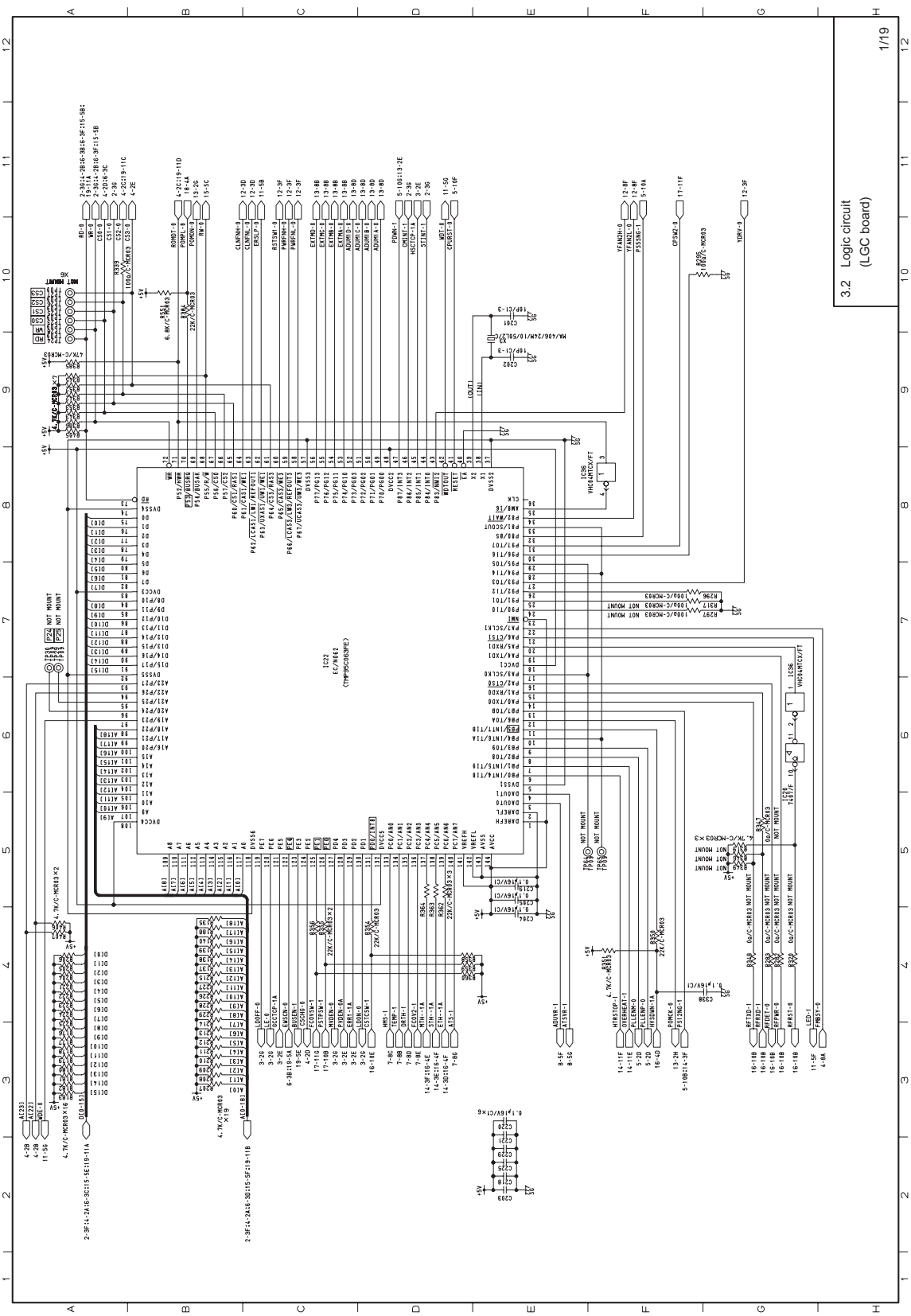


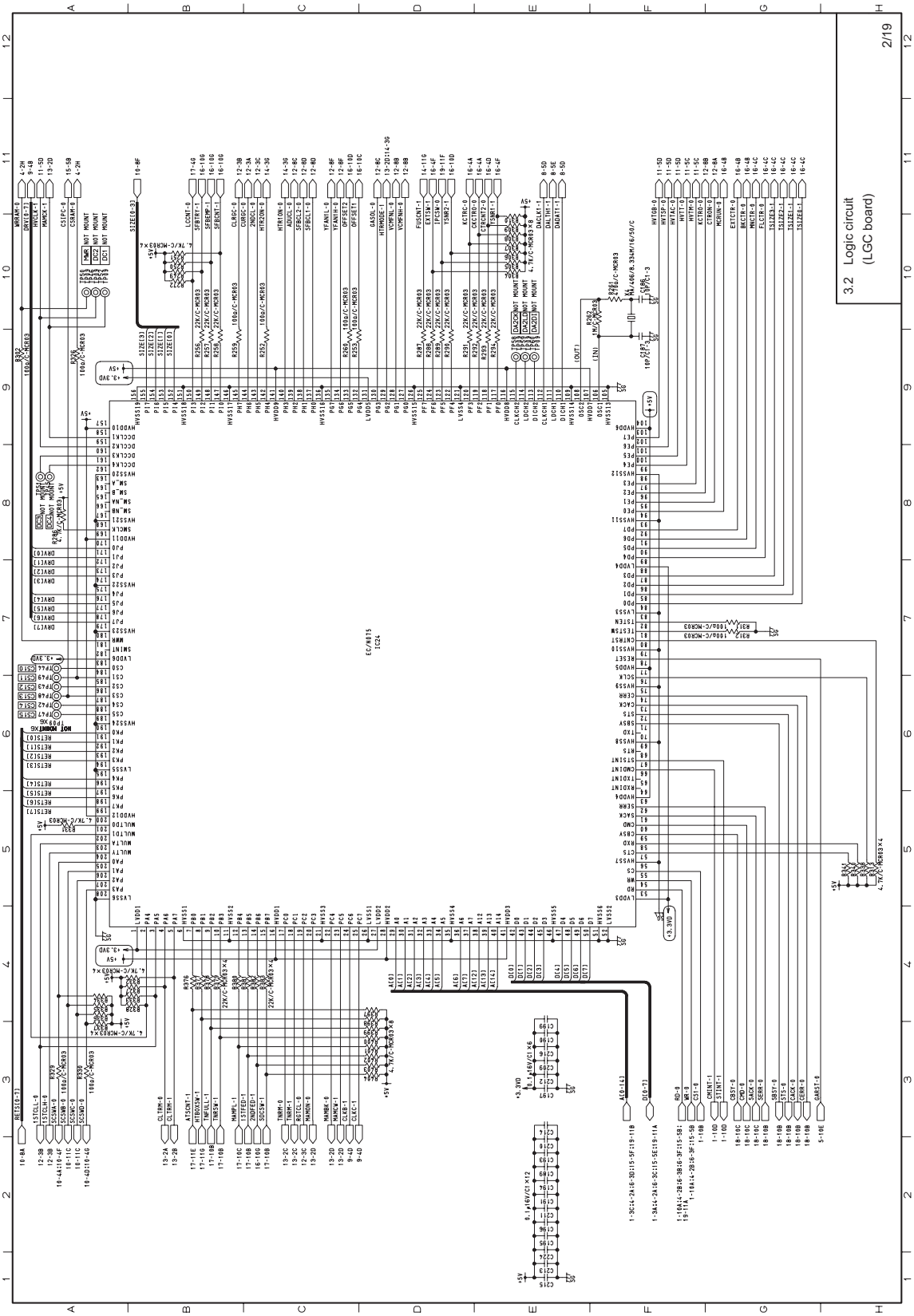


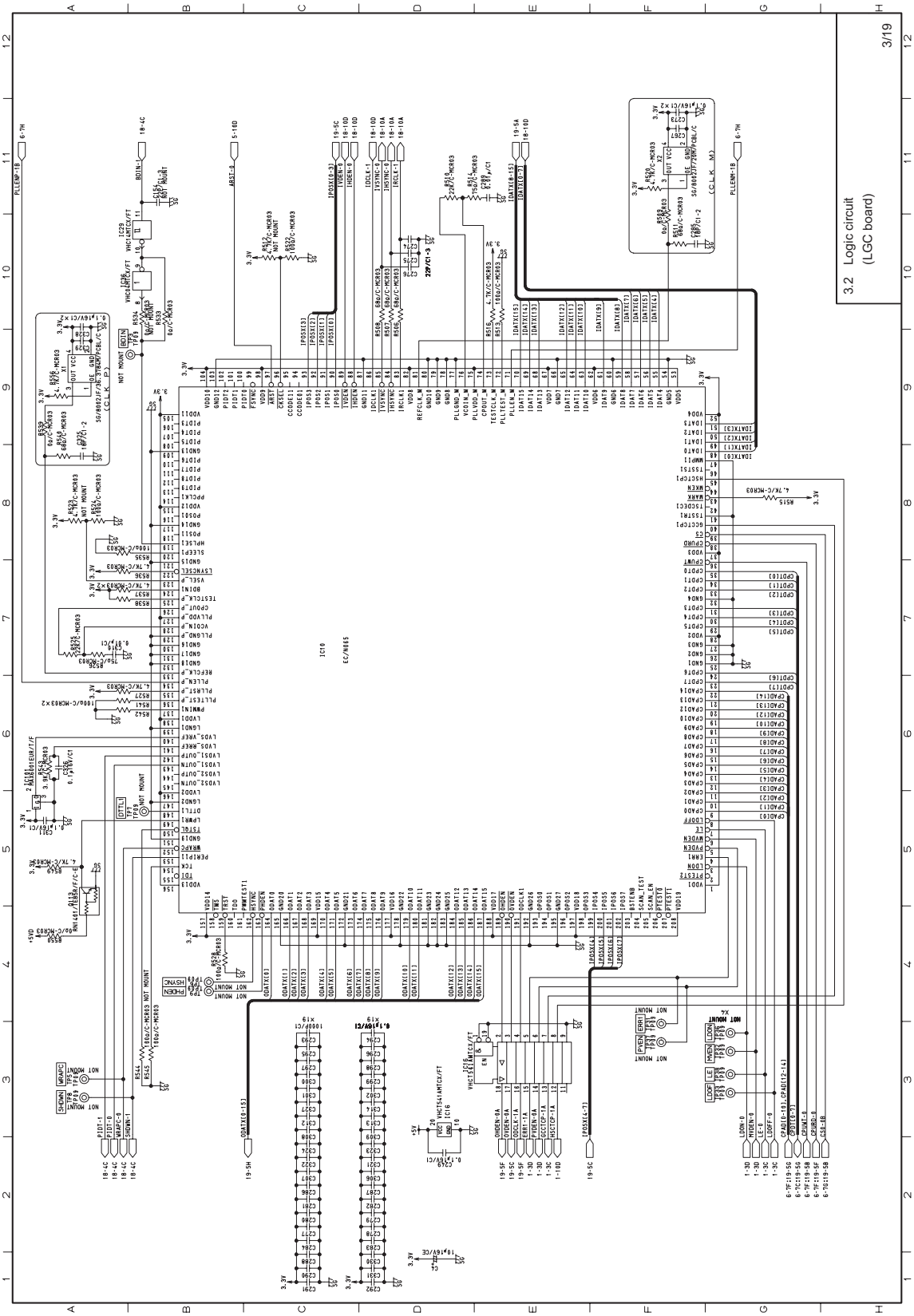


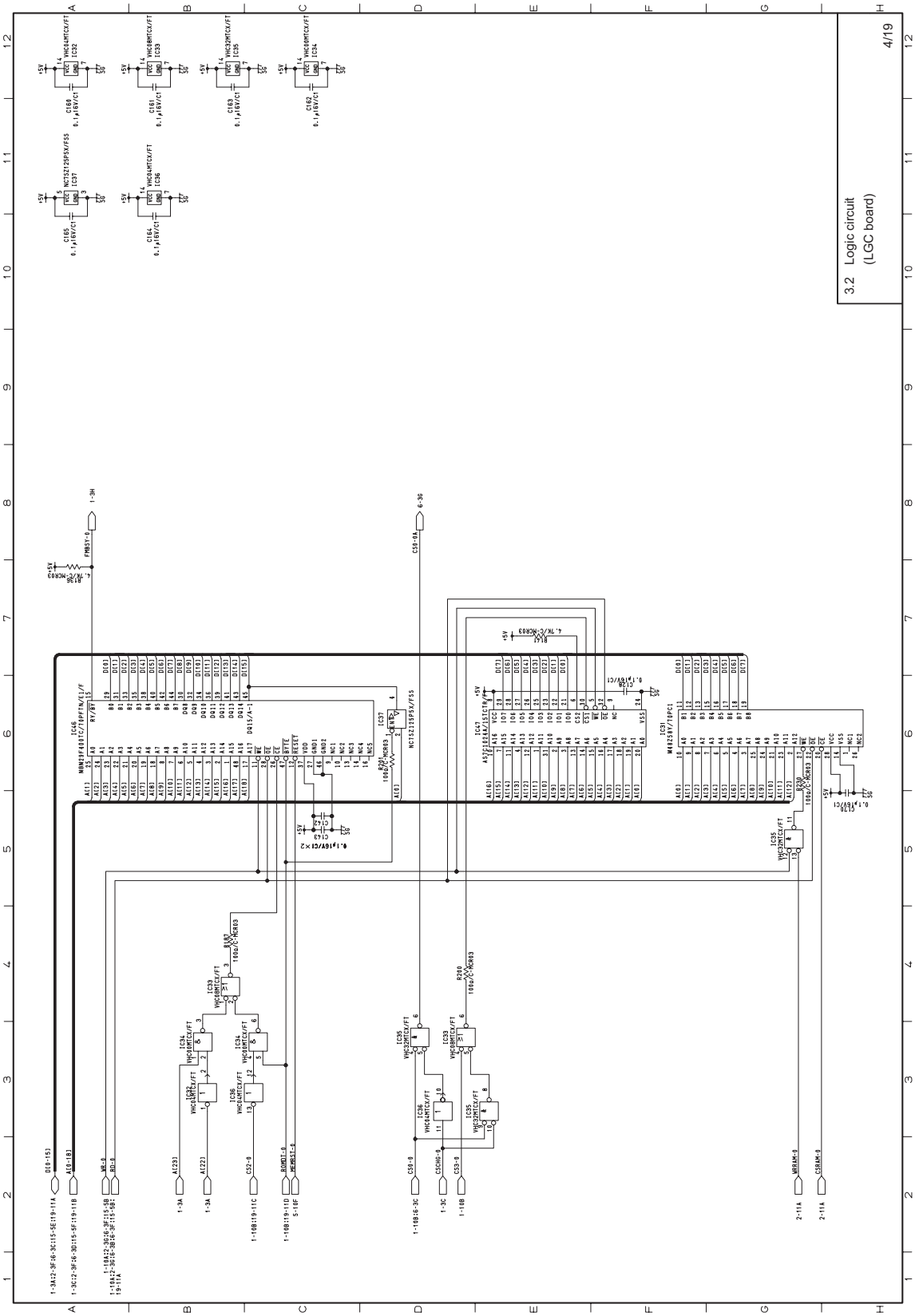


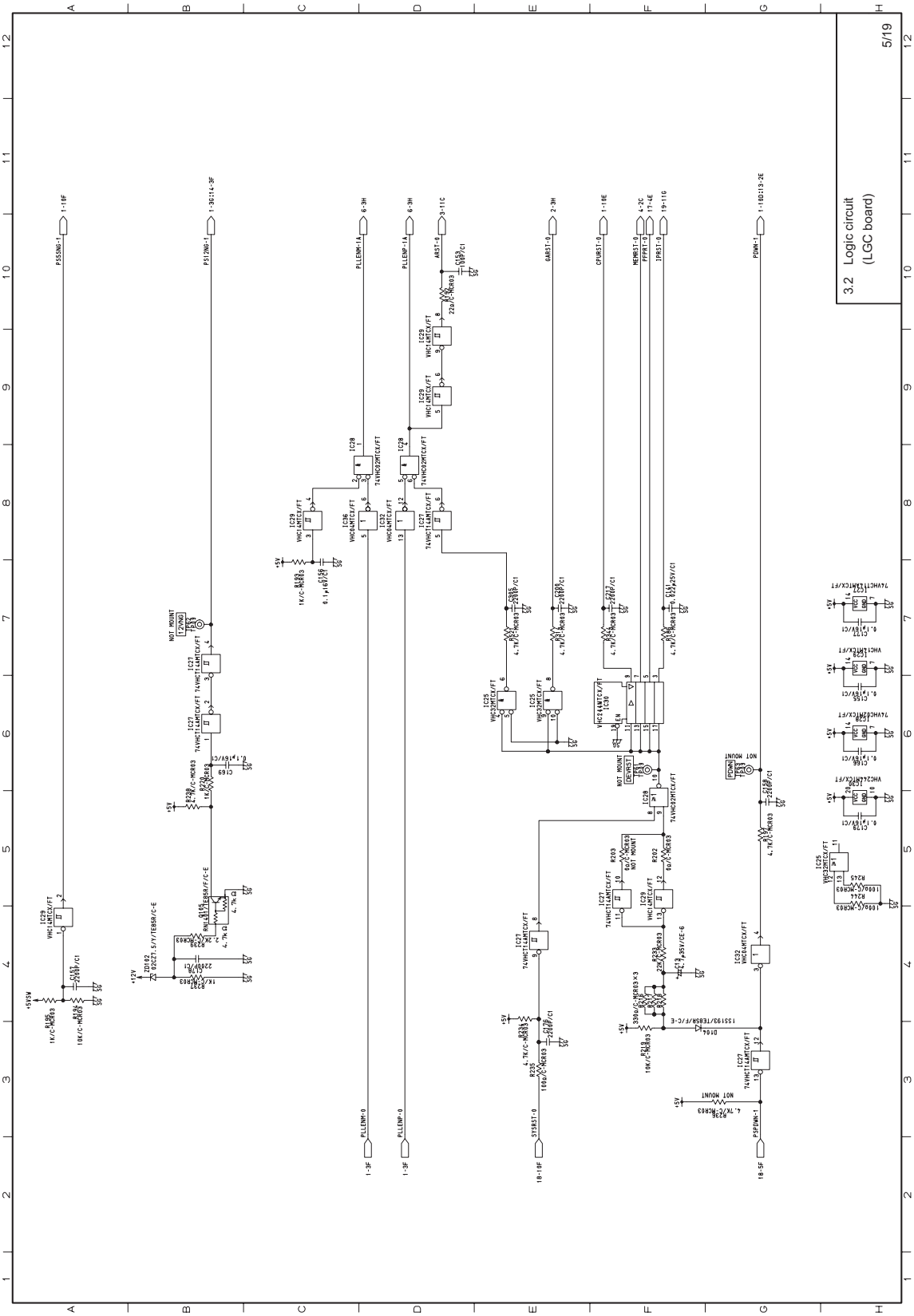
# 3.2 Logic circuit (LGC board)

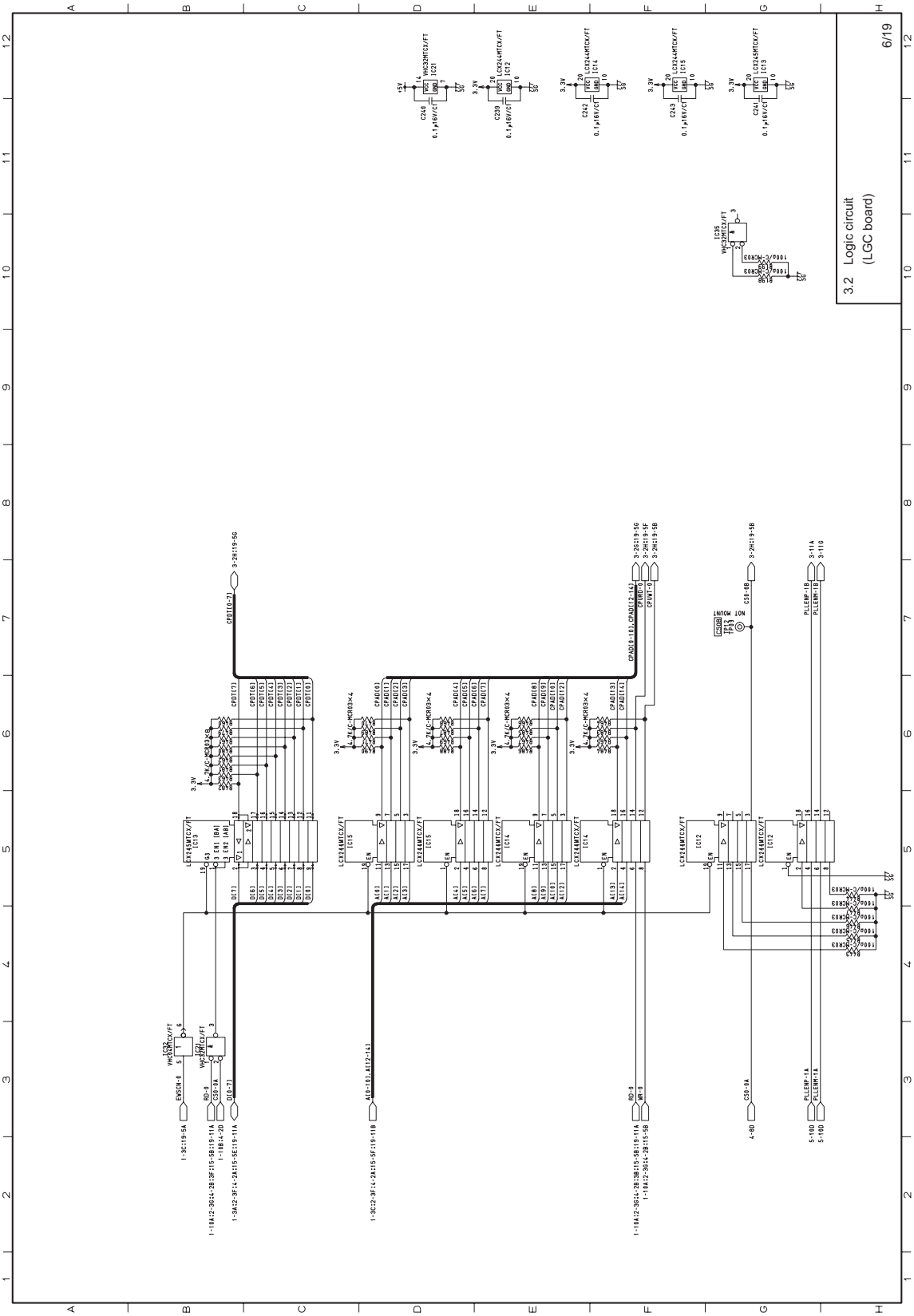


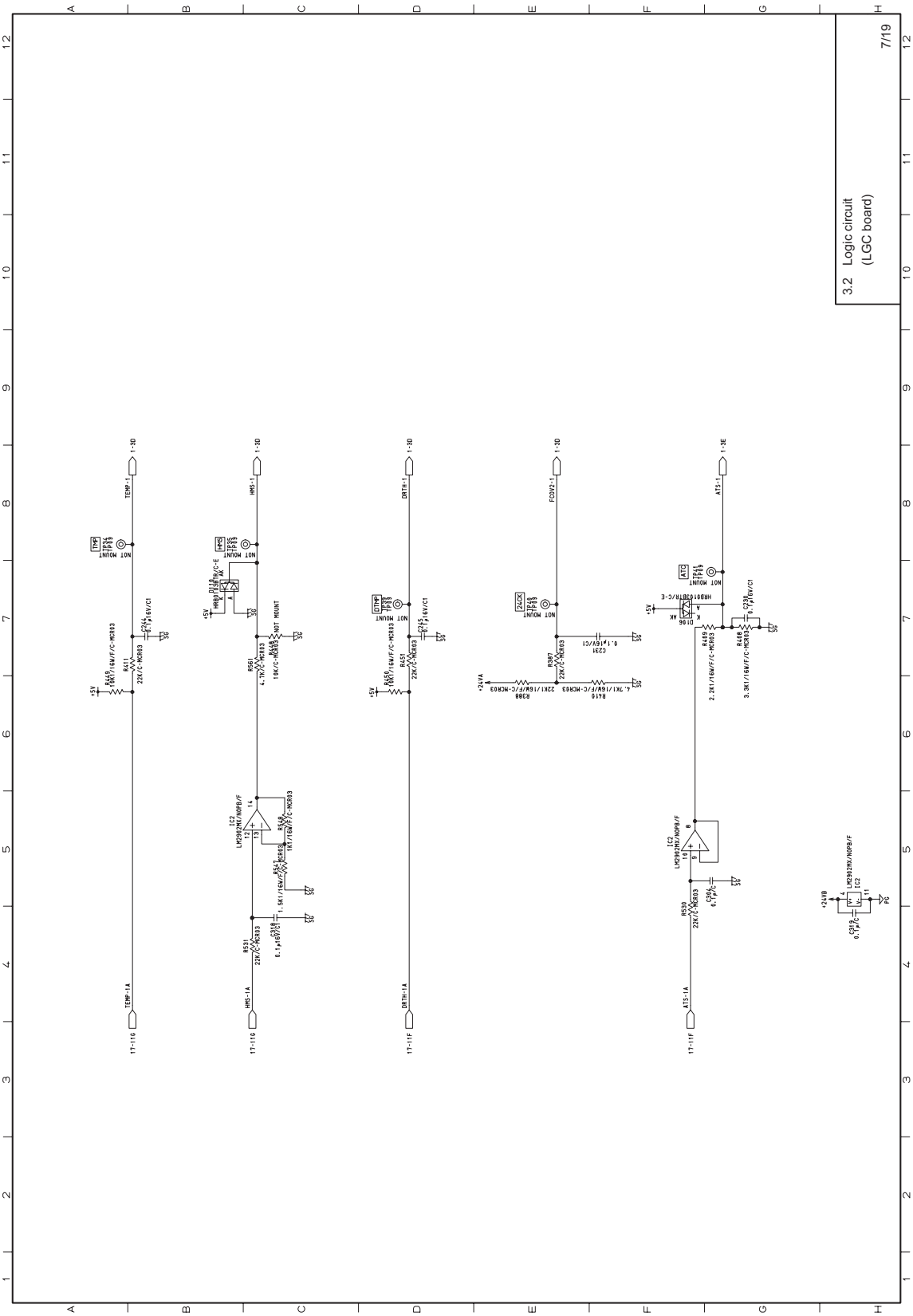


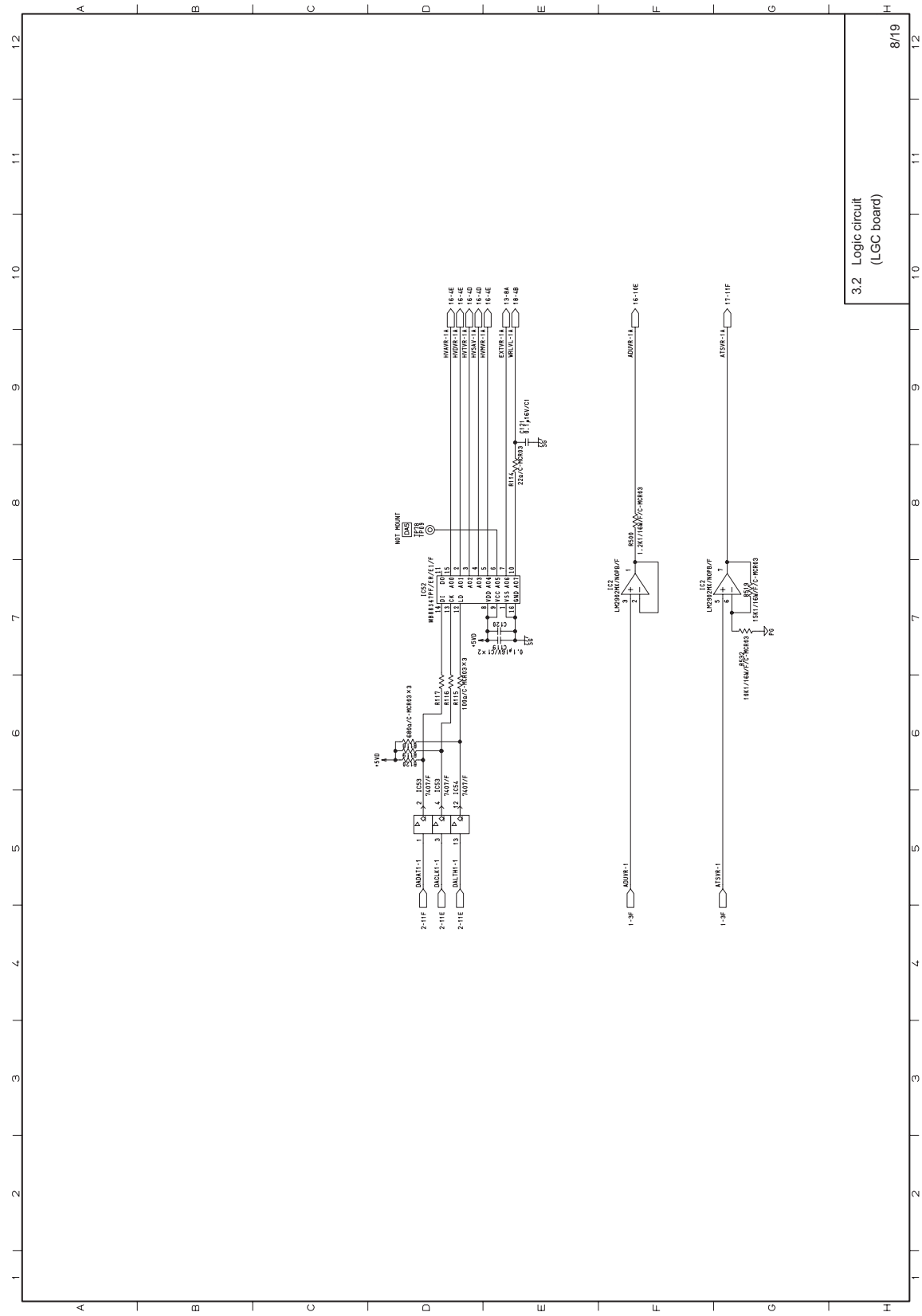


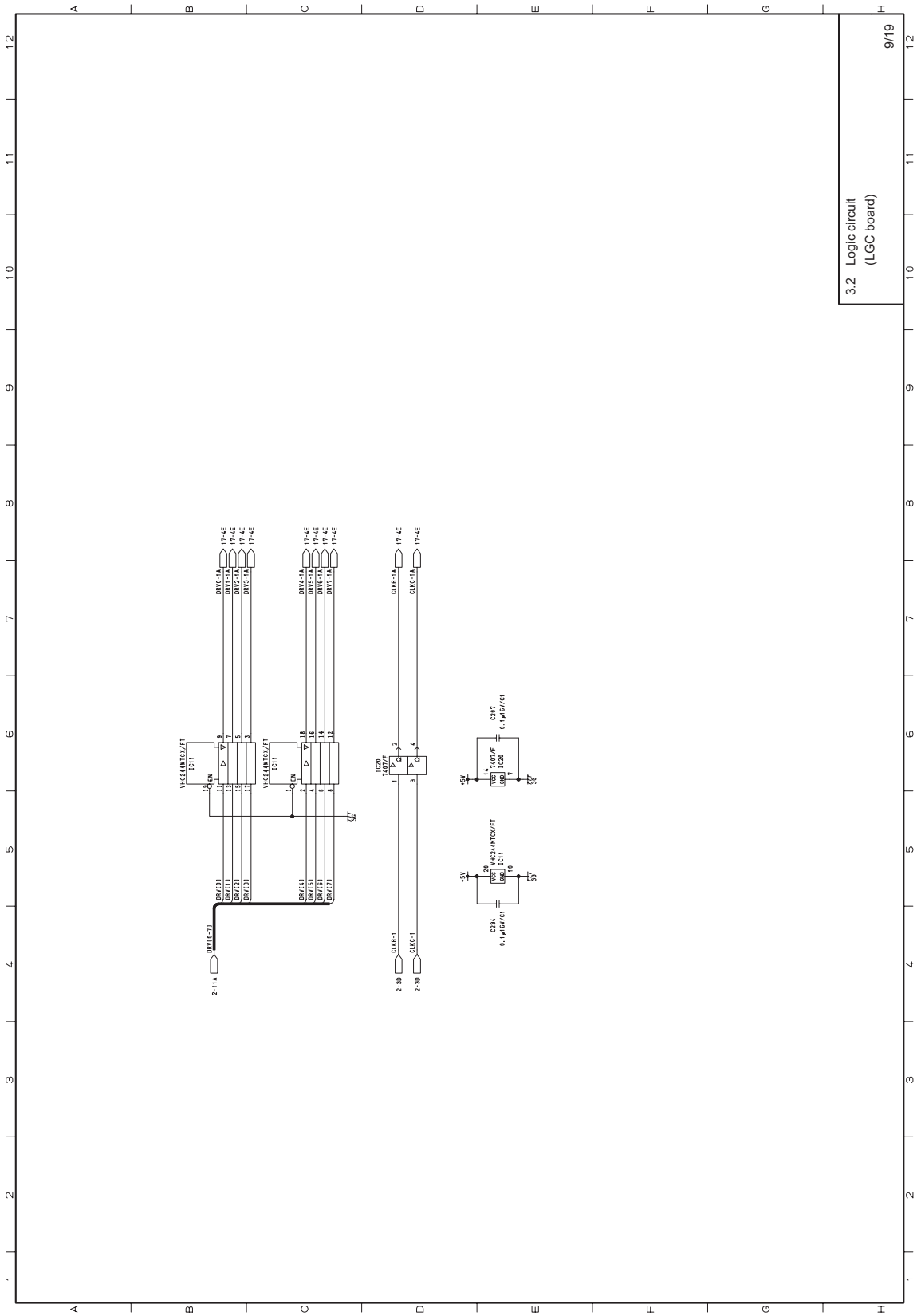


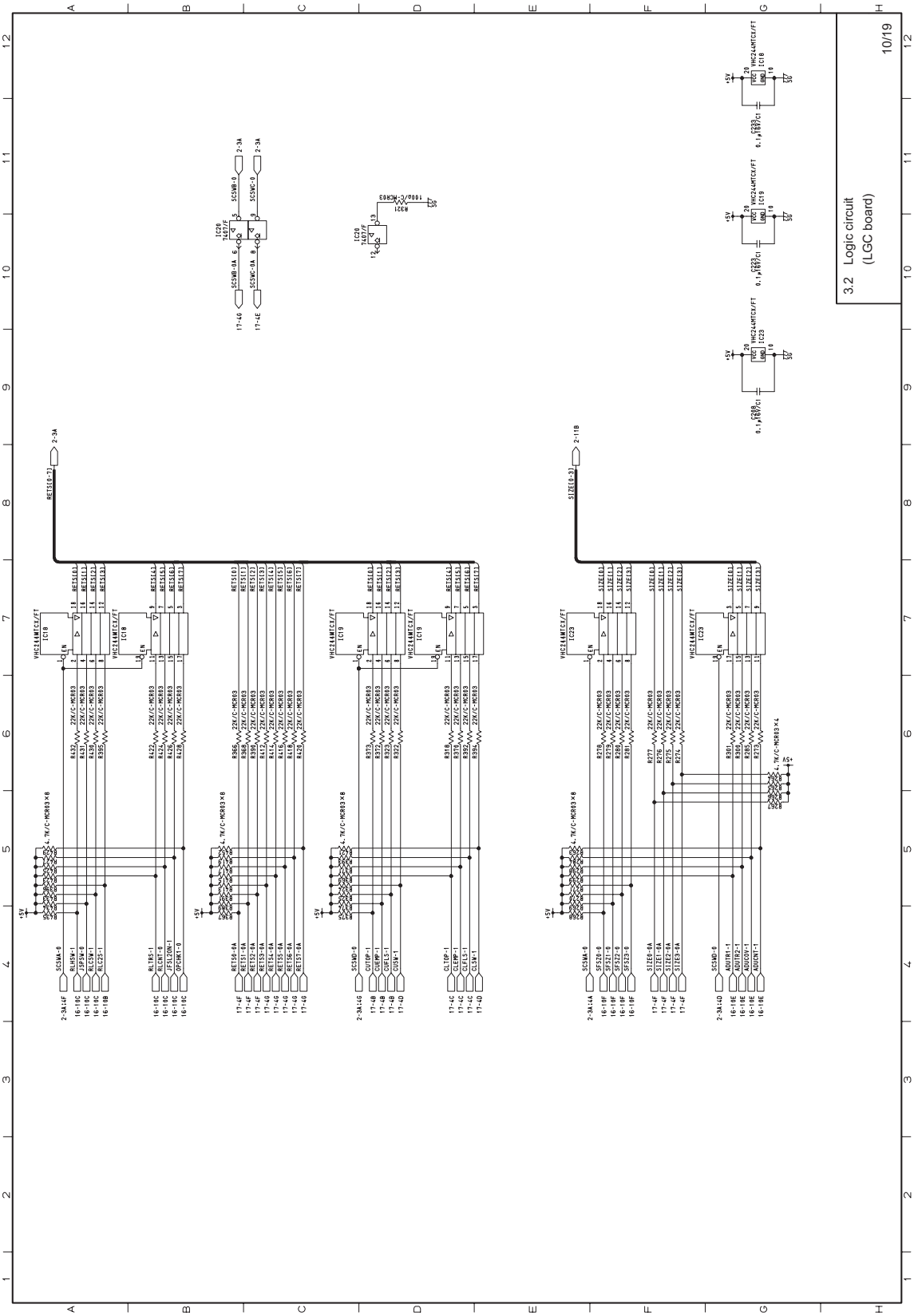


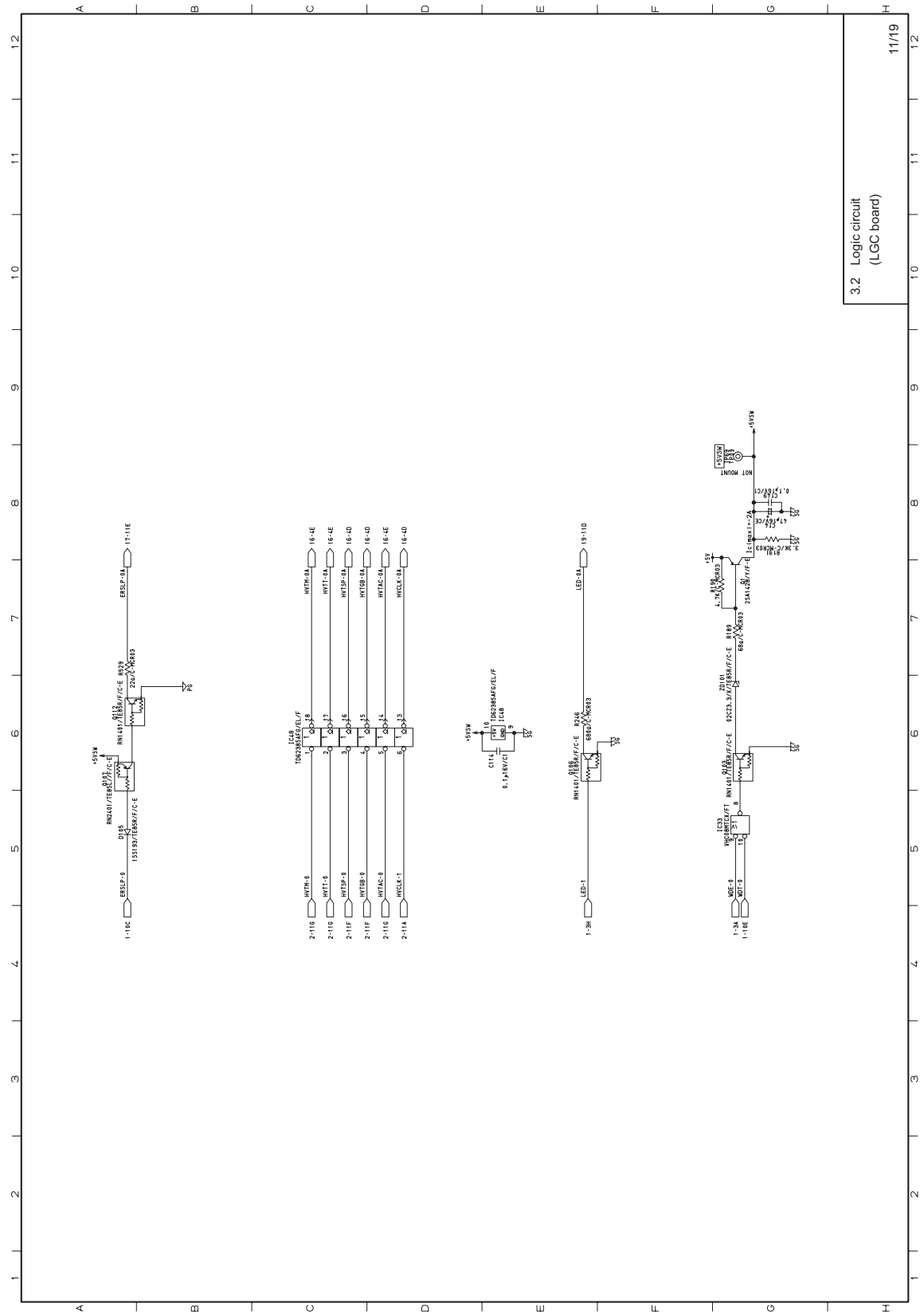


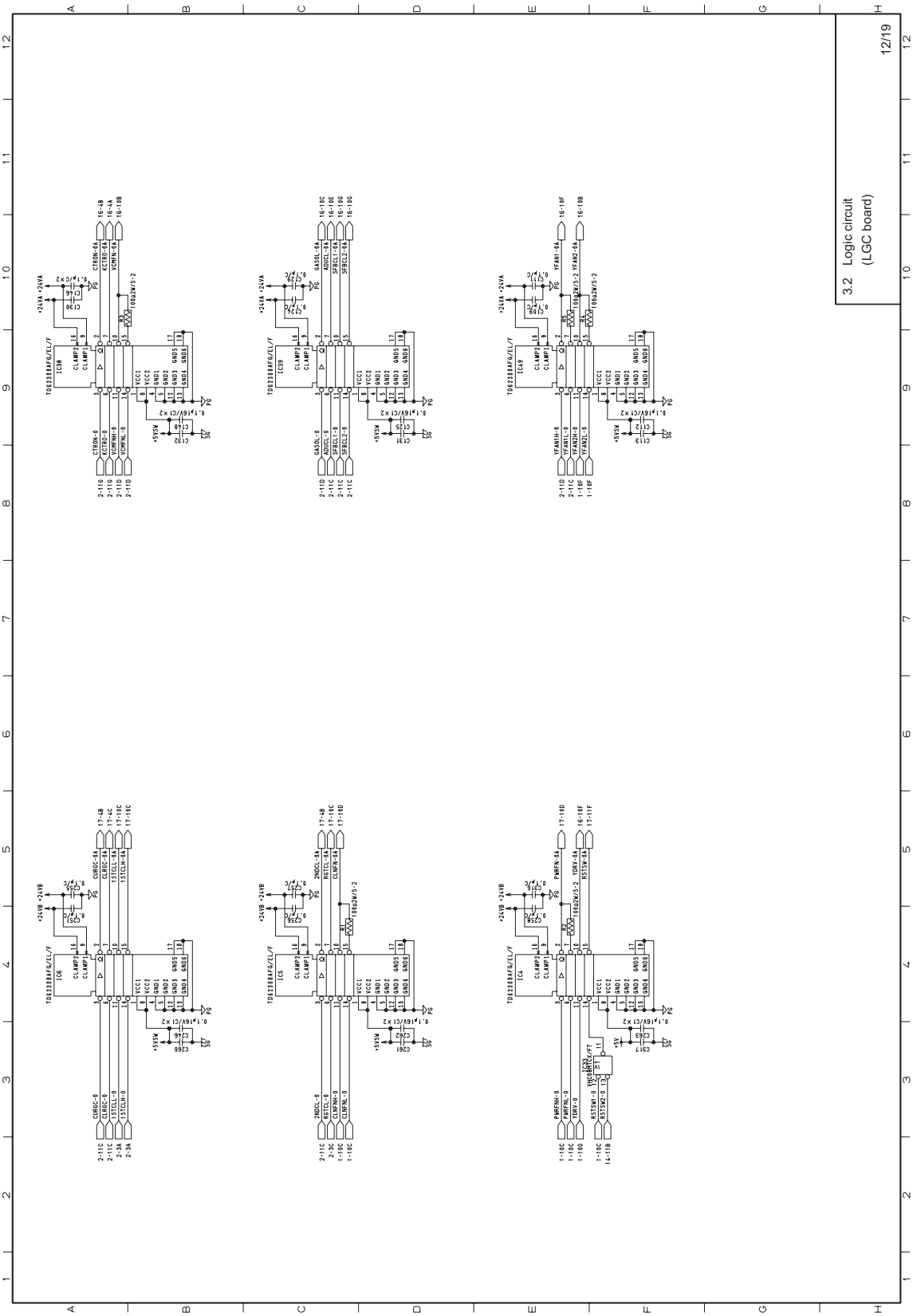


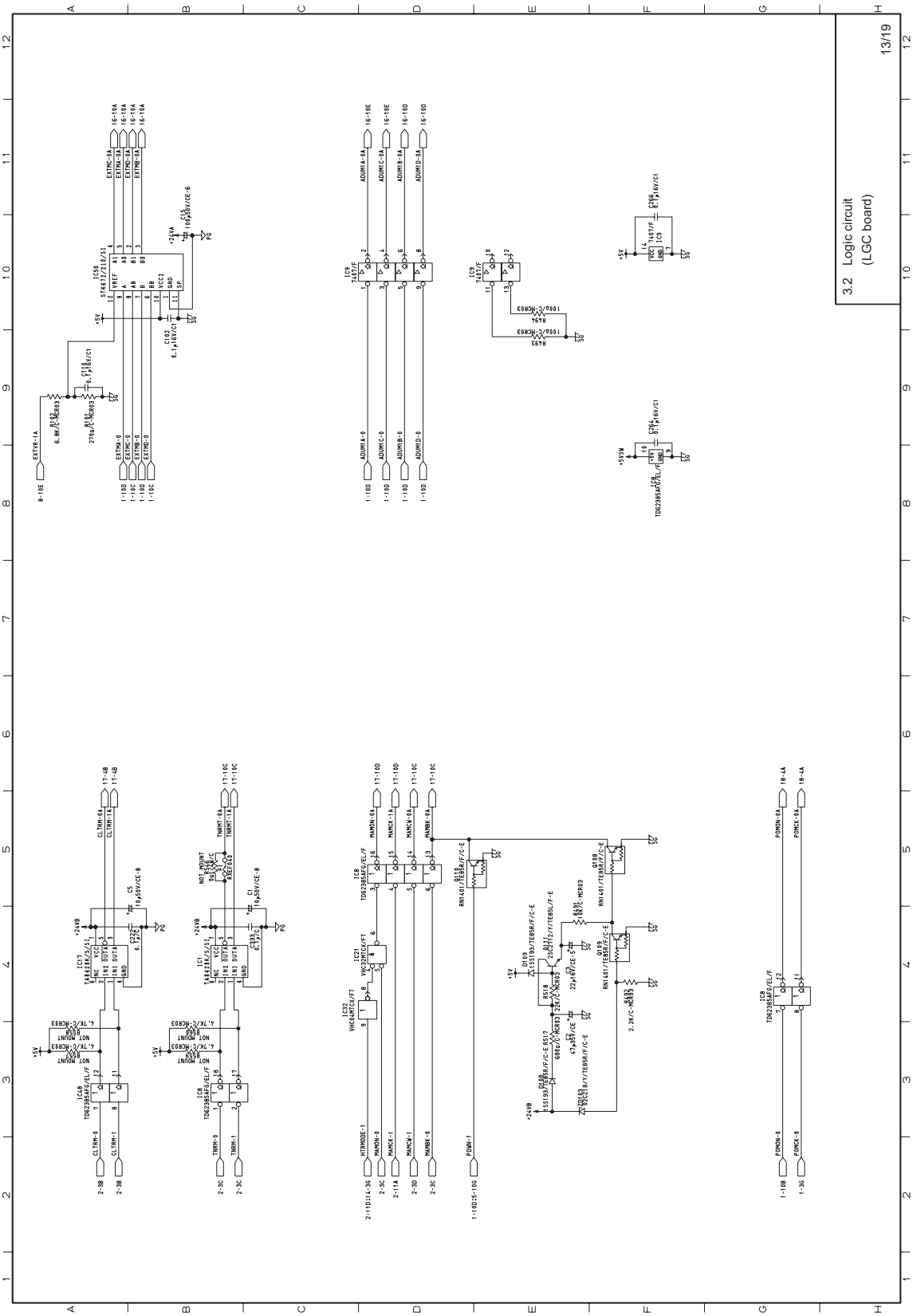


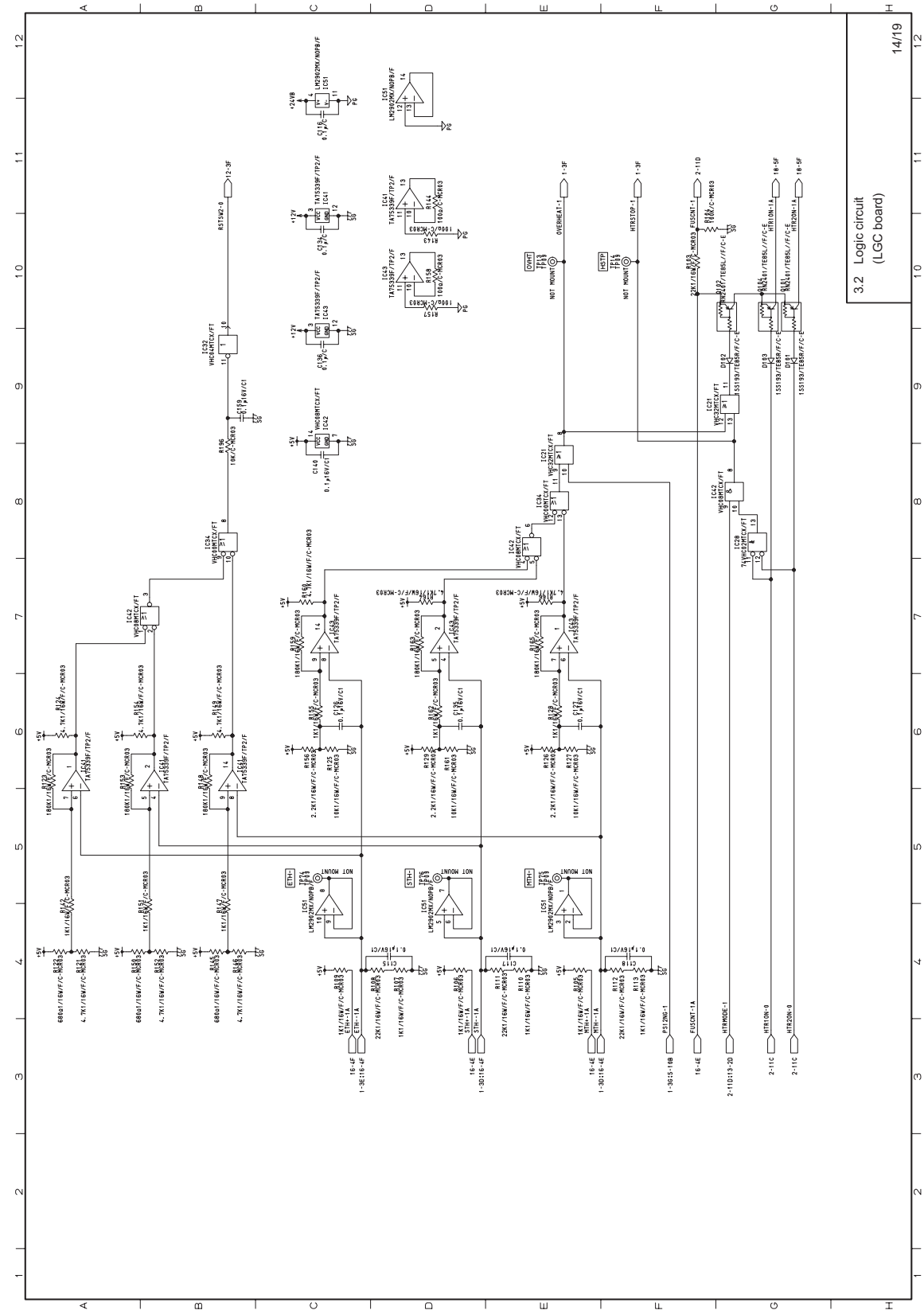


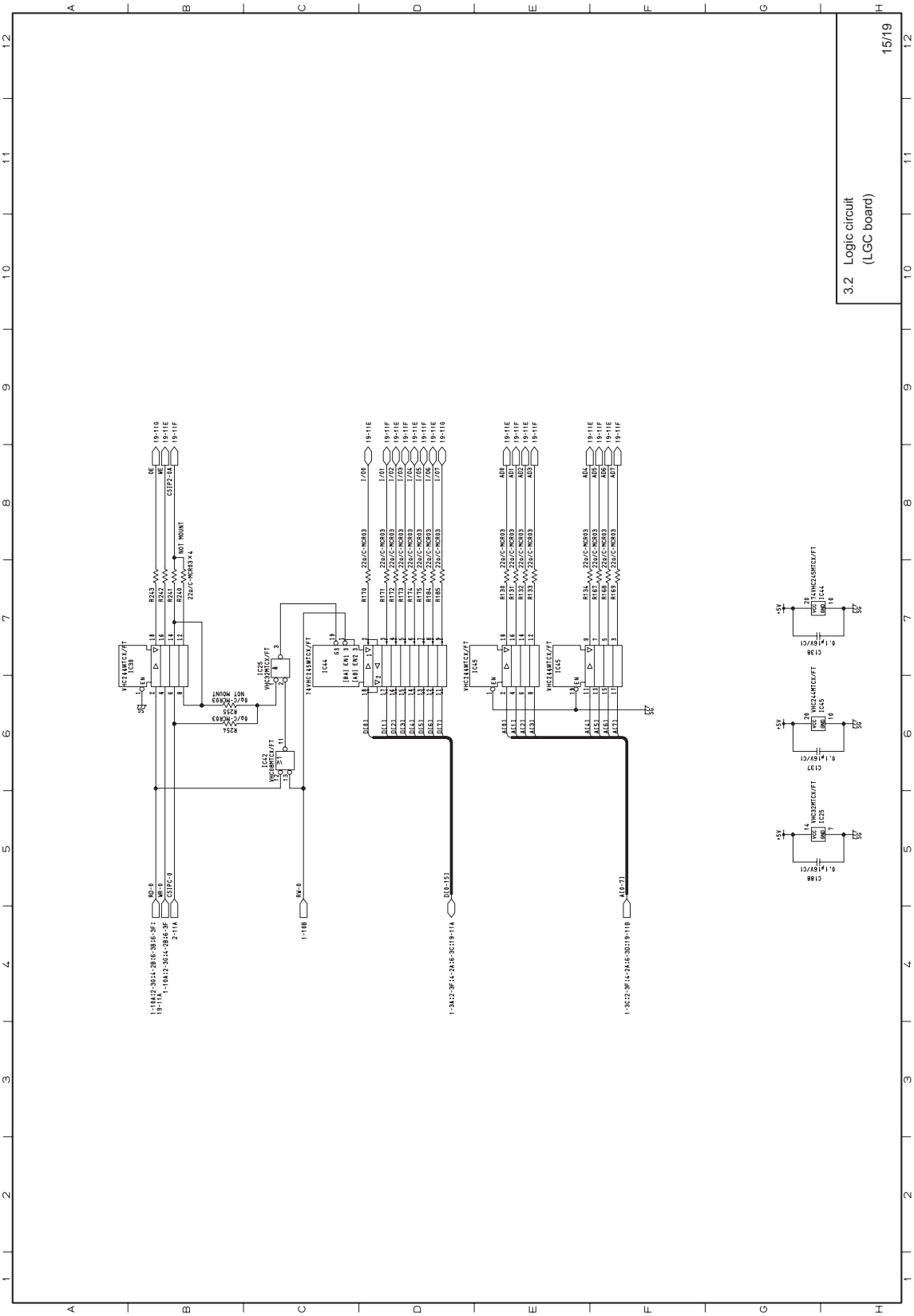


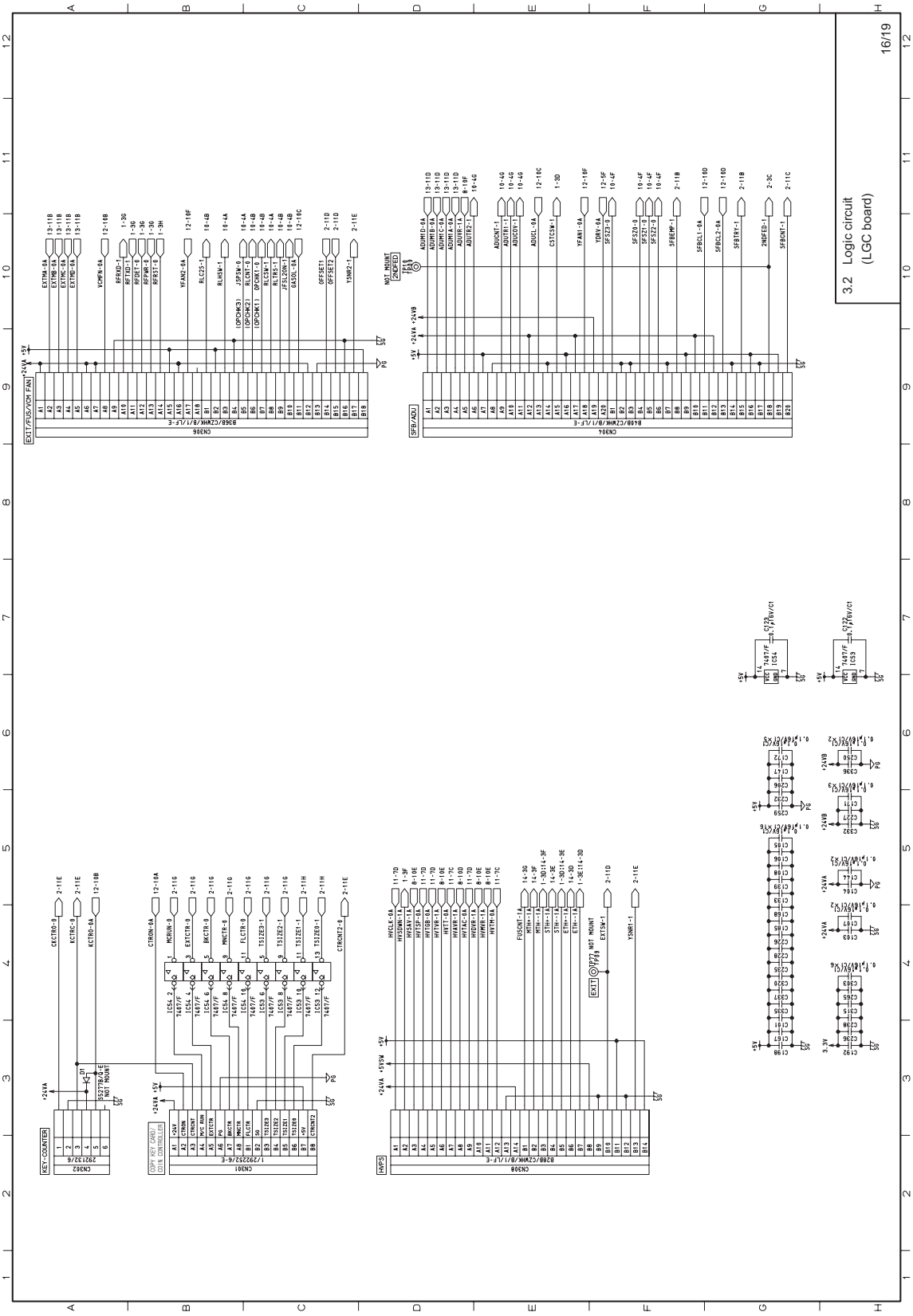


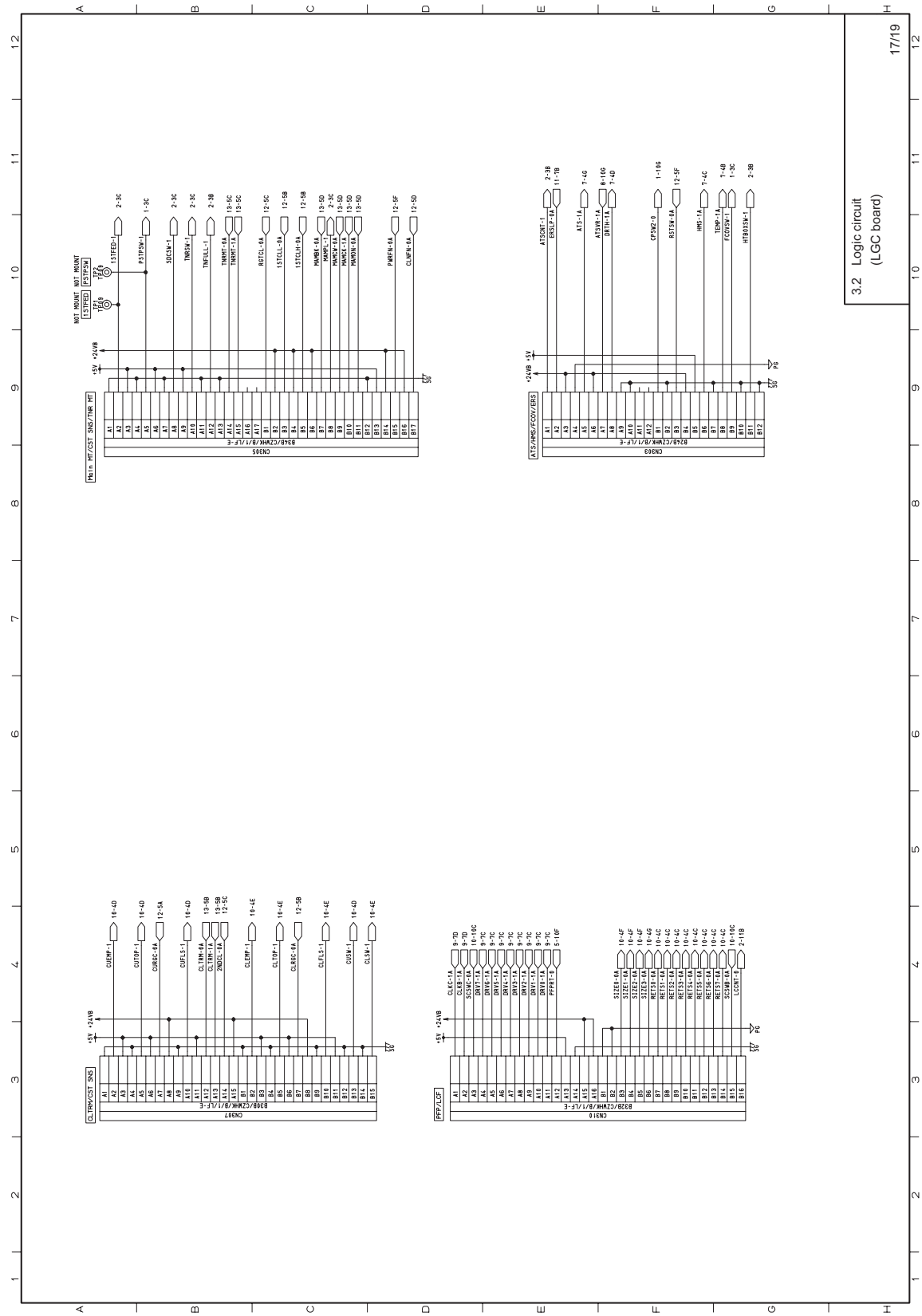


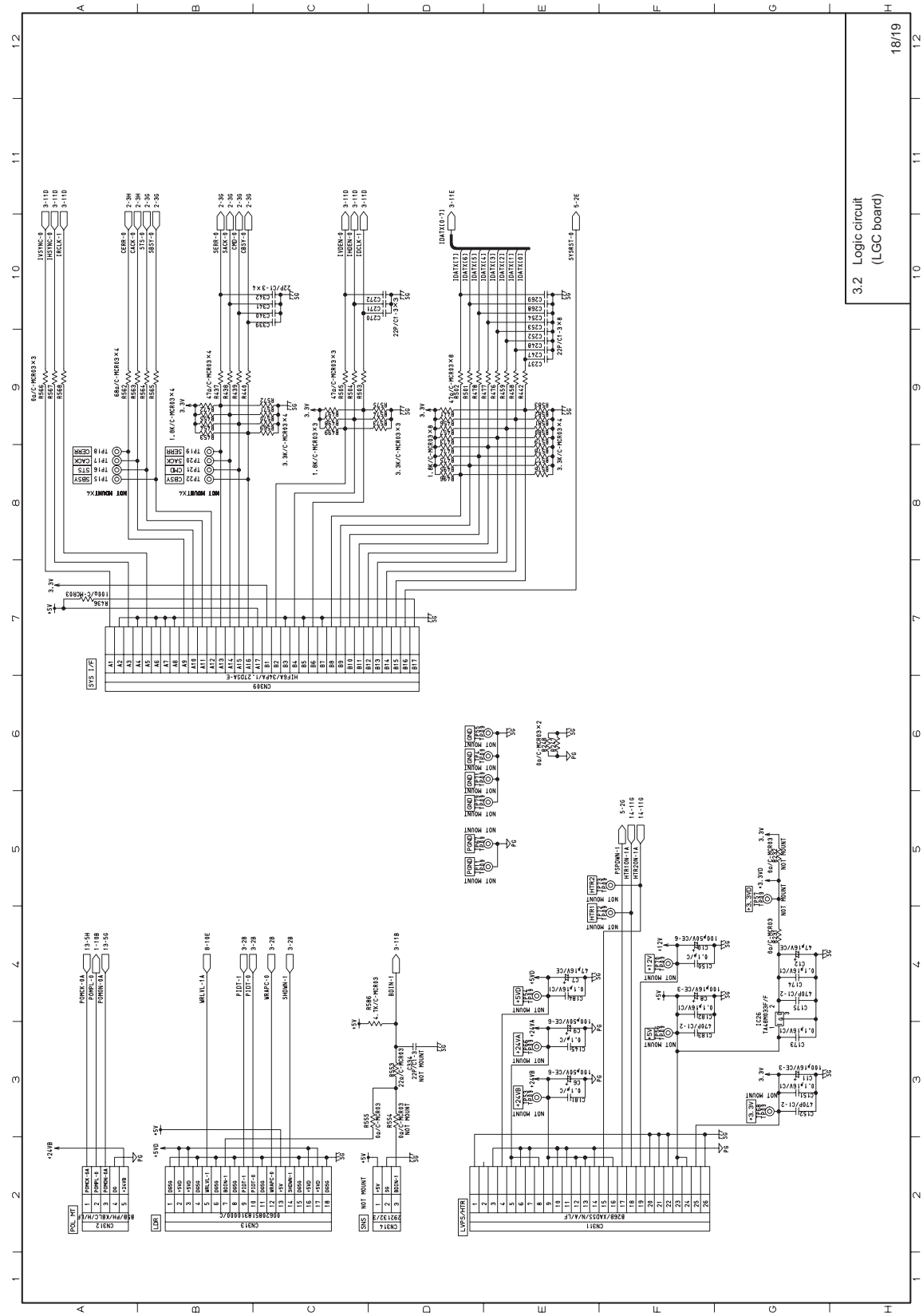


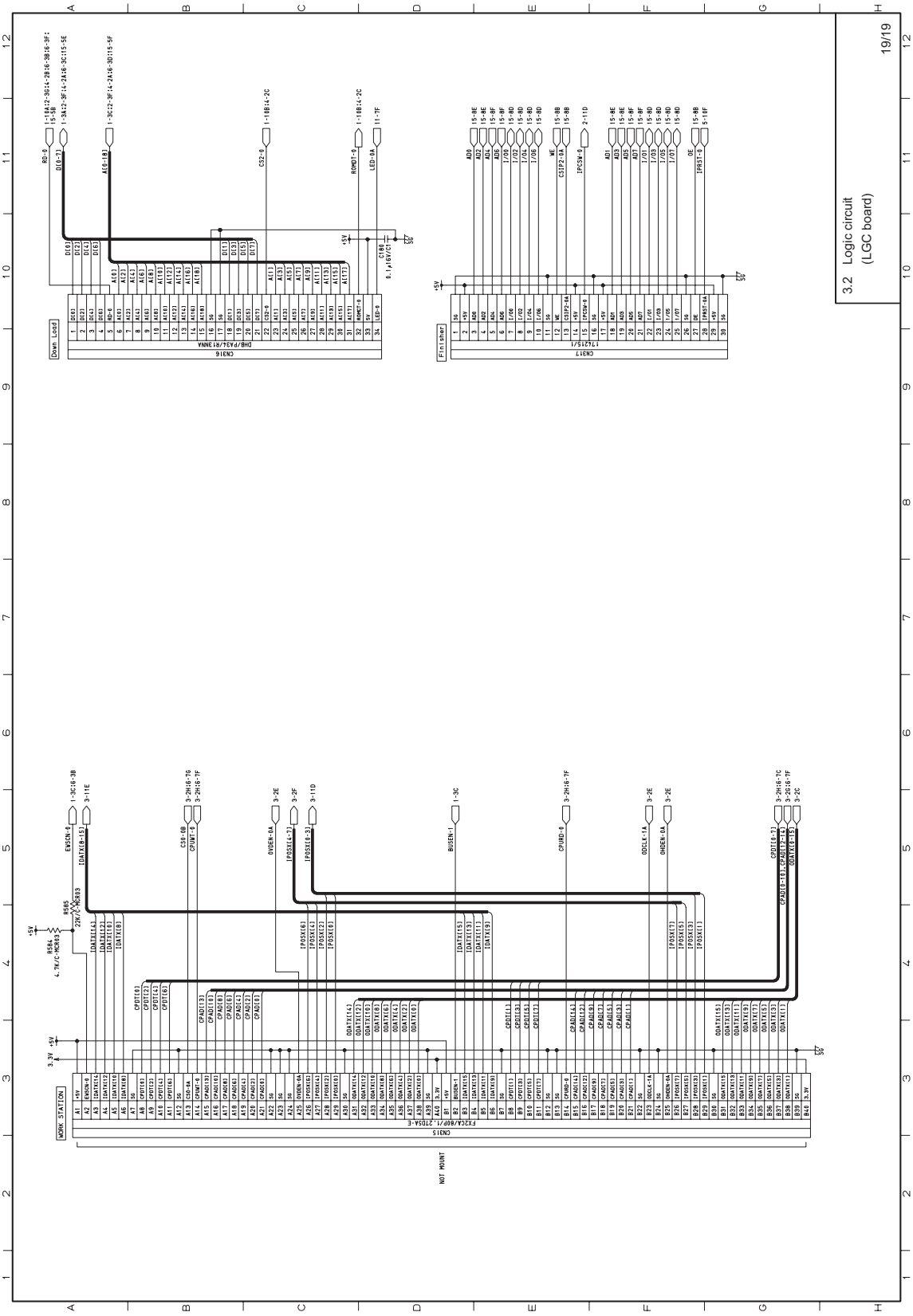




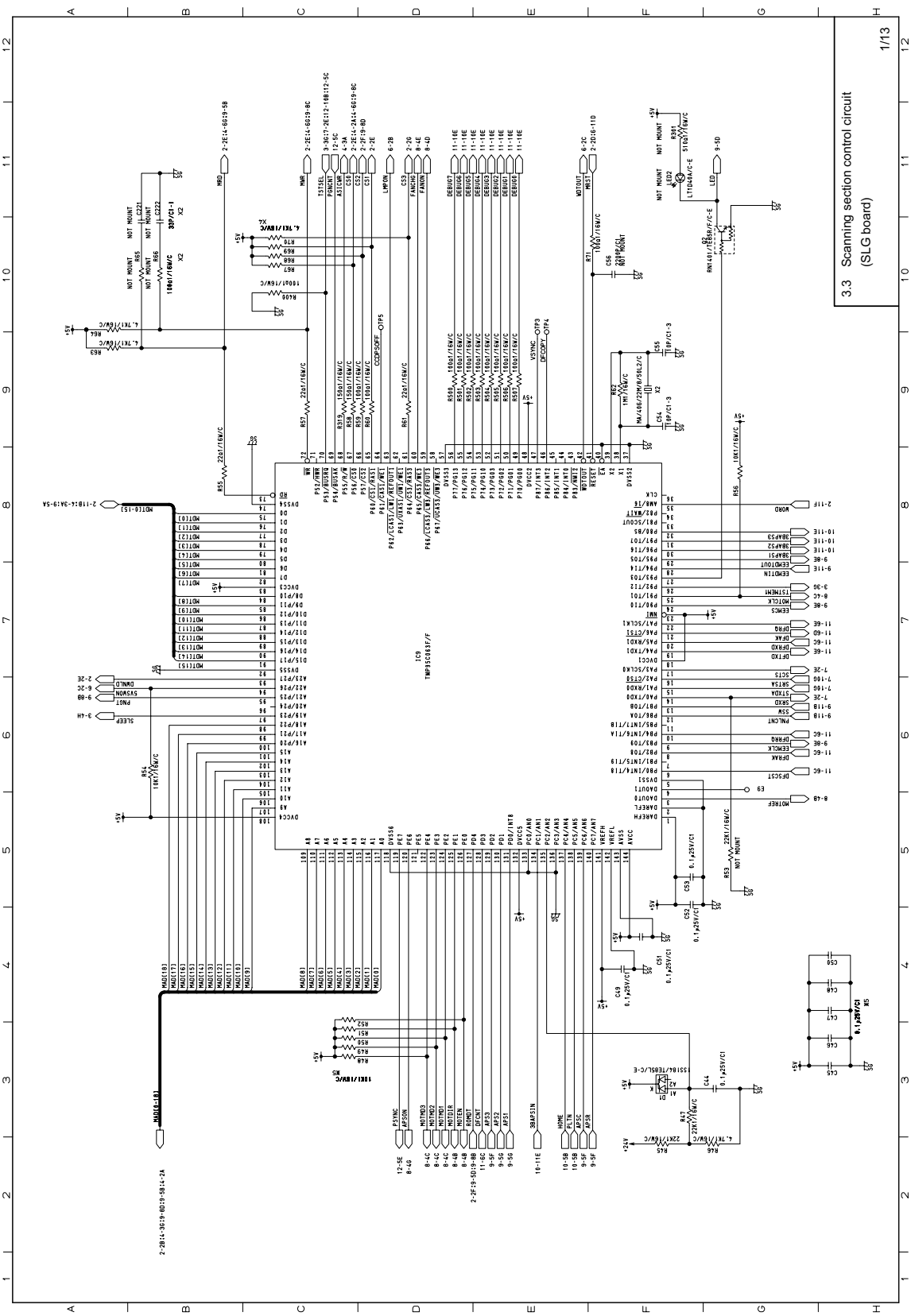


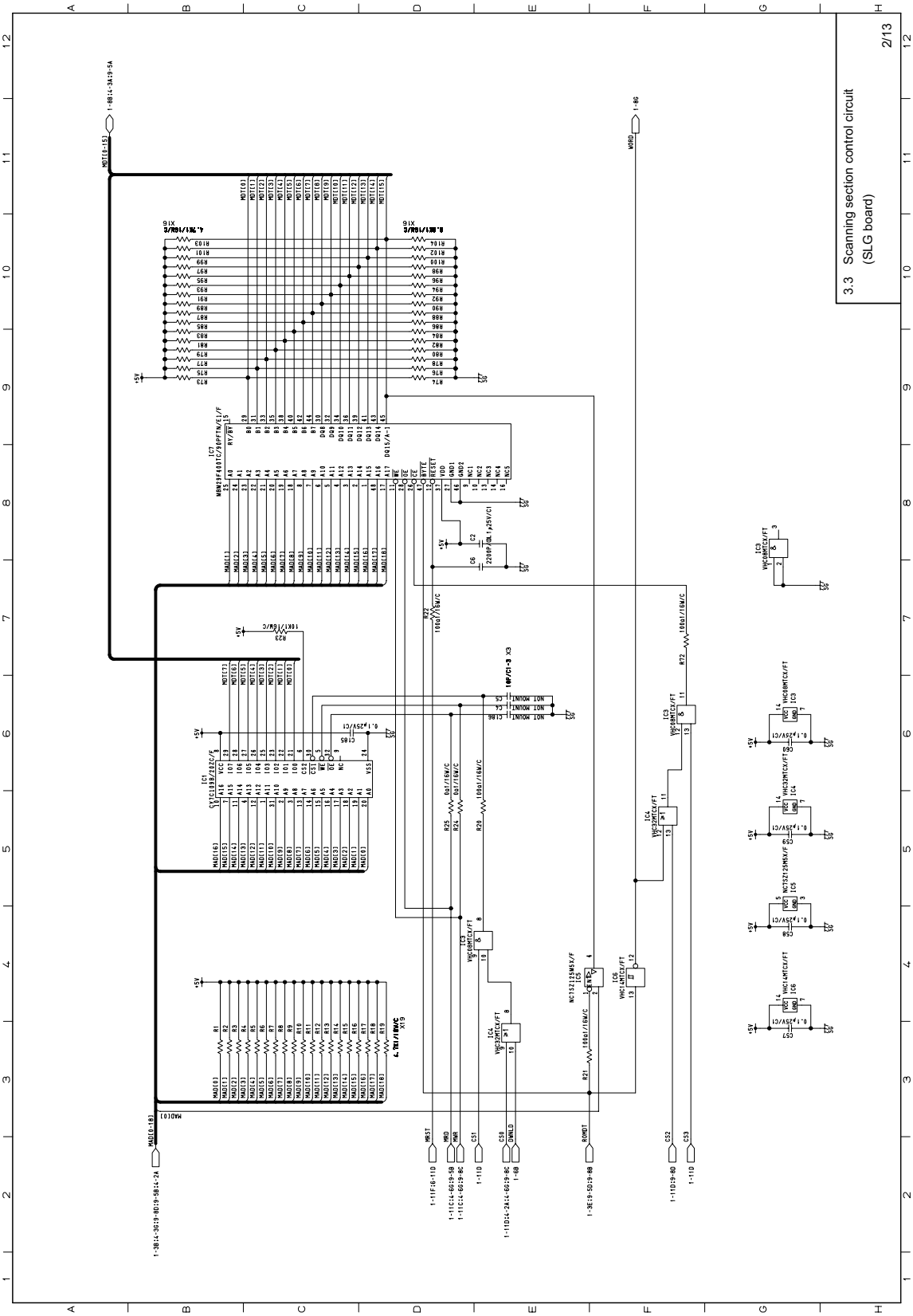


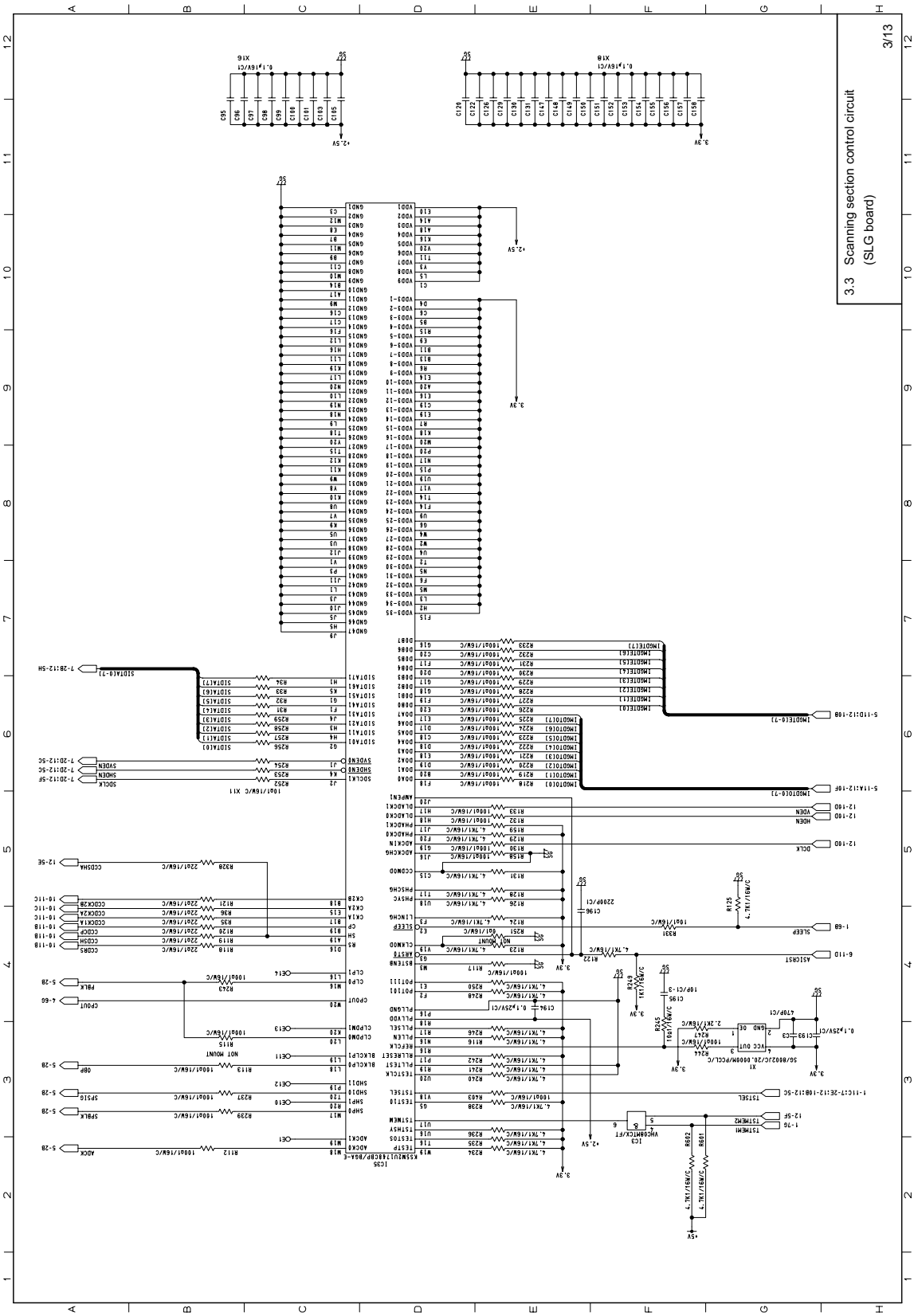


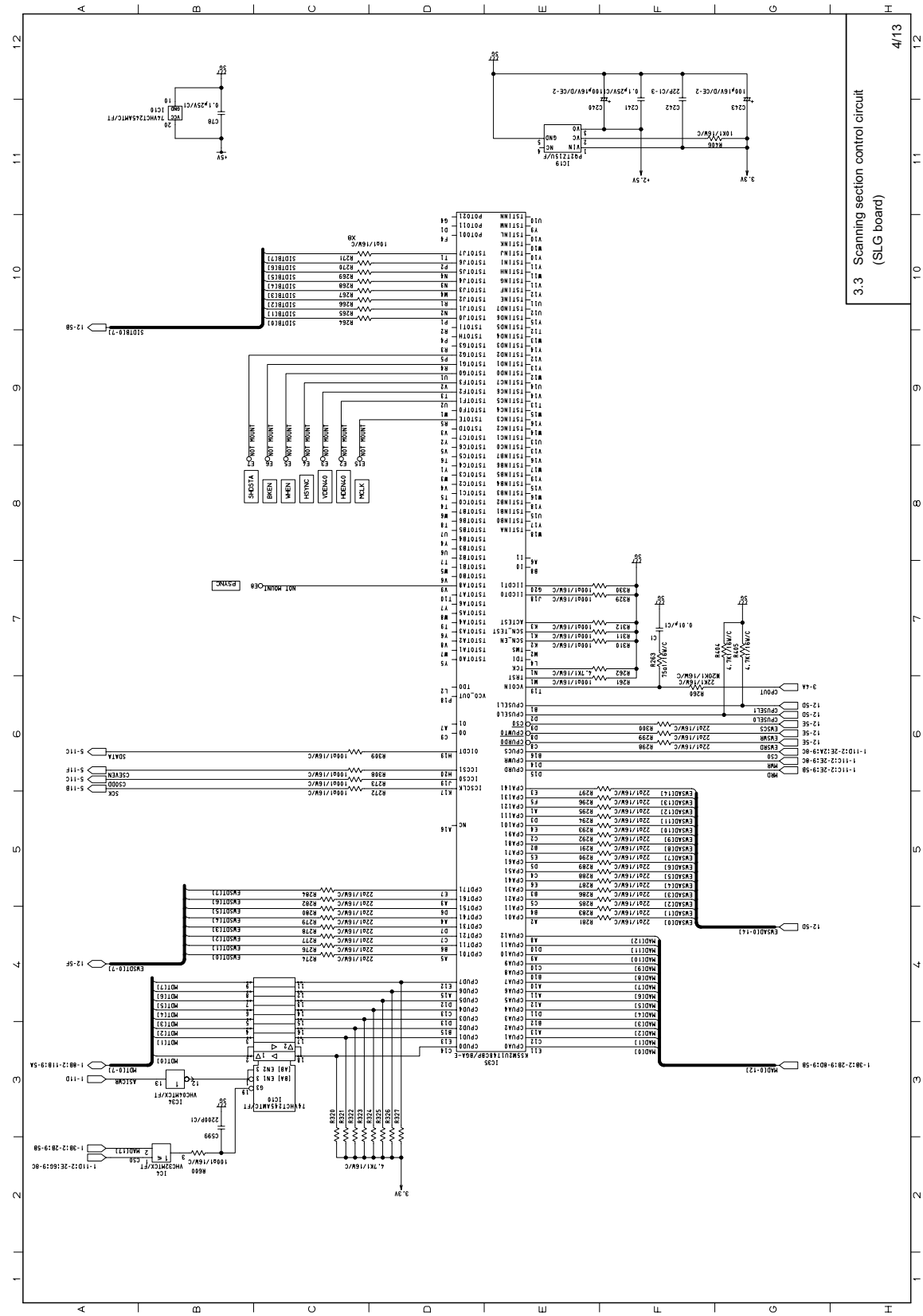


# 3.3 Scanning section control circuit (SLG board)









3.3 Scanning section control circuit (SLG board)

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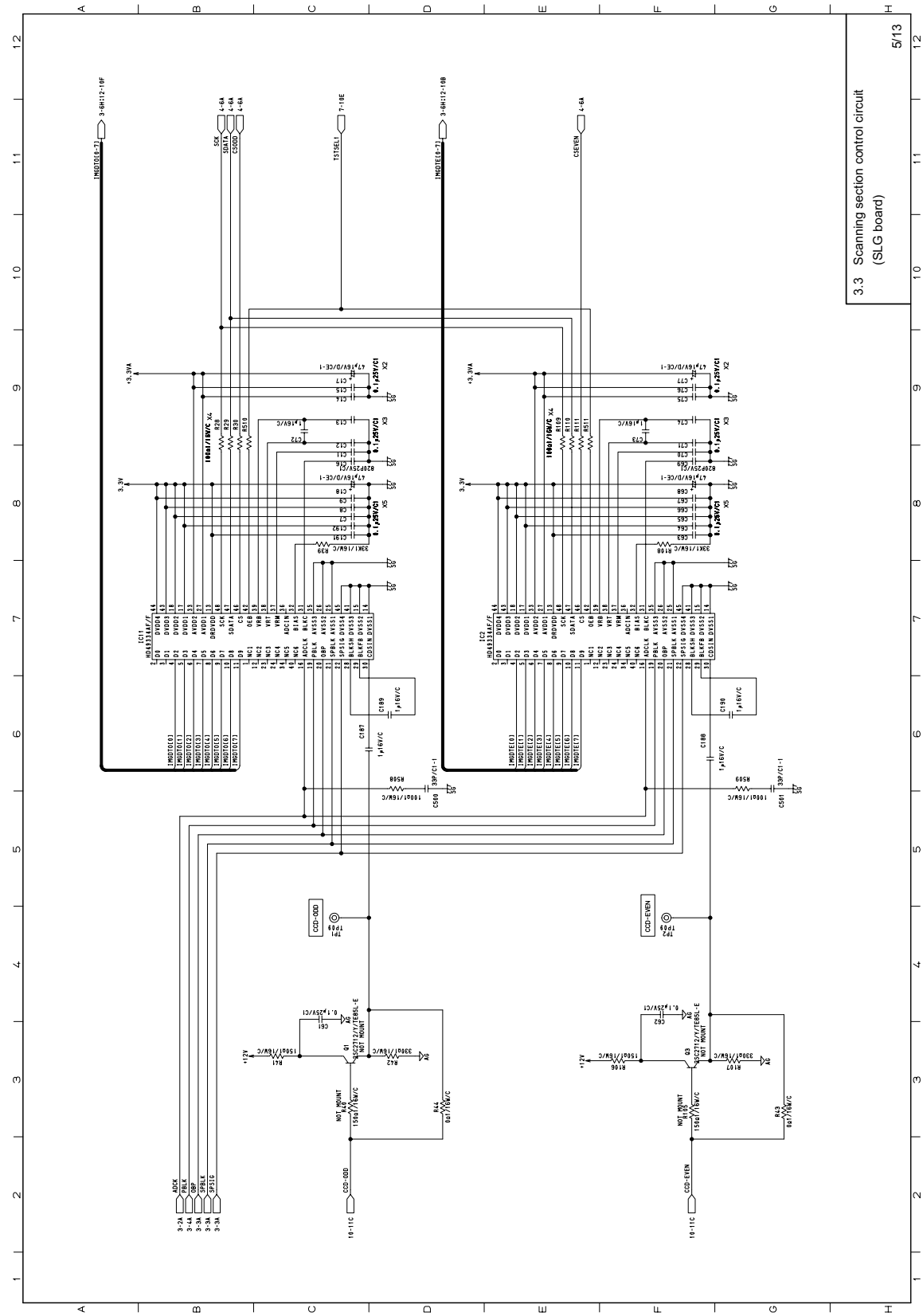
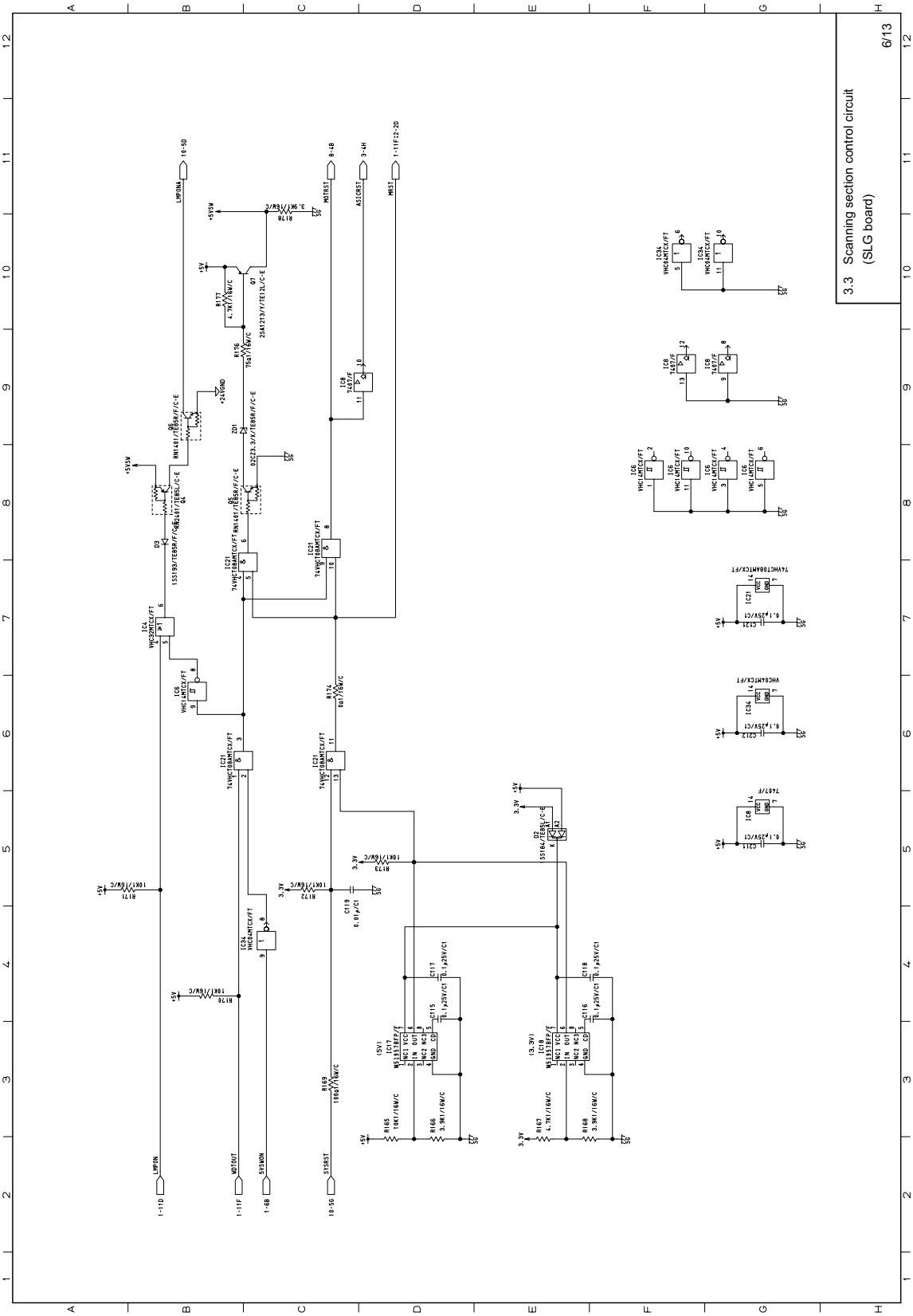
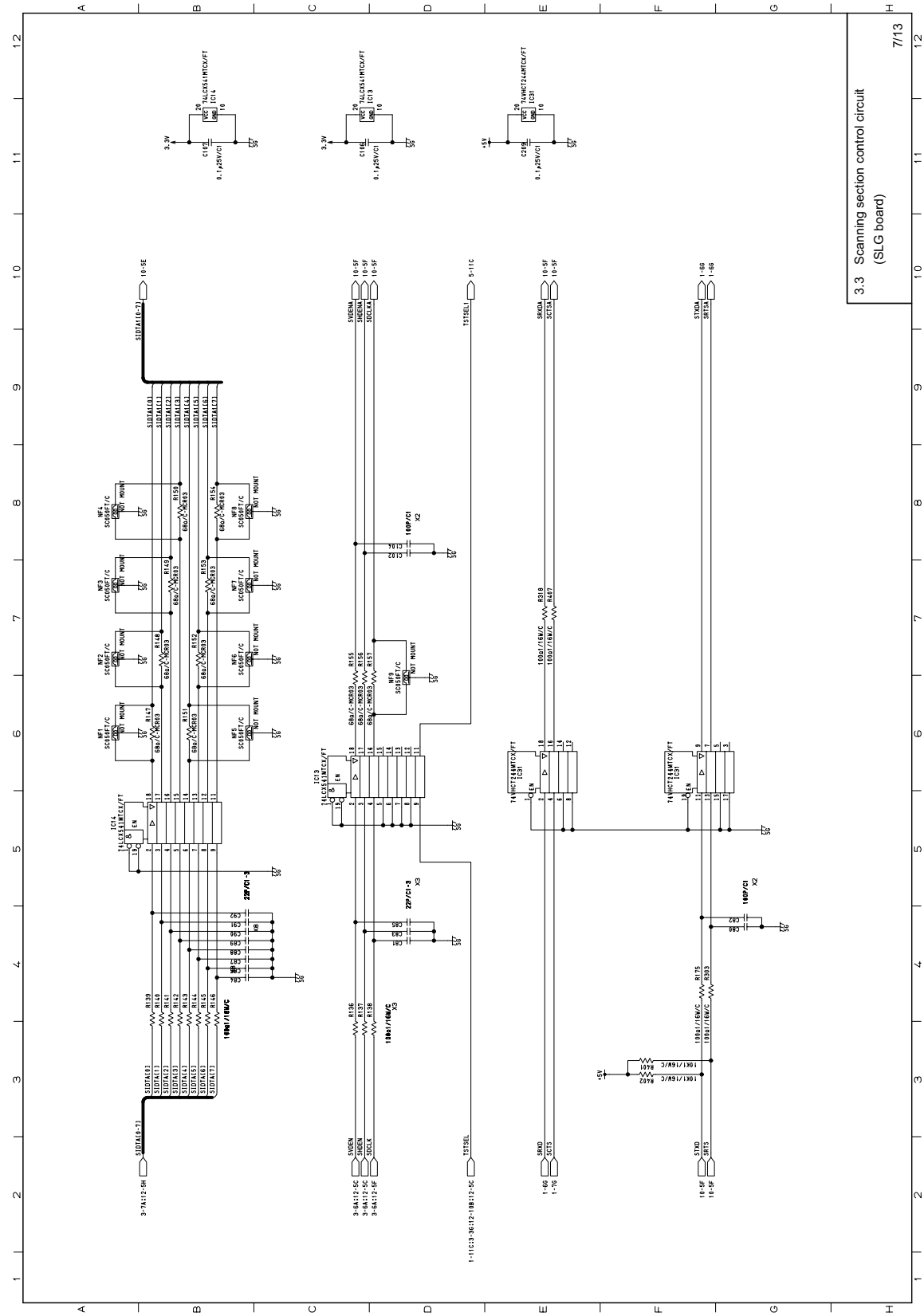
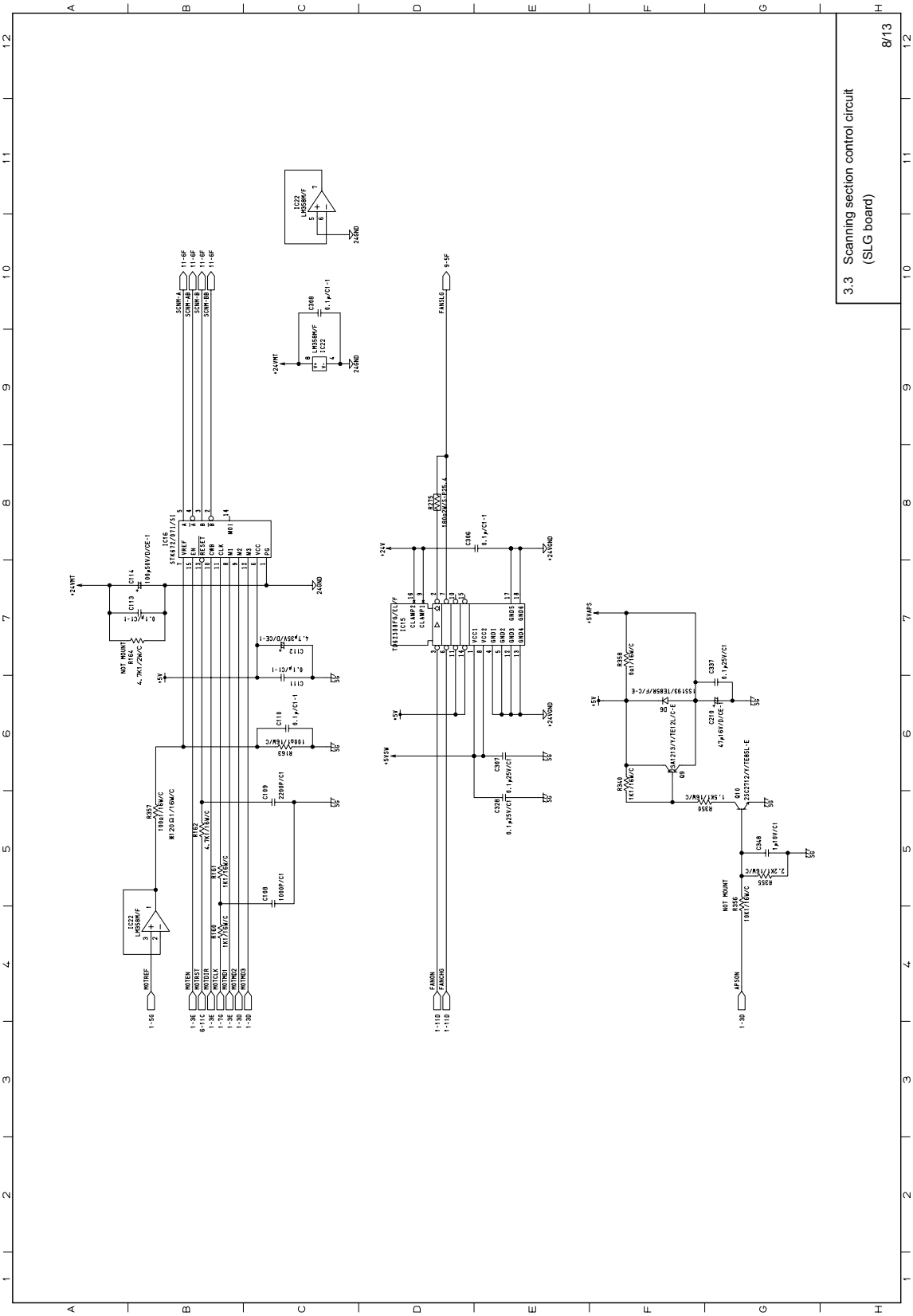
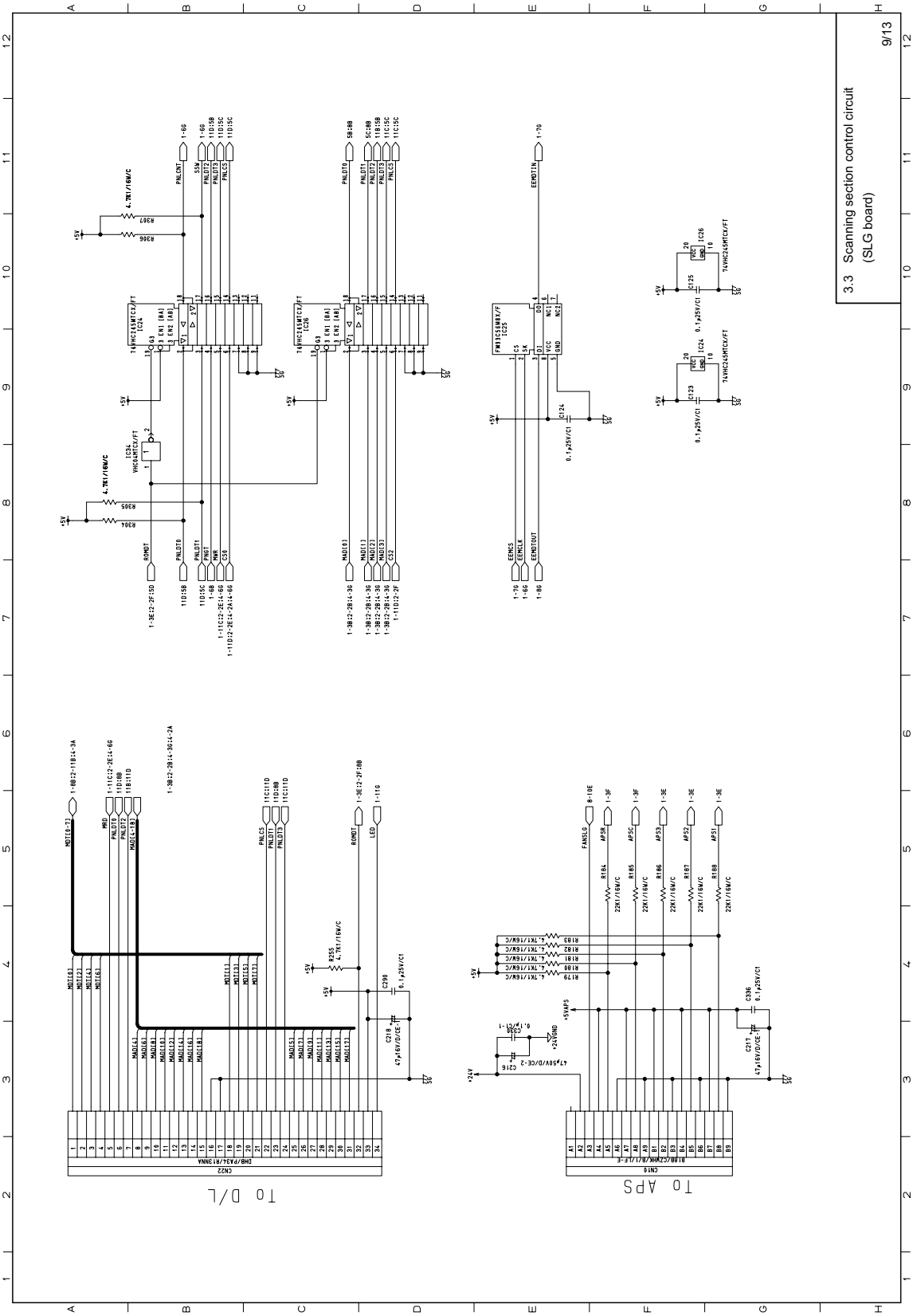
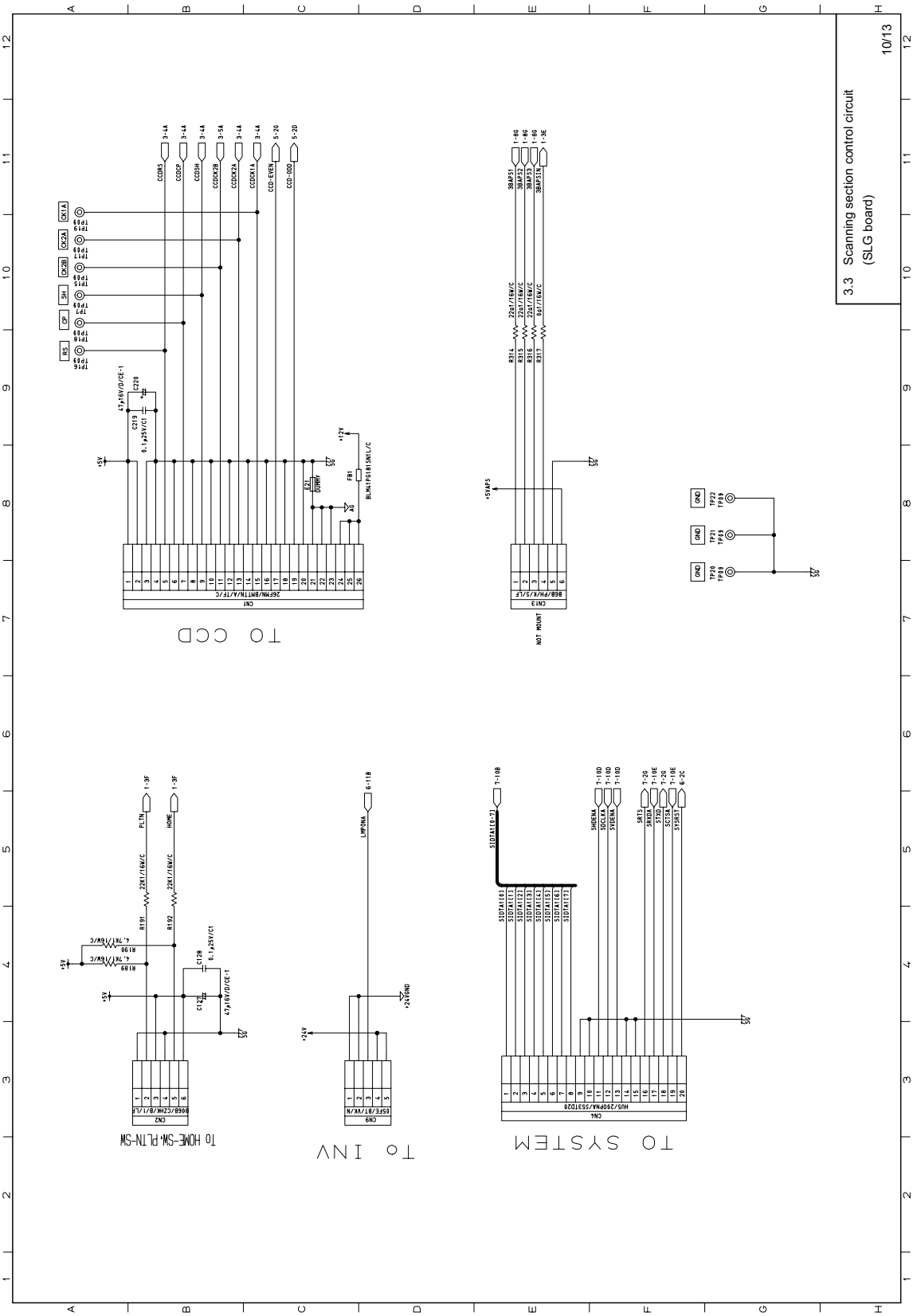


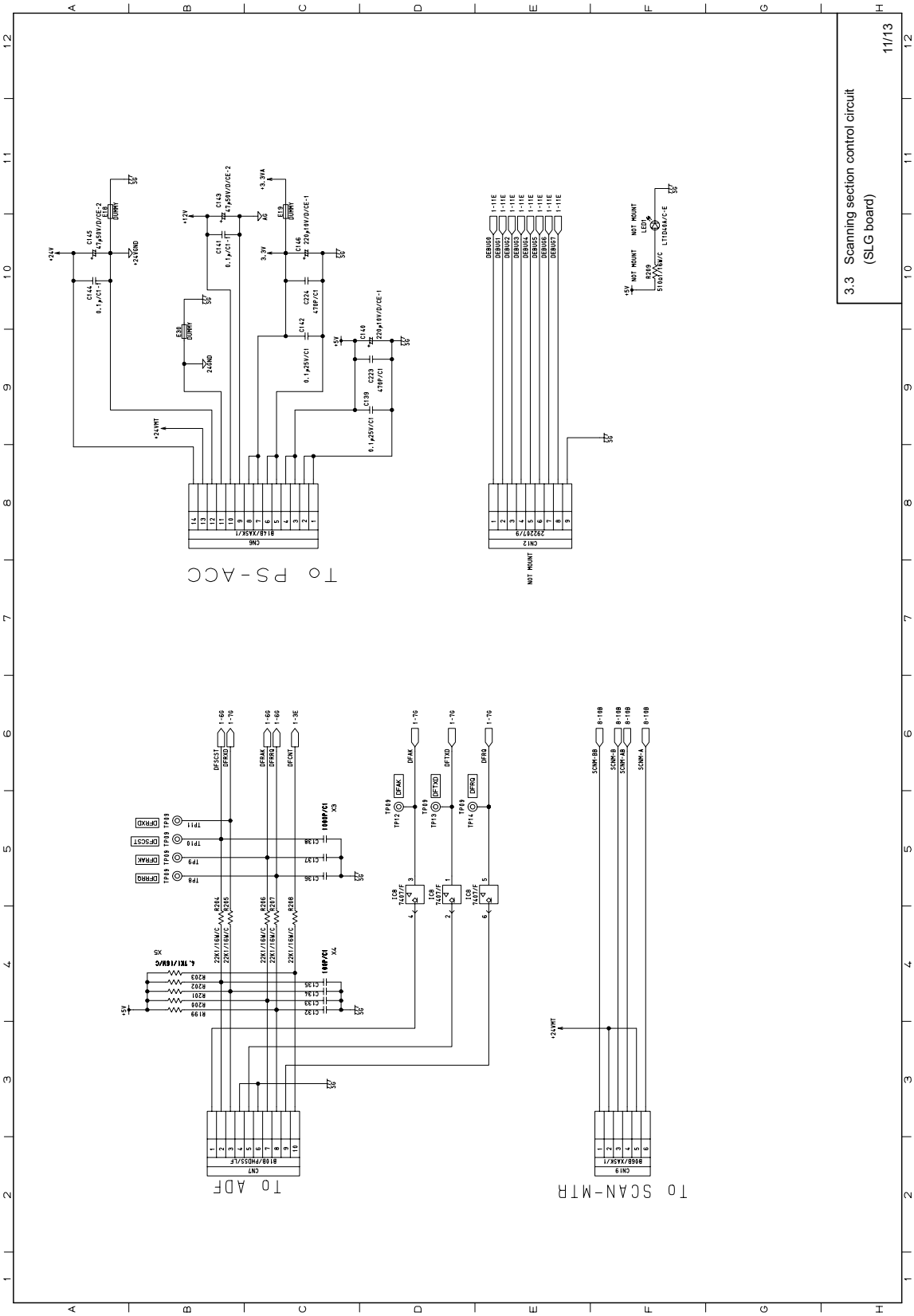


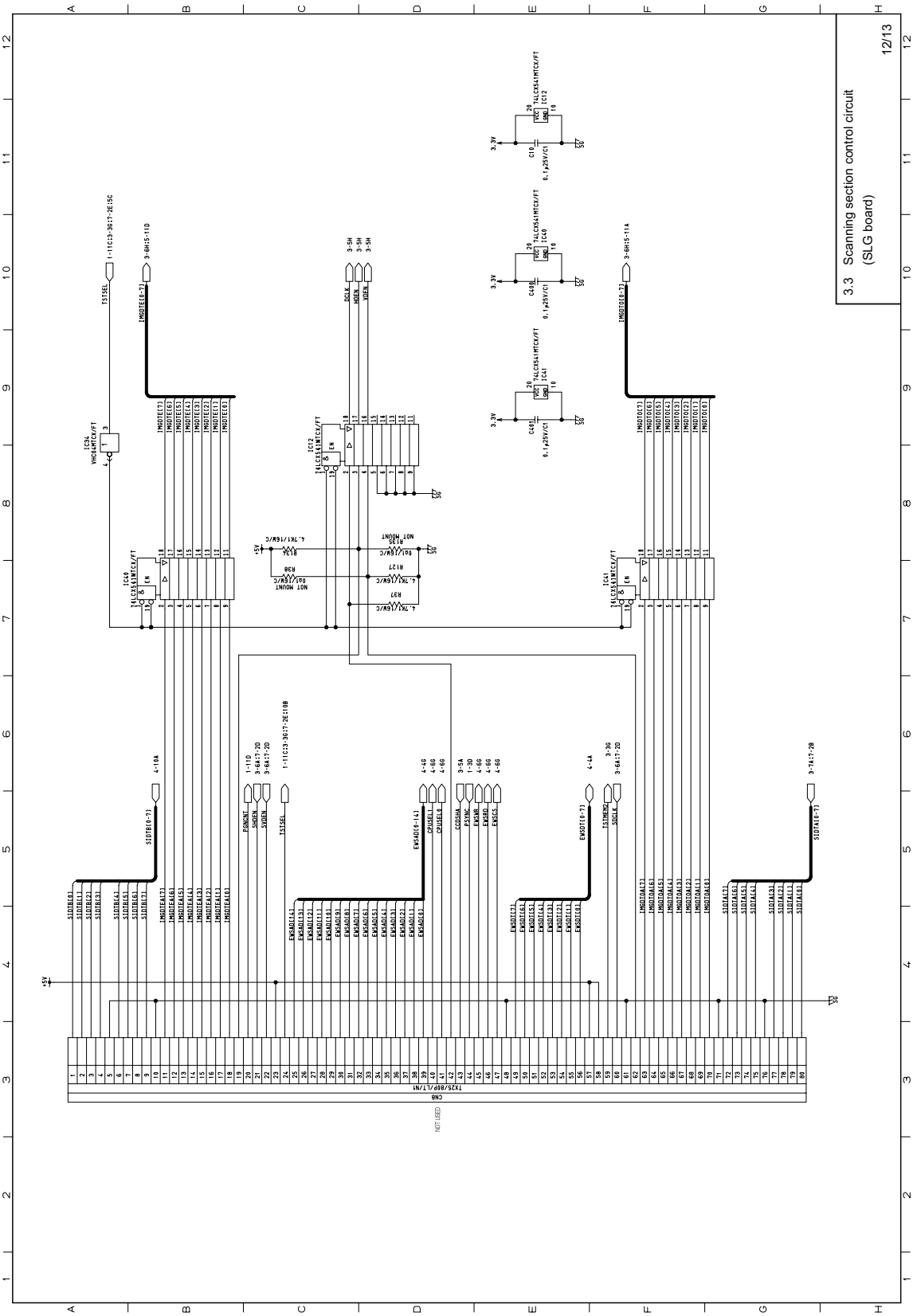


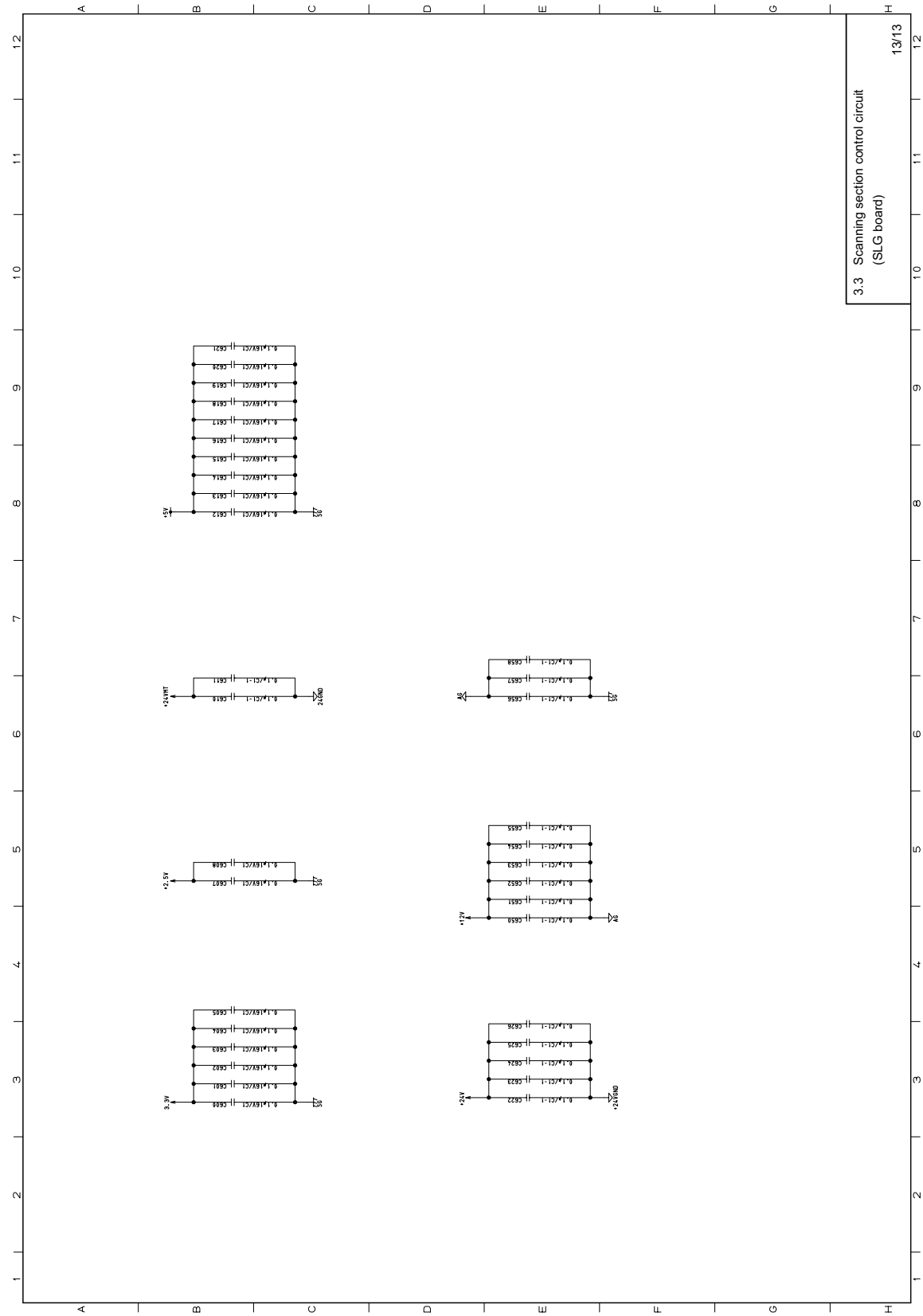




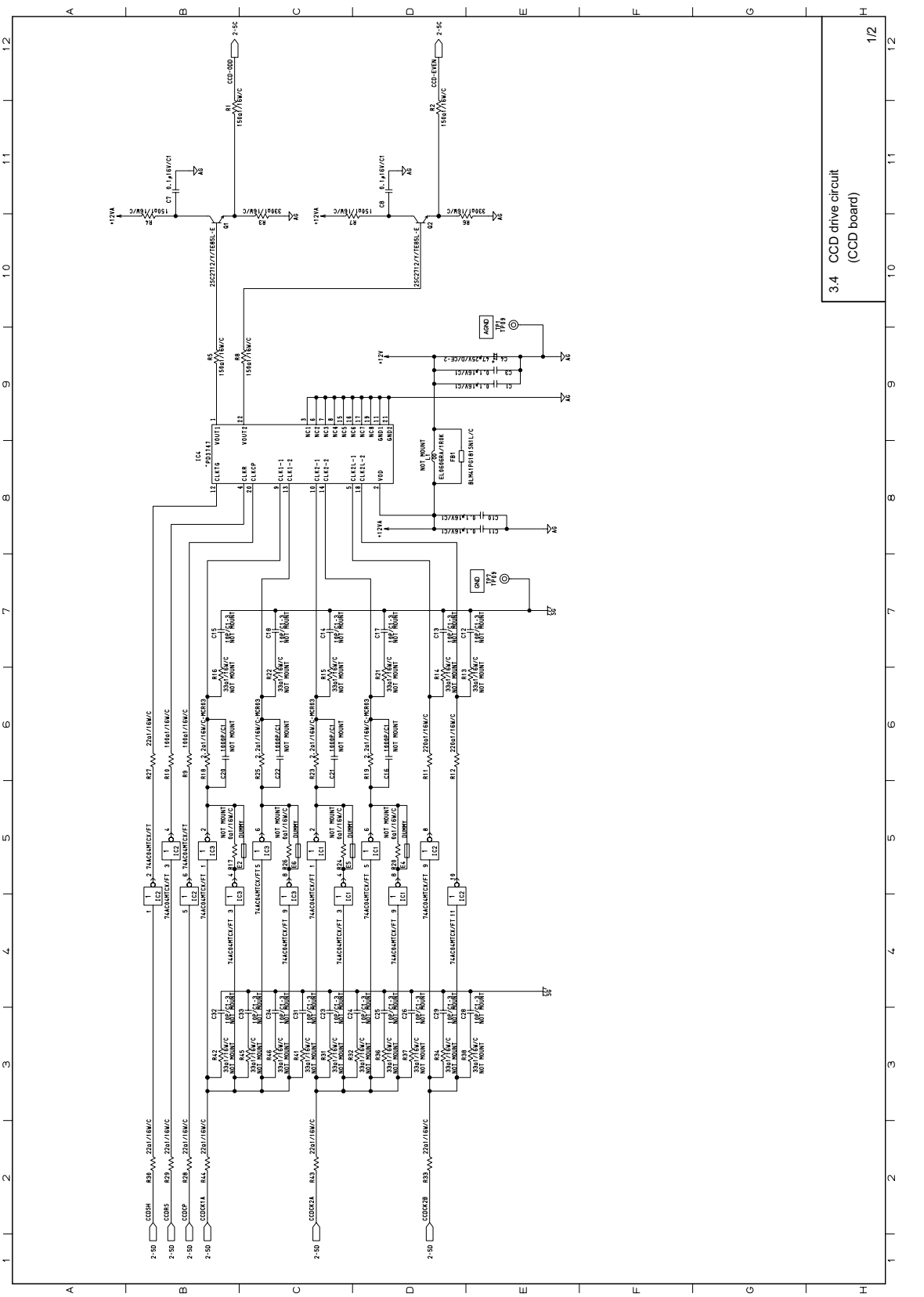


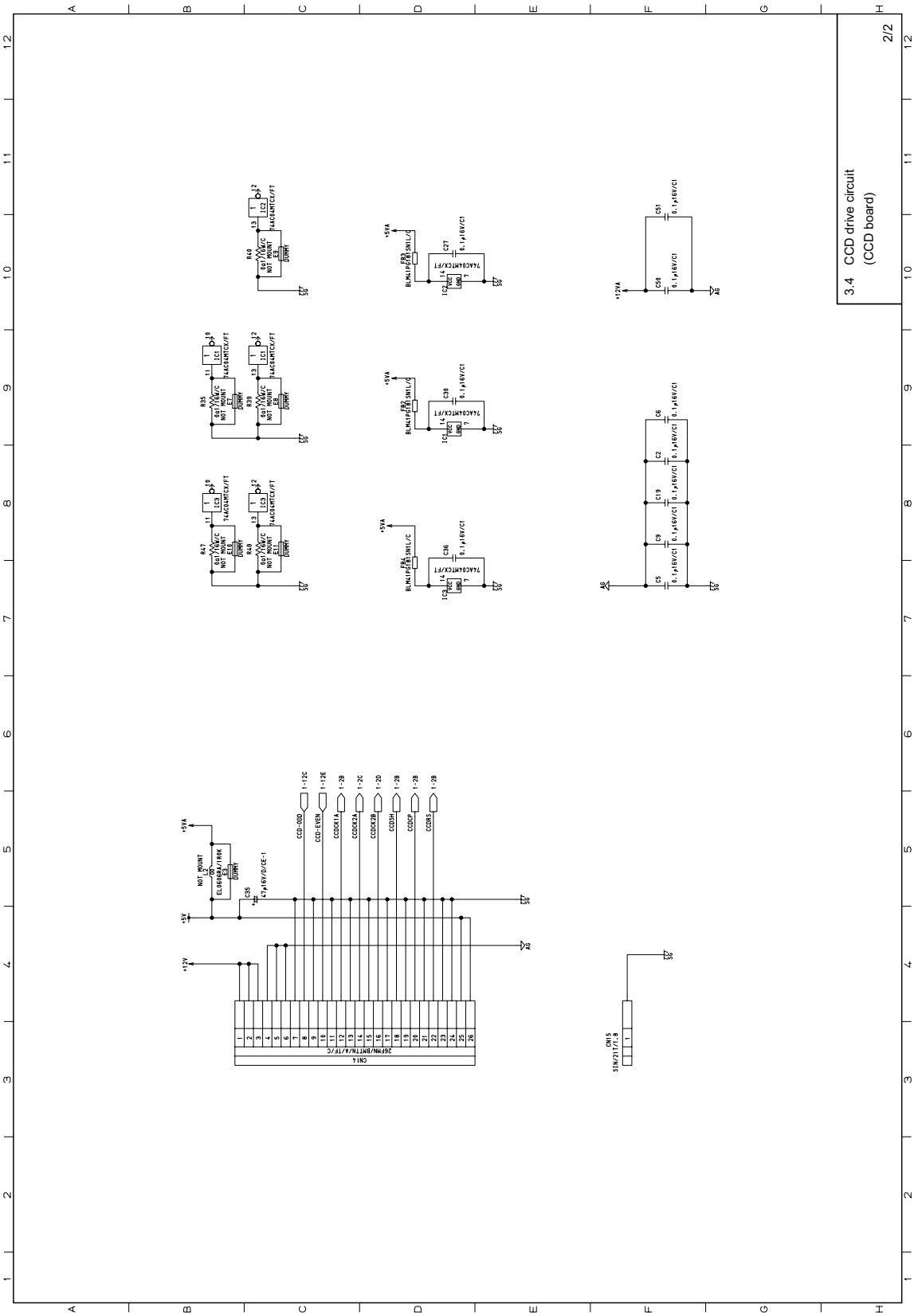




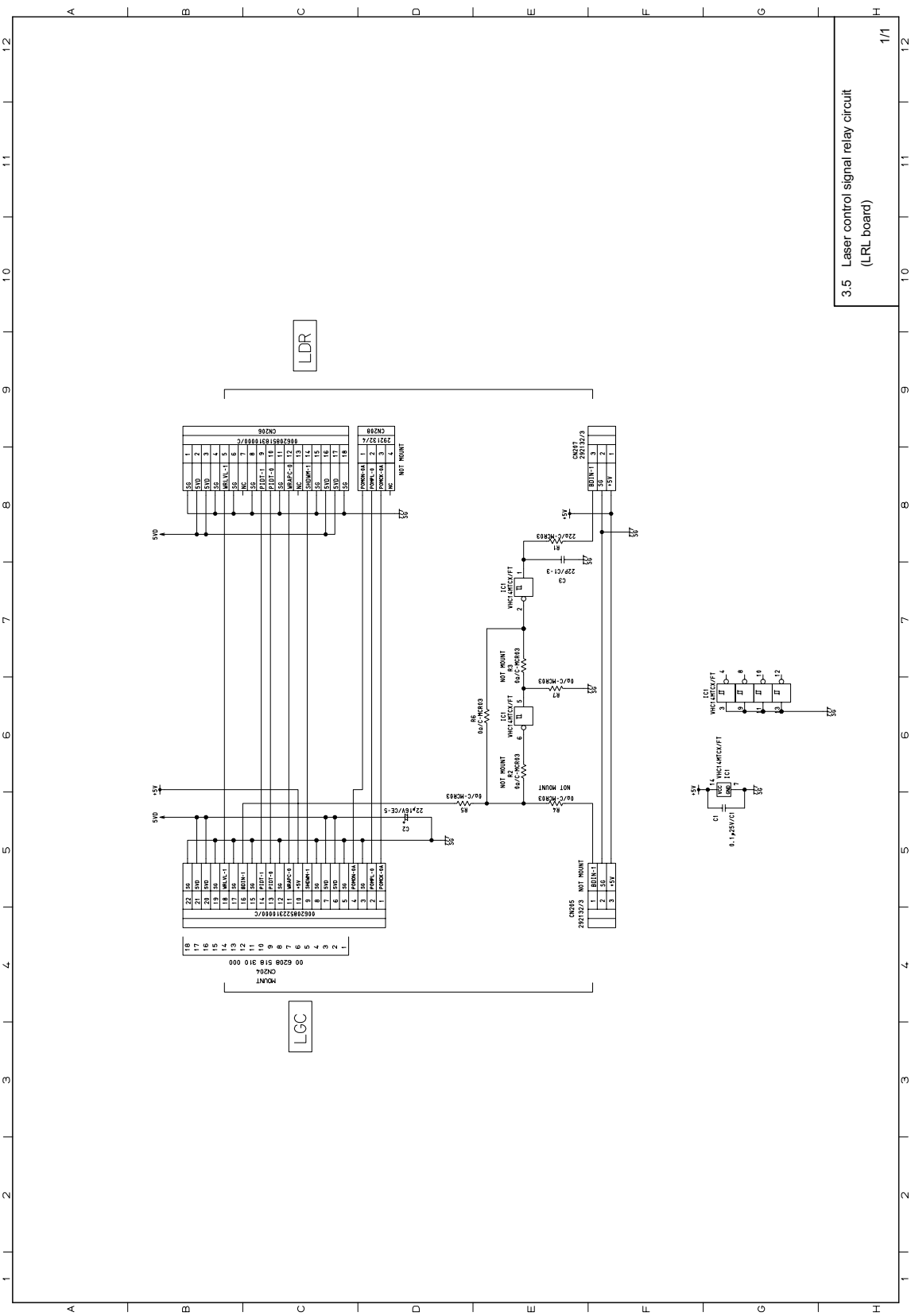


# 3.4 CCD drive circuit (CCD board)

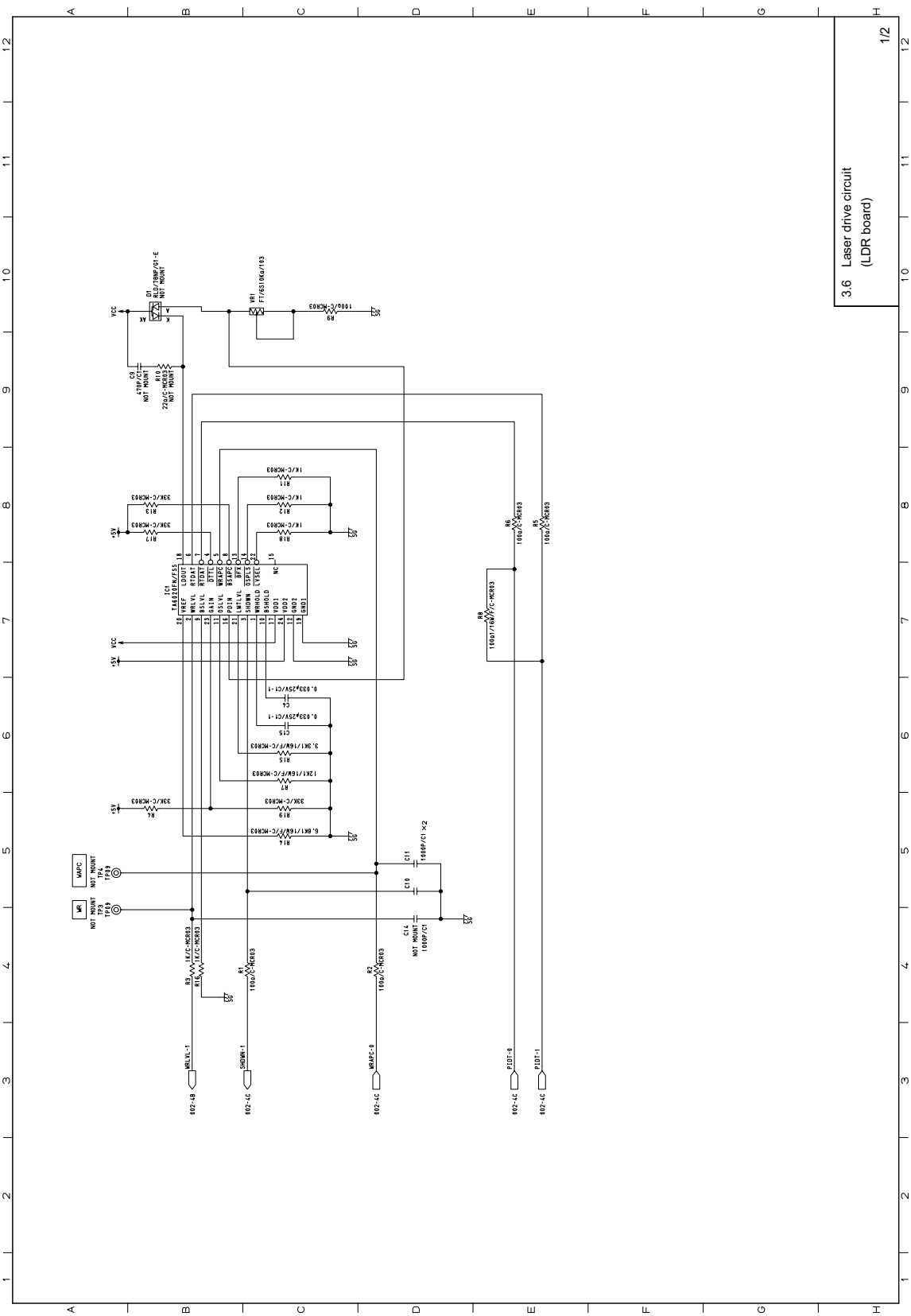


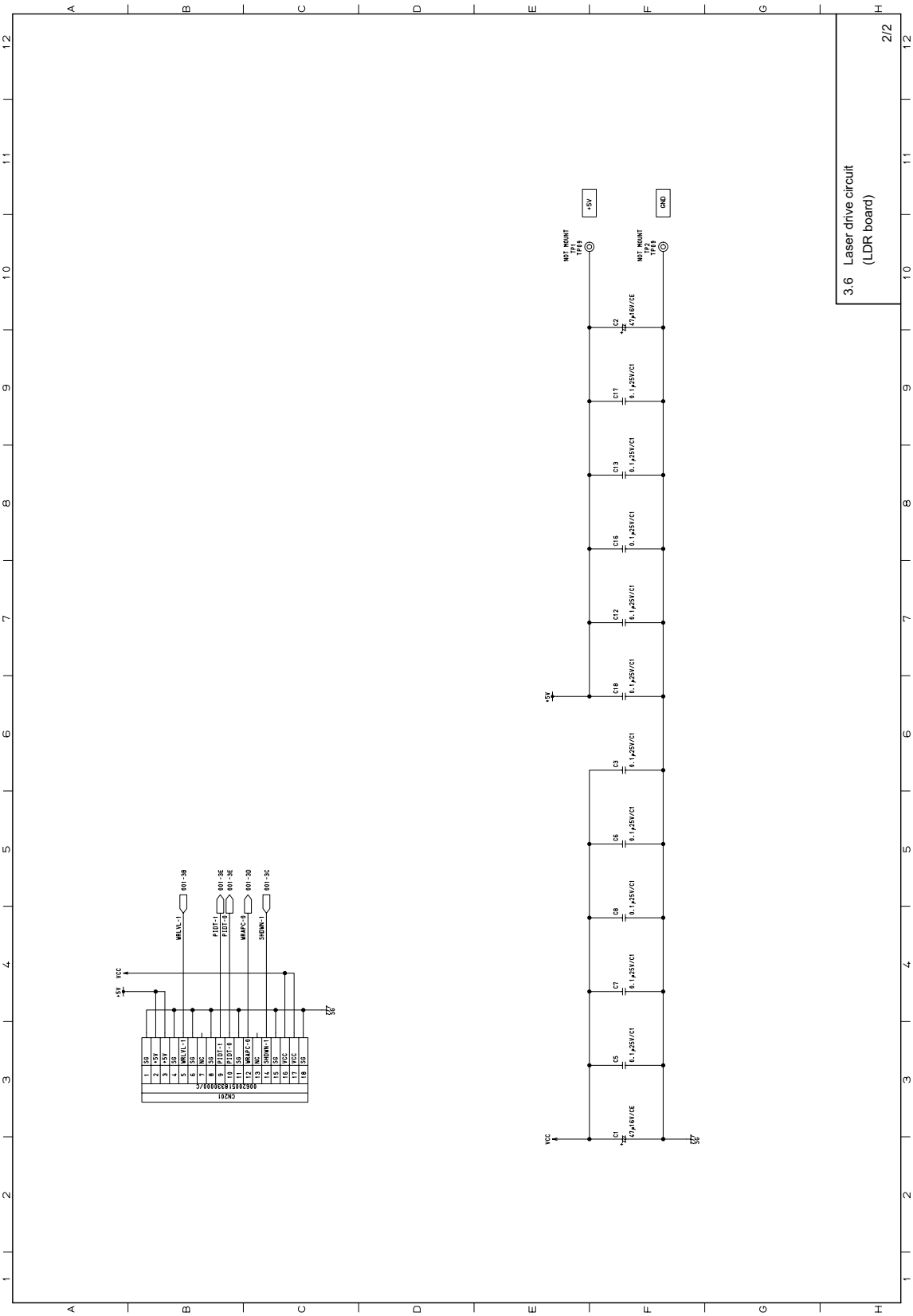


# 3.5 Laser control signal relay circuit (LRL board)

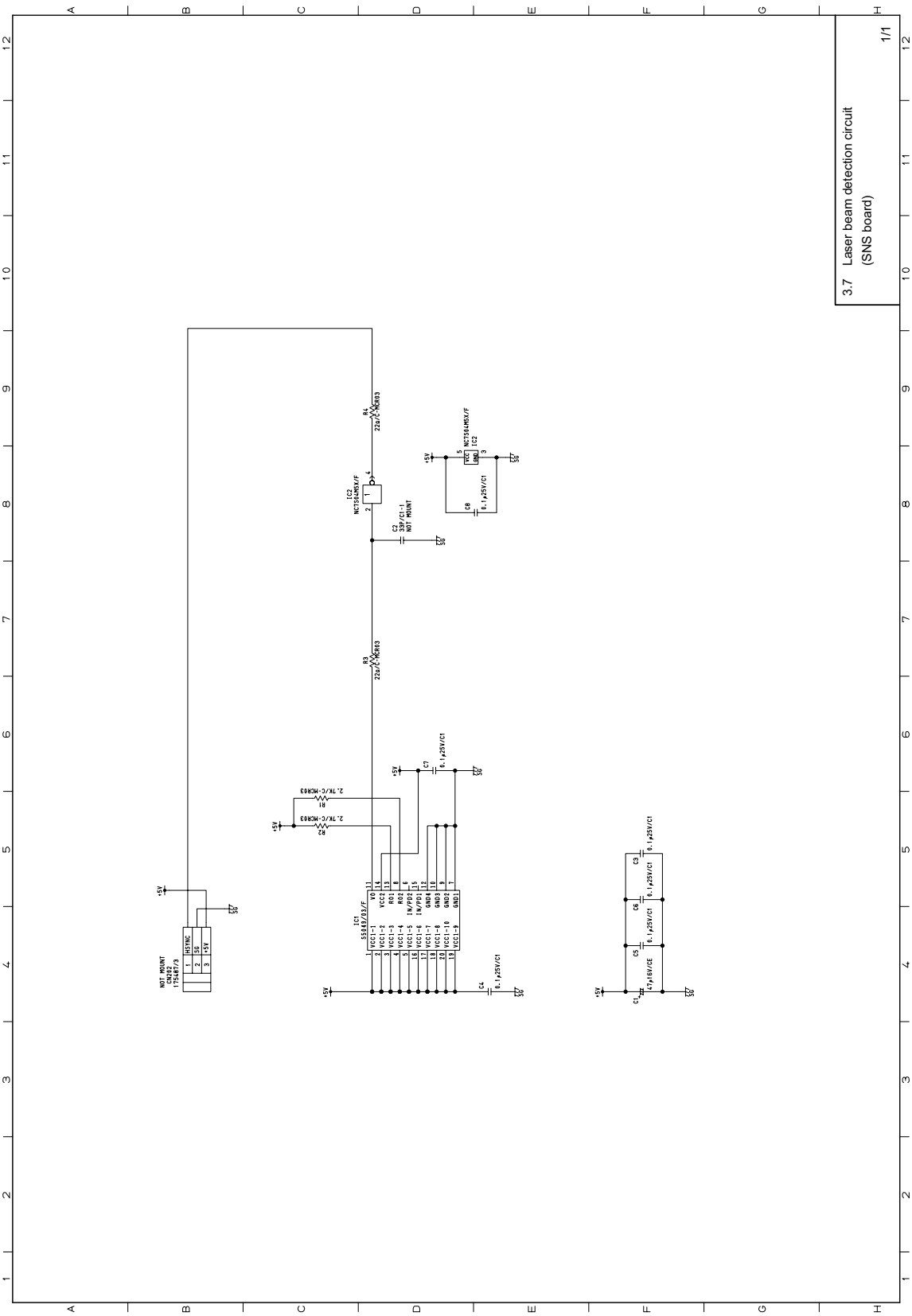


# 3.6 Laser drive circuit (LDR board)

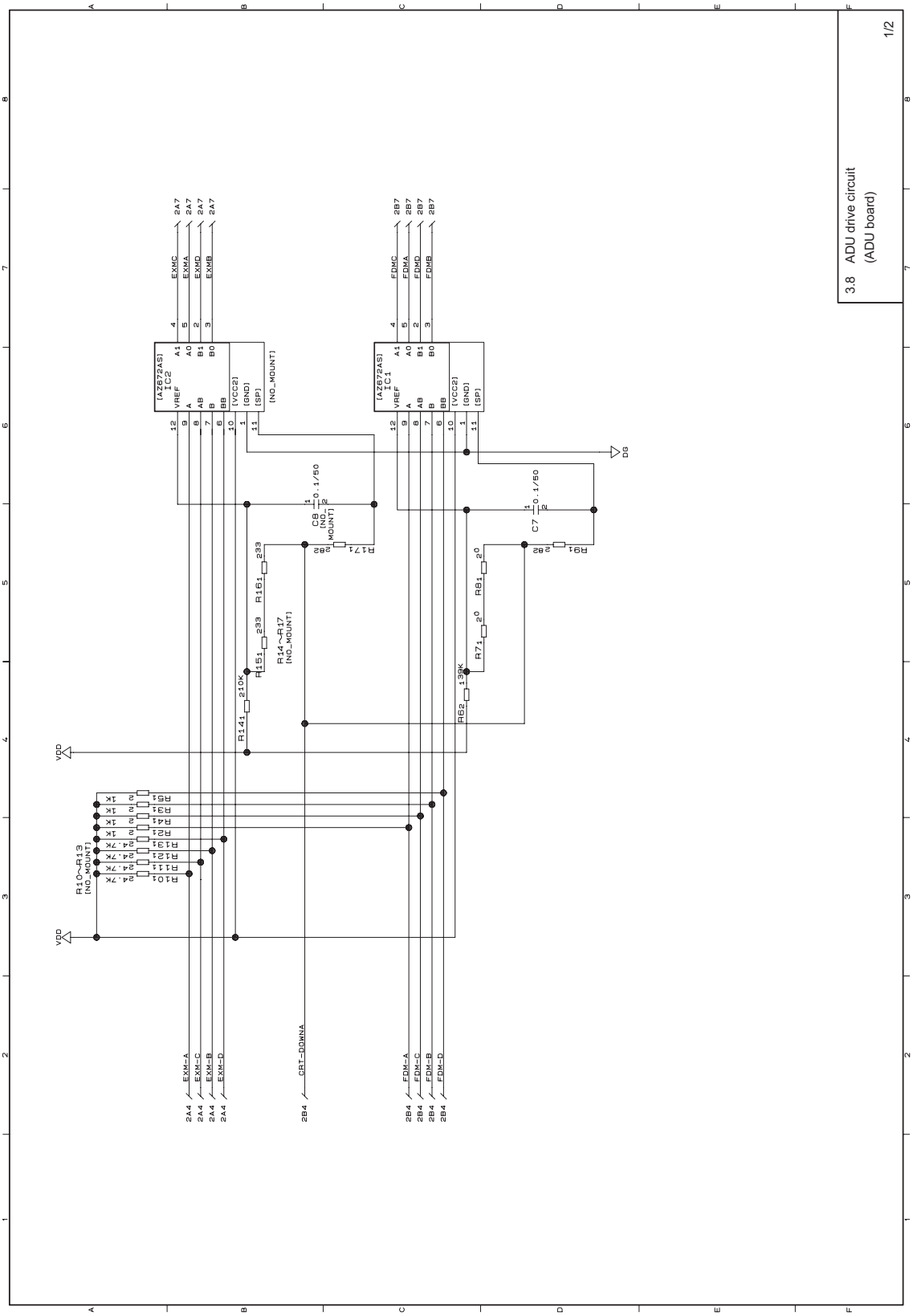


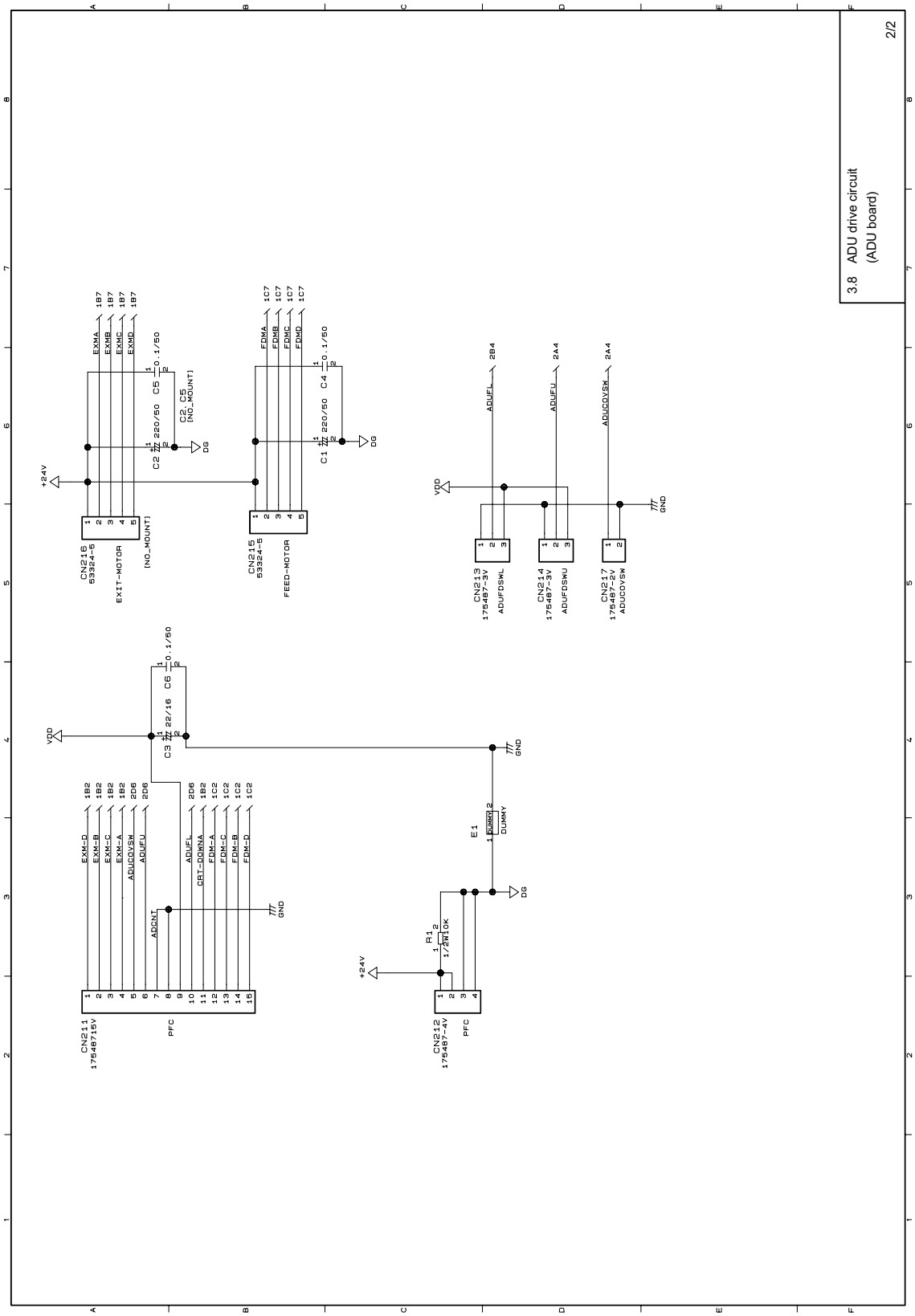


# 3.7 Laser beam detection circuit (LDR board)

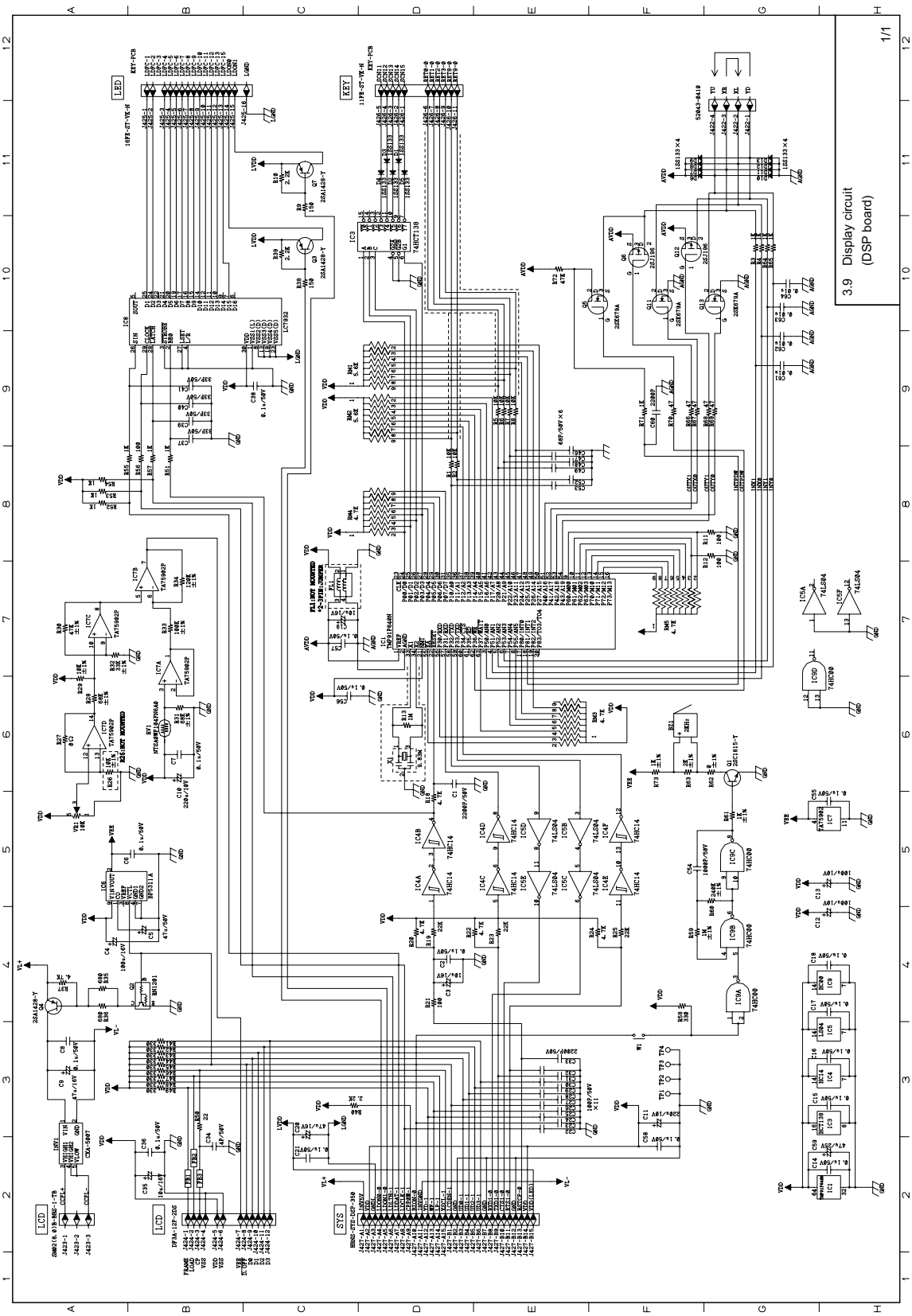


# 3.8 ADU drive circuit (ADU board)

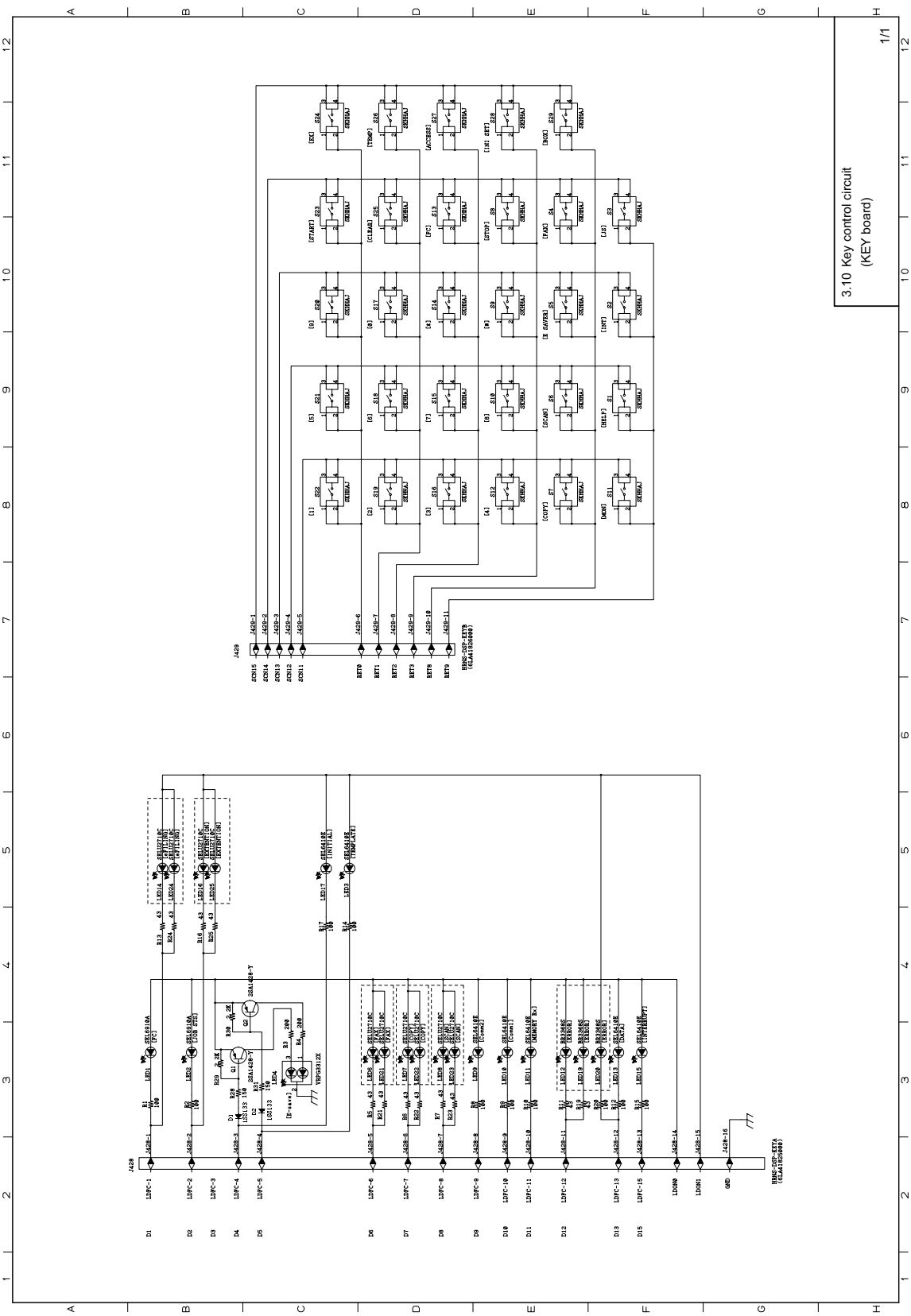




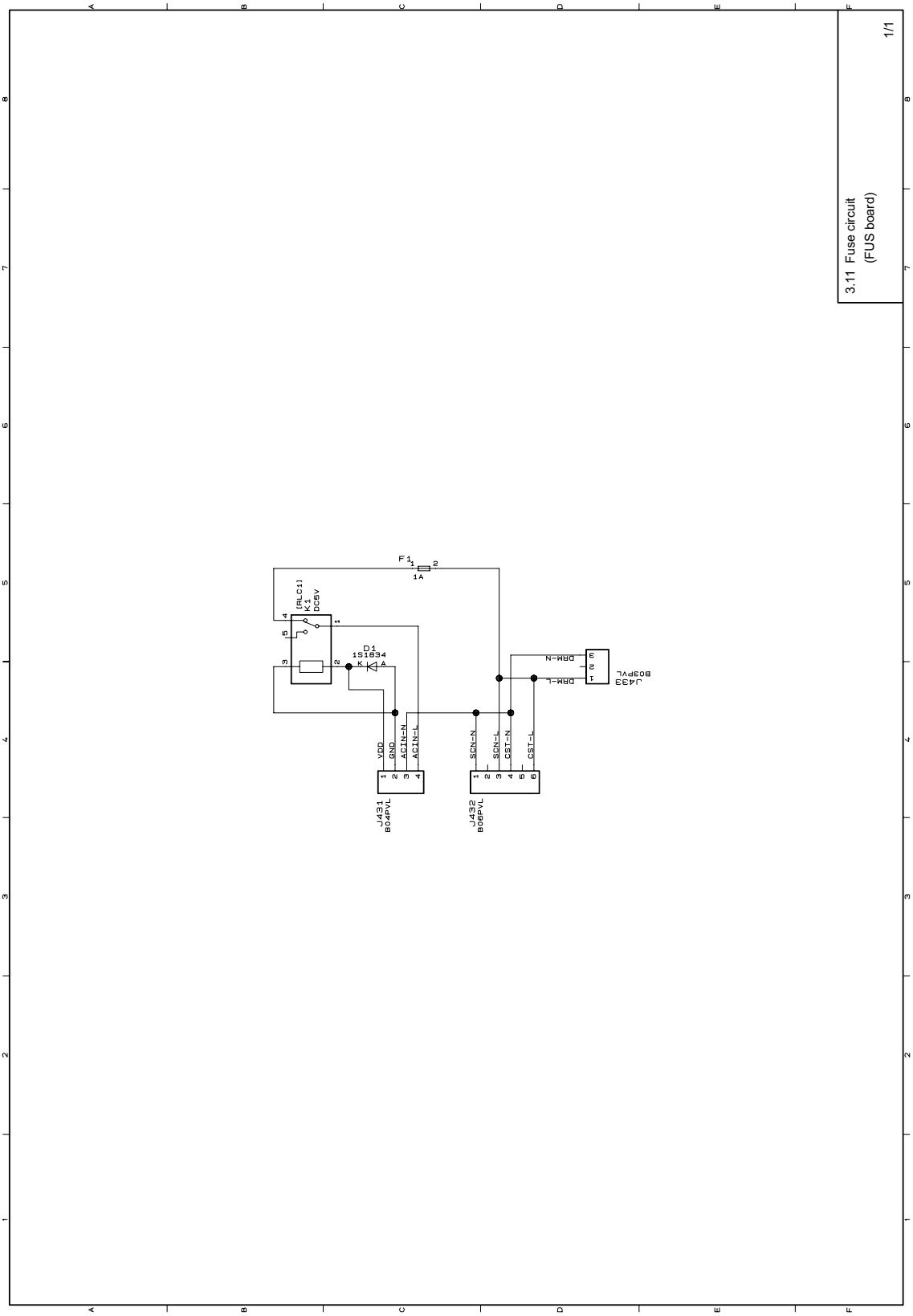
# 3.9 Display circuit (DSP board)



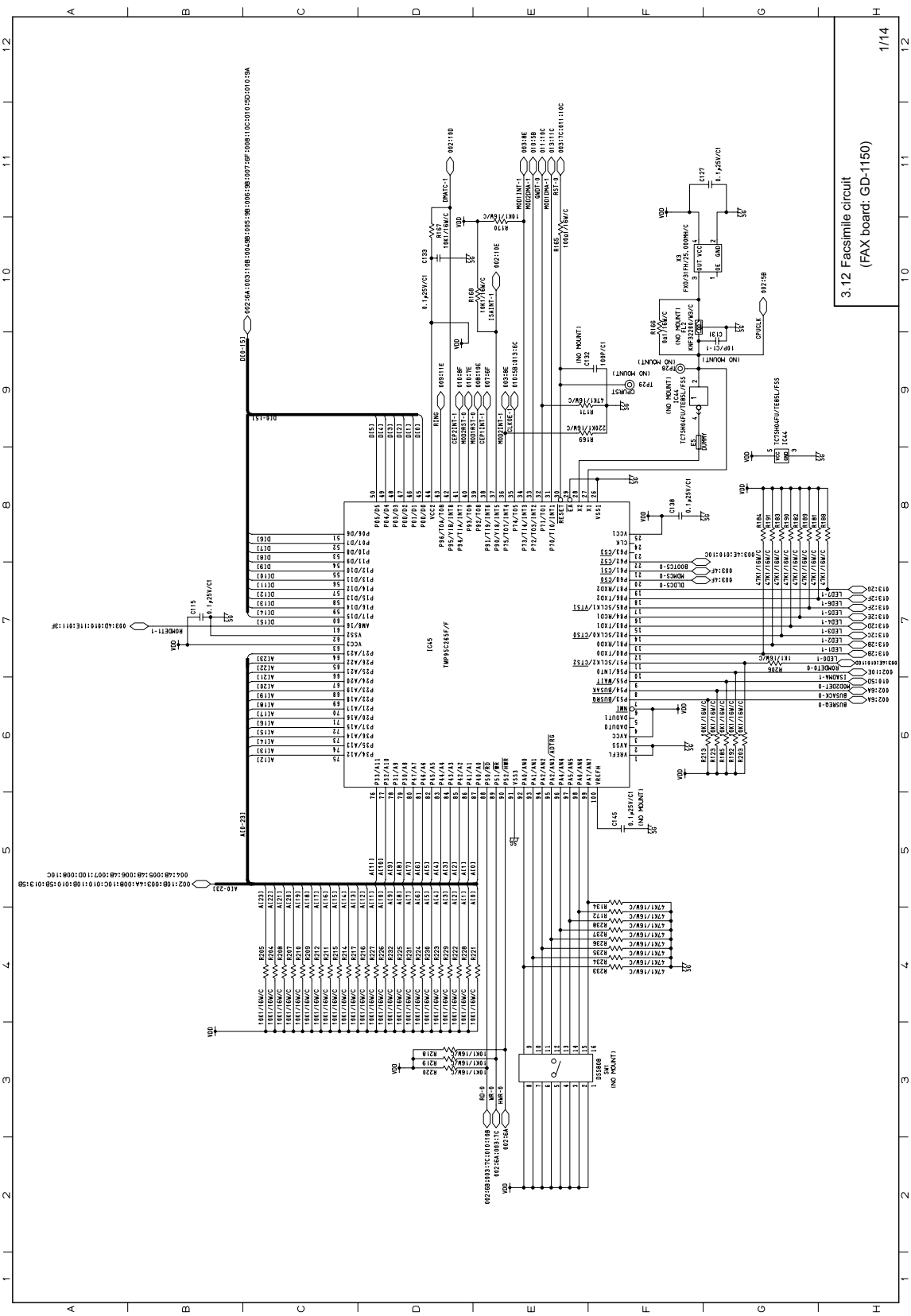
# 3.10 Key control circuit (KEY board)

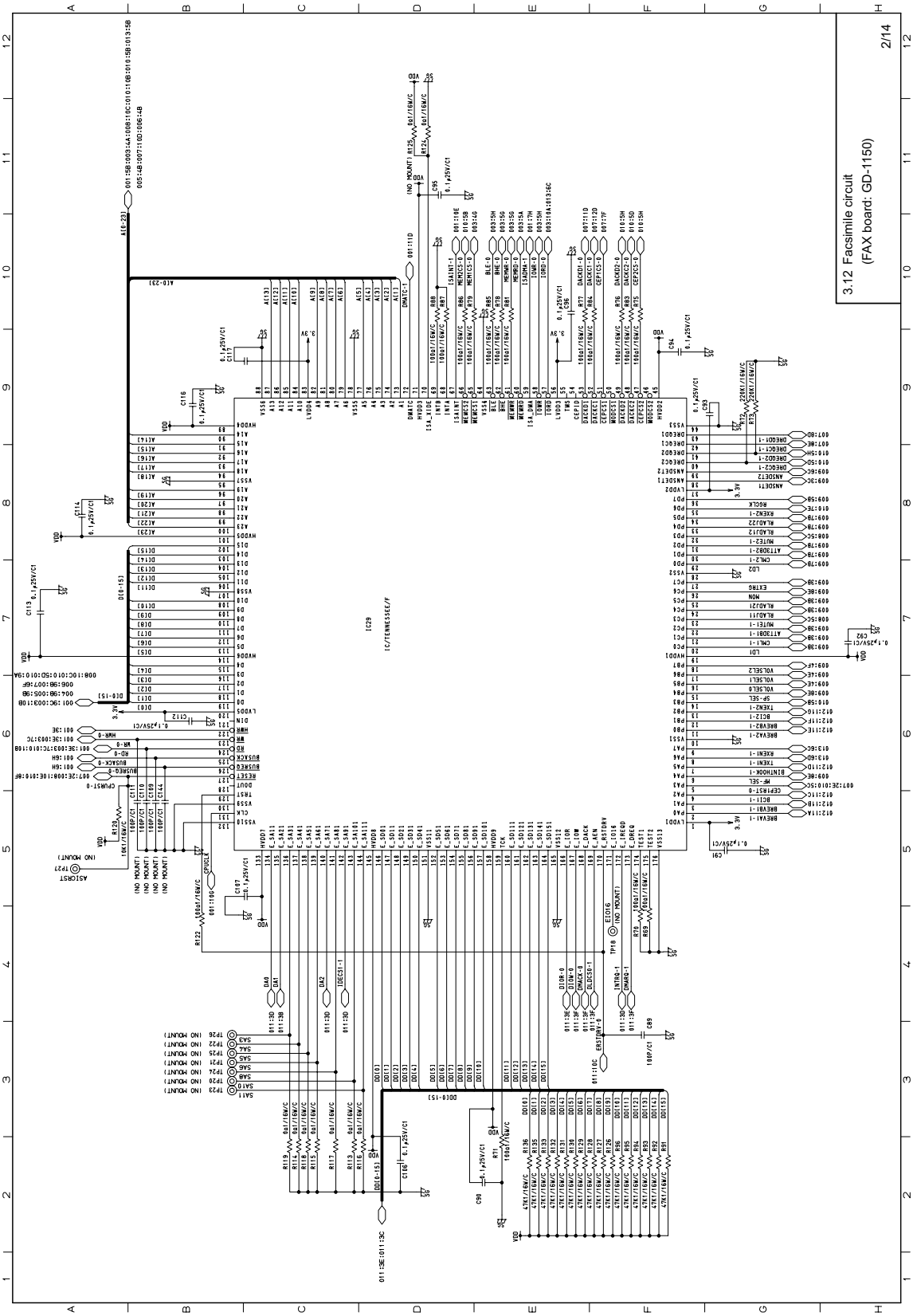


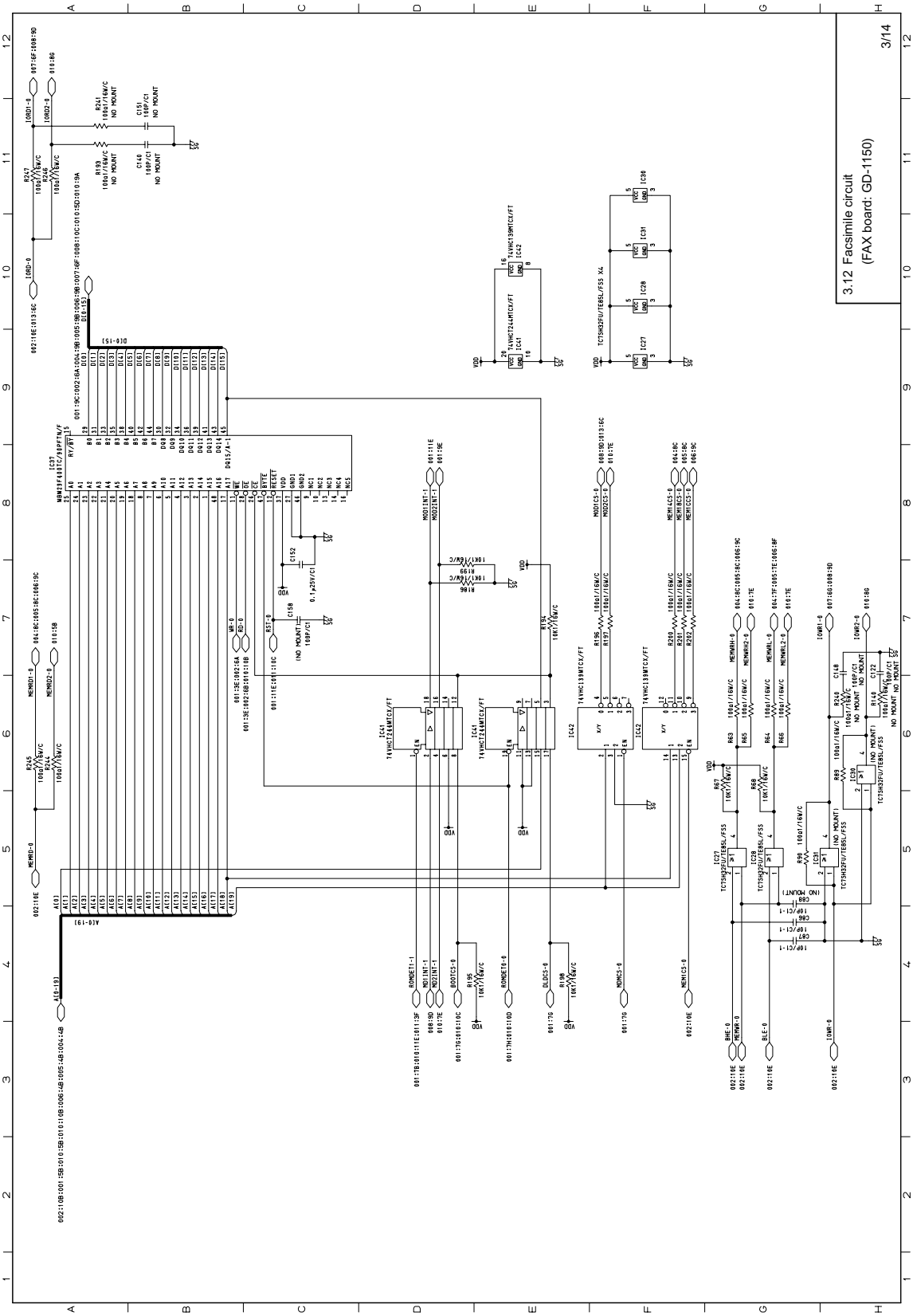
# 3.11 Fuse circuit (FUS board)

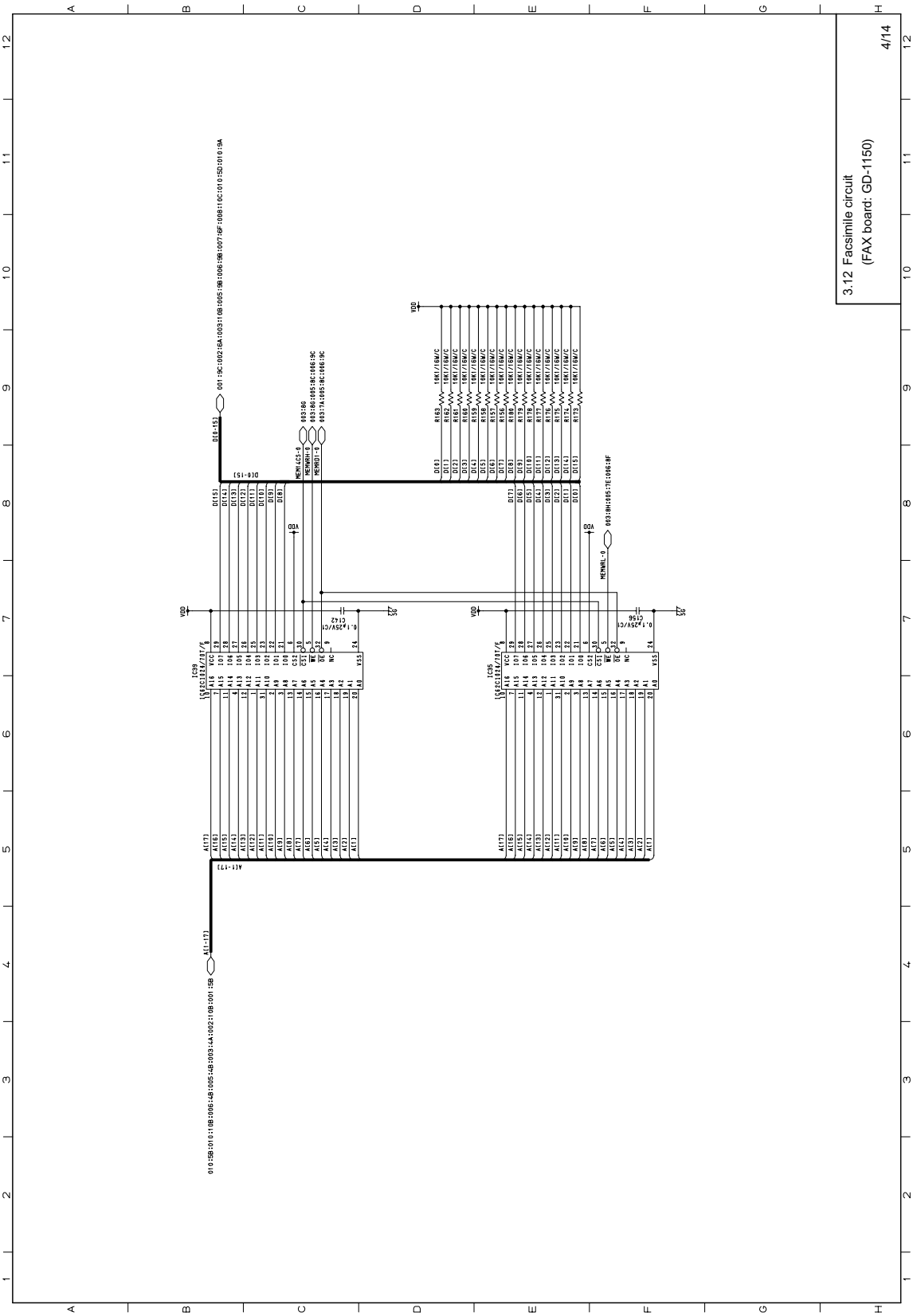


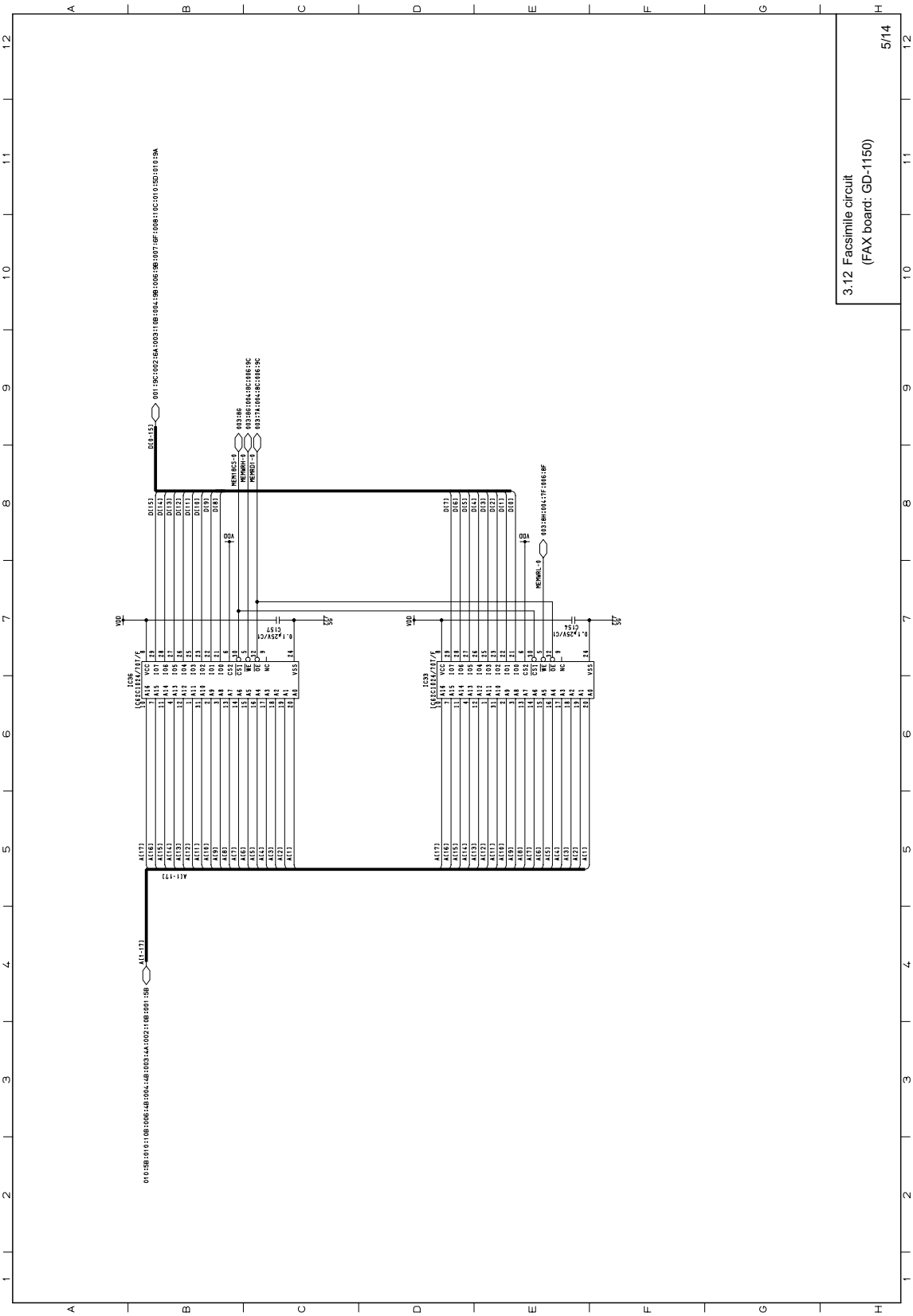
# 3.12 Facsimile circuit (FAX board: GD-1150)

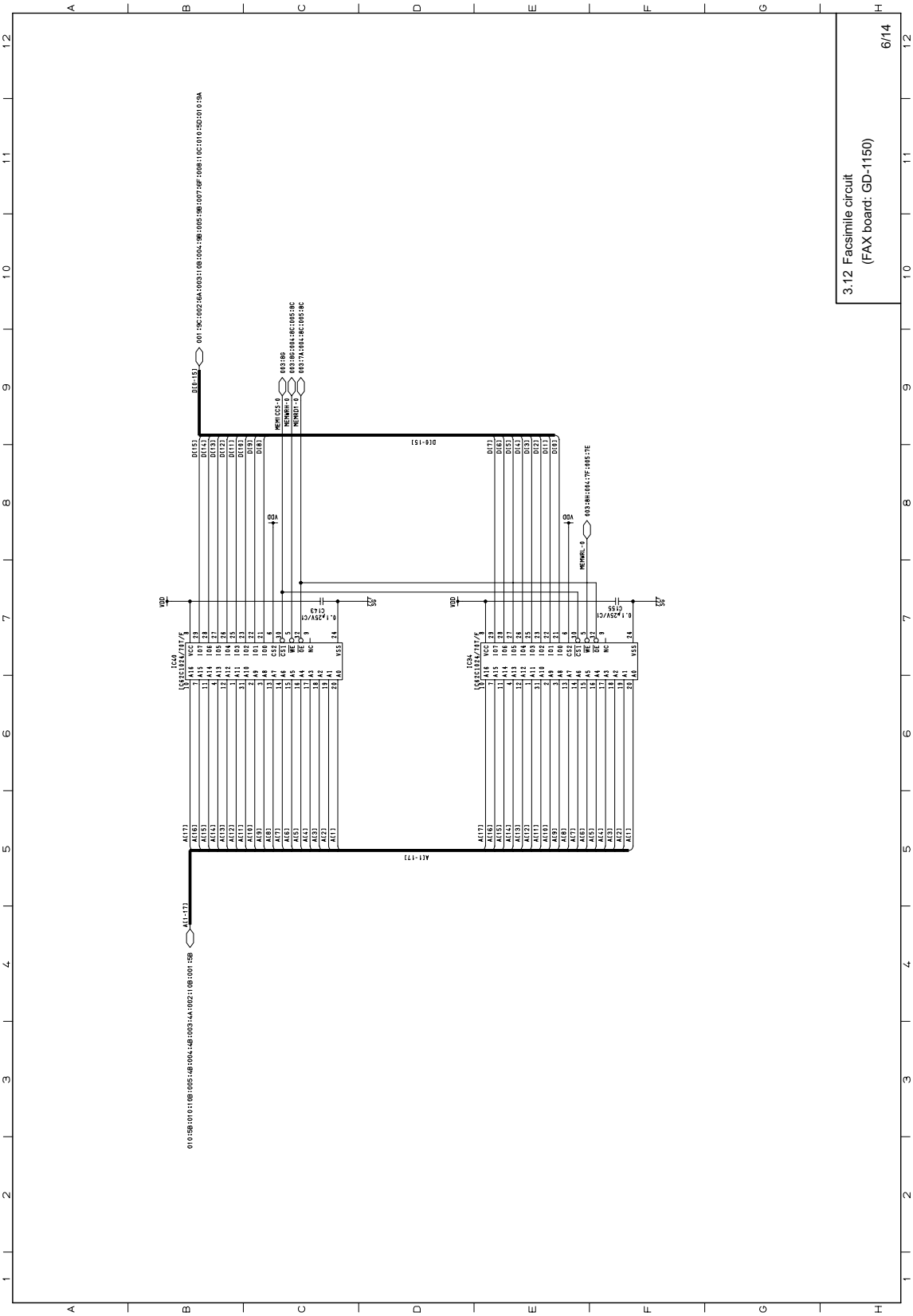












3.12 Facsimile circuit
(FAX board: GD-1150)

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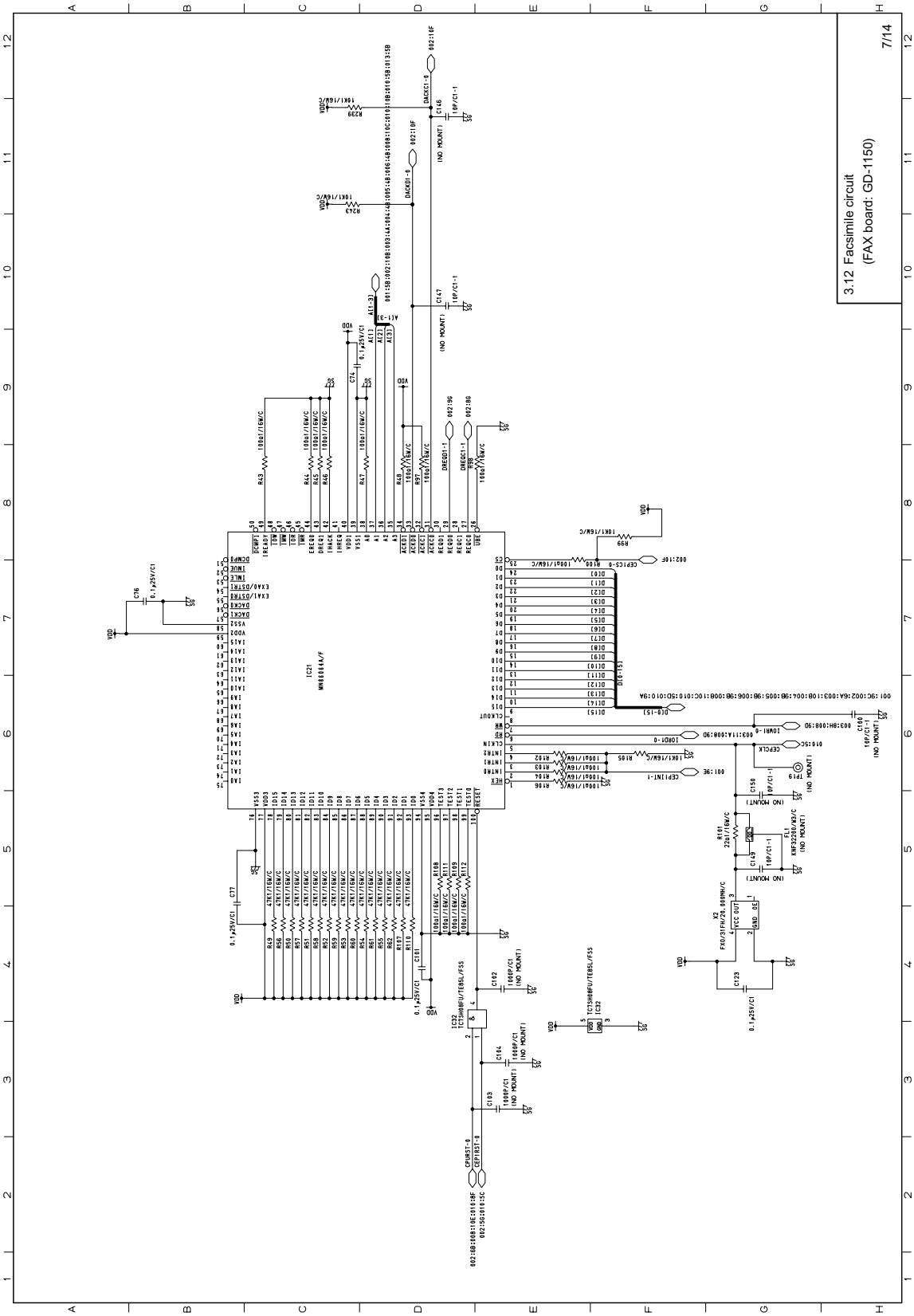
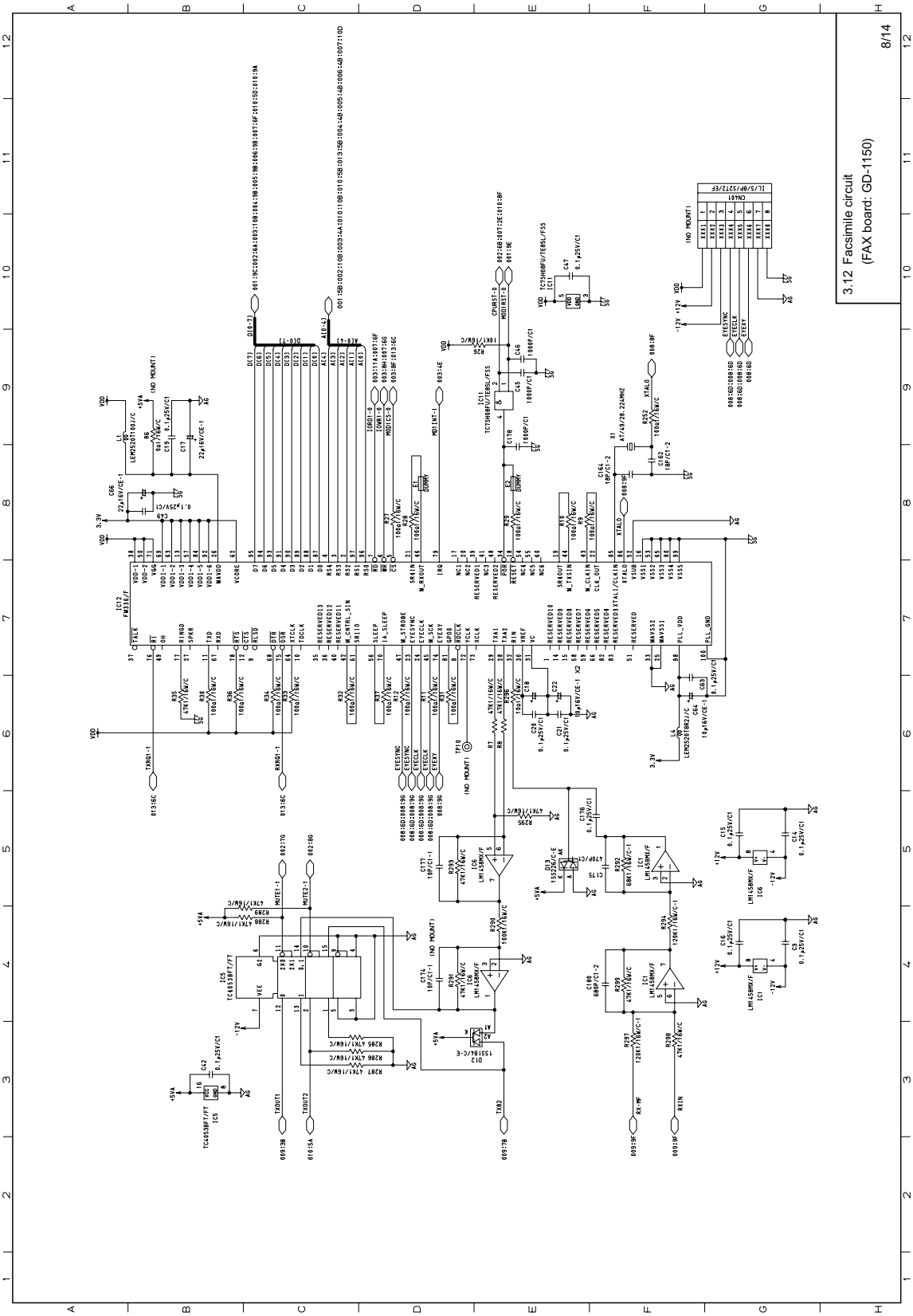
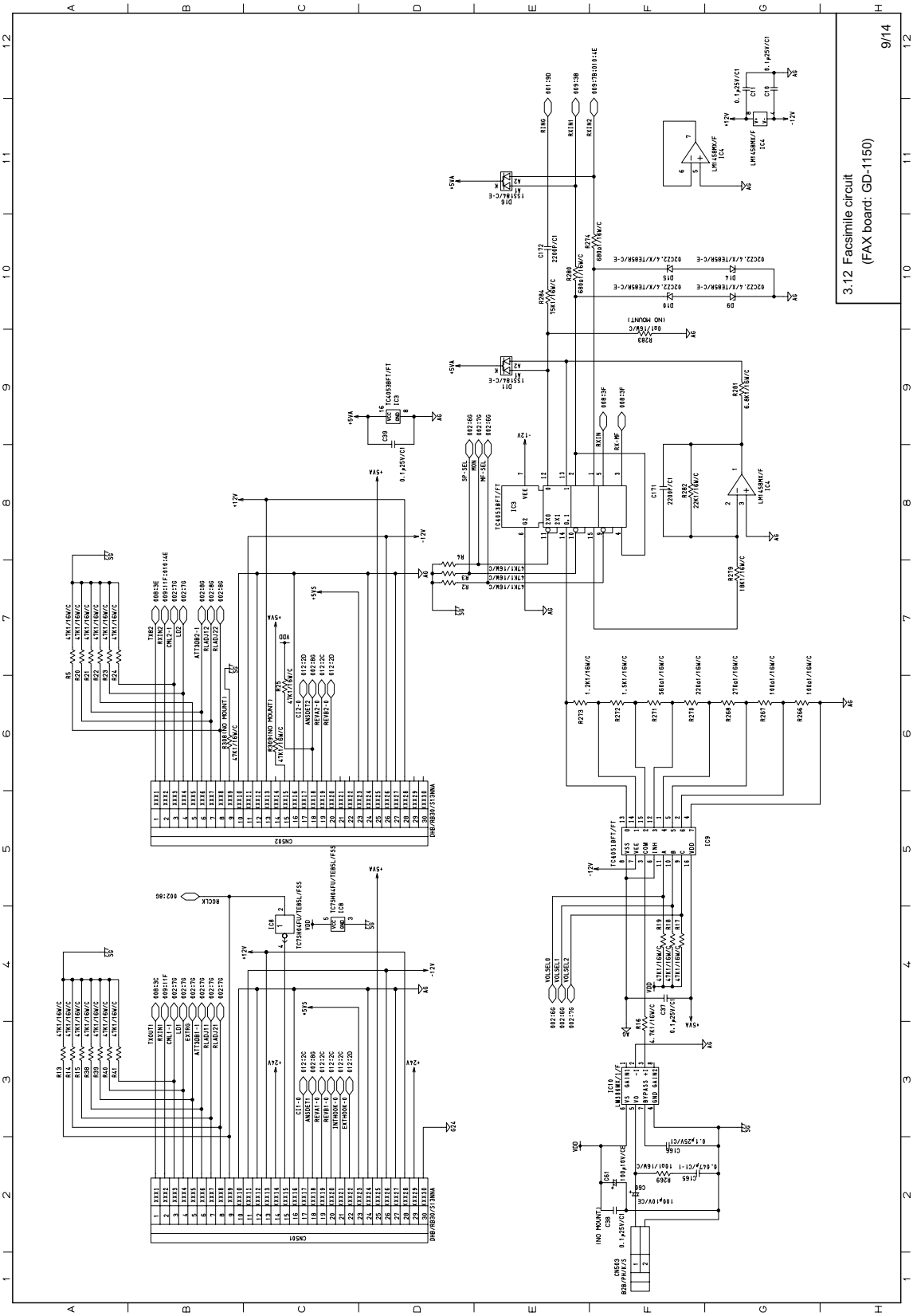
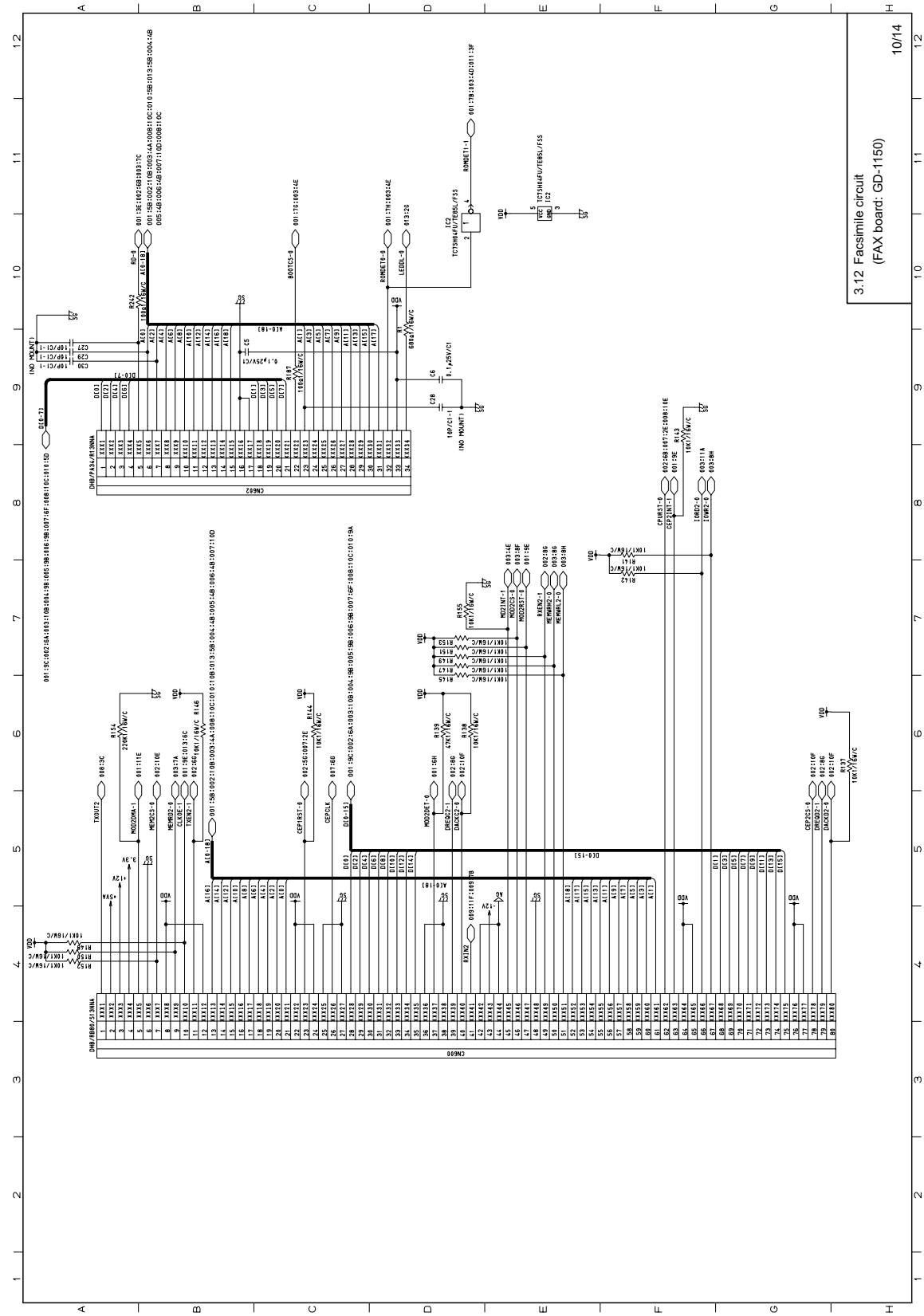


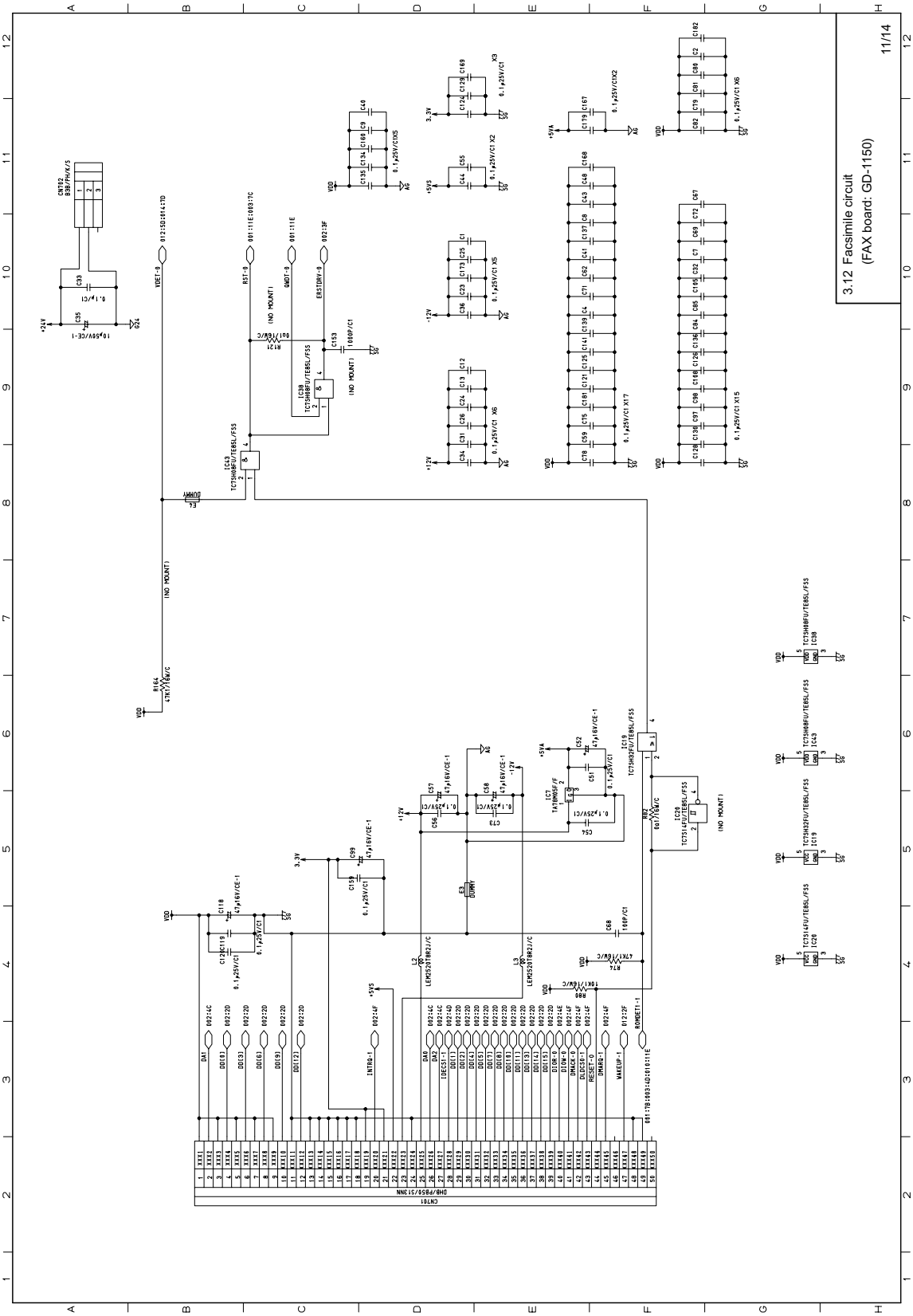


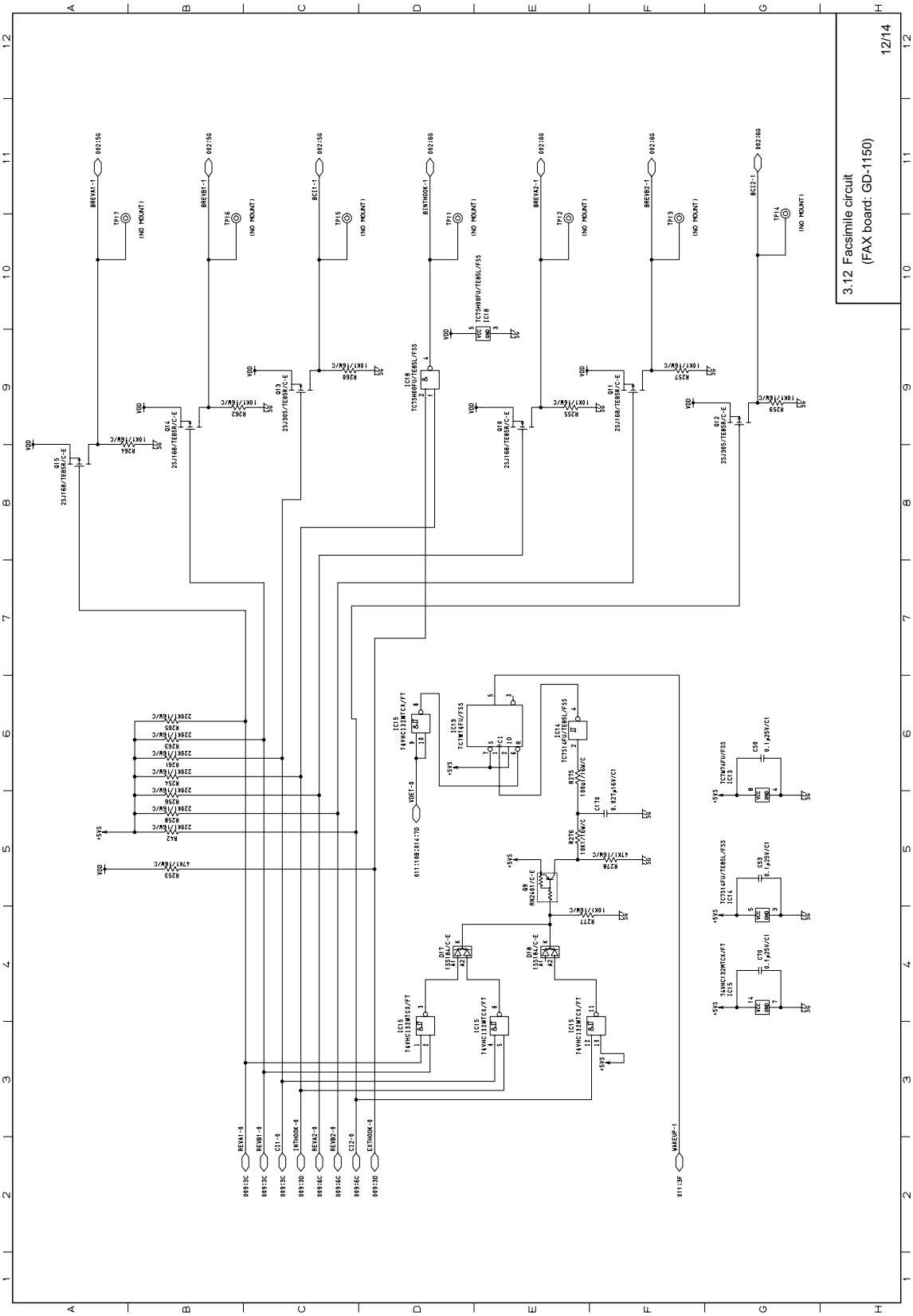
3.12 Facsimile circuit
(FAX board: GD-1150)

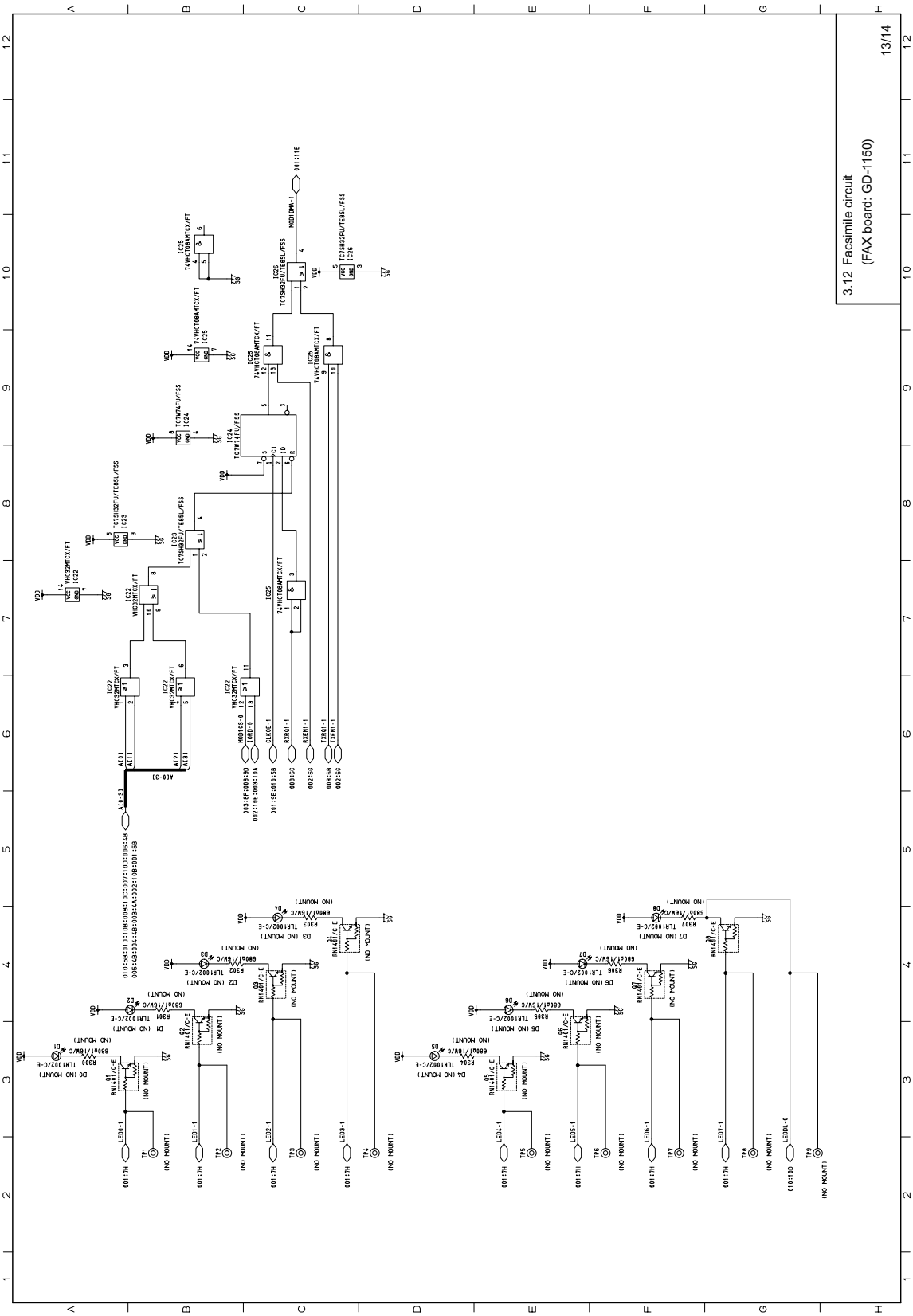
9/14

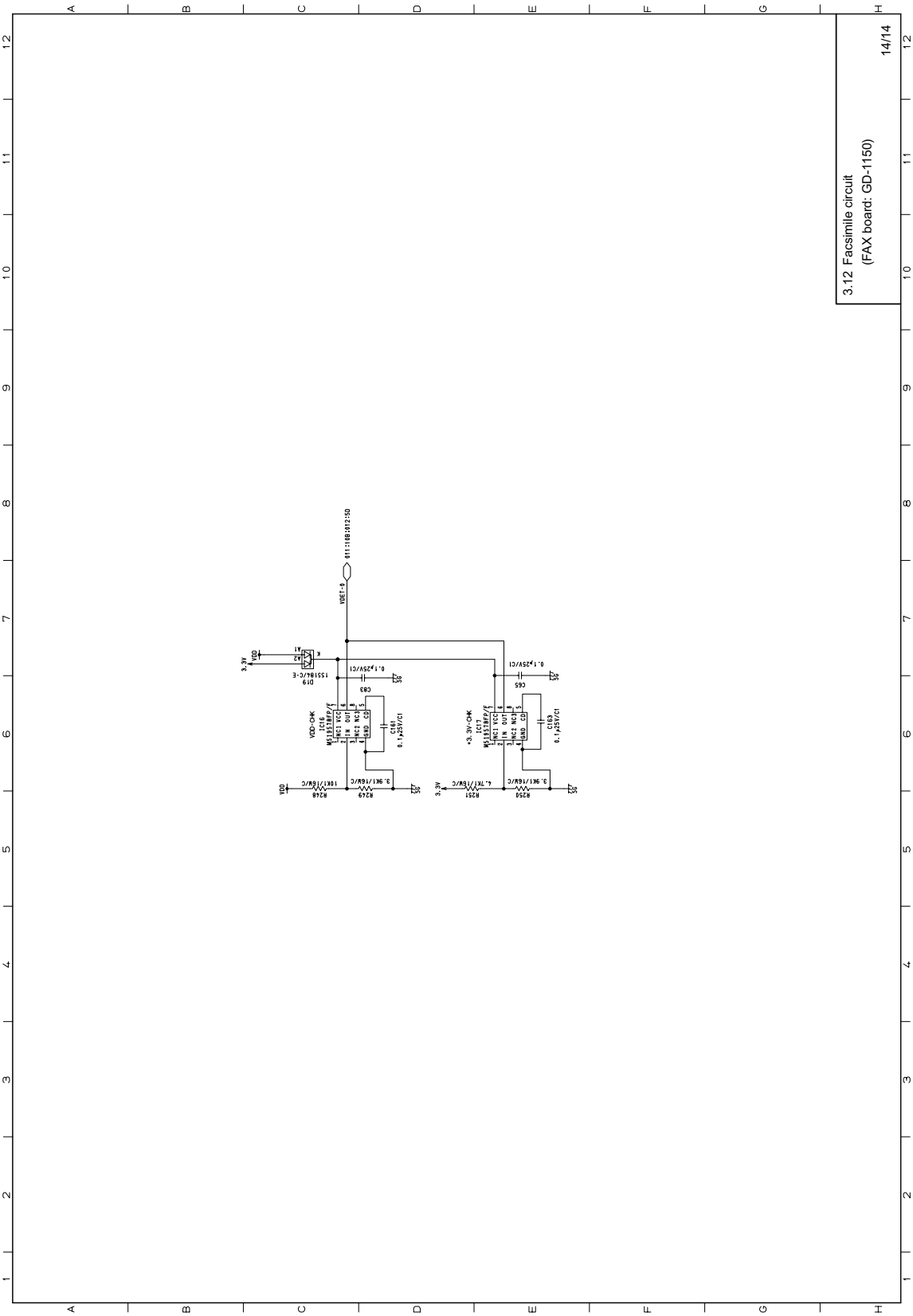




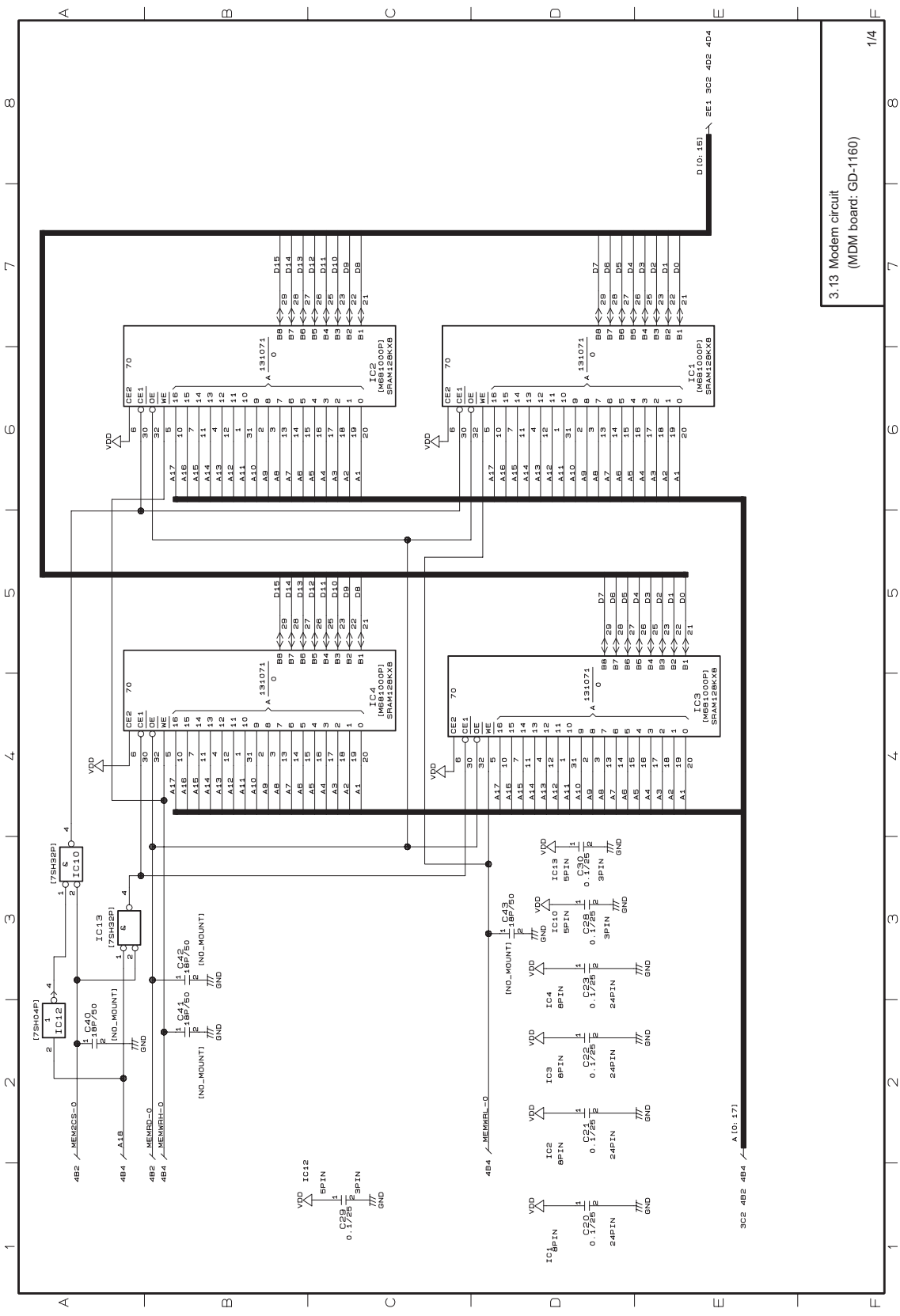


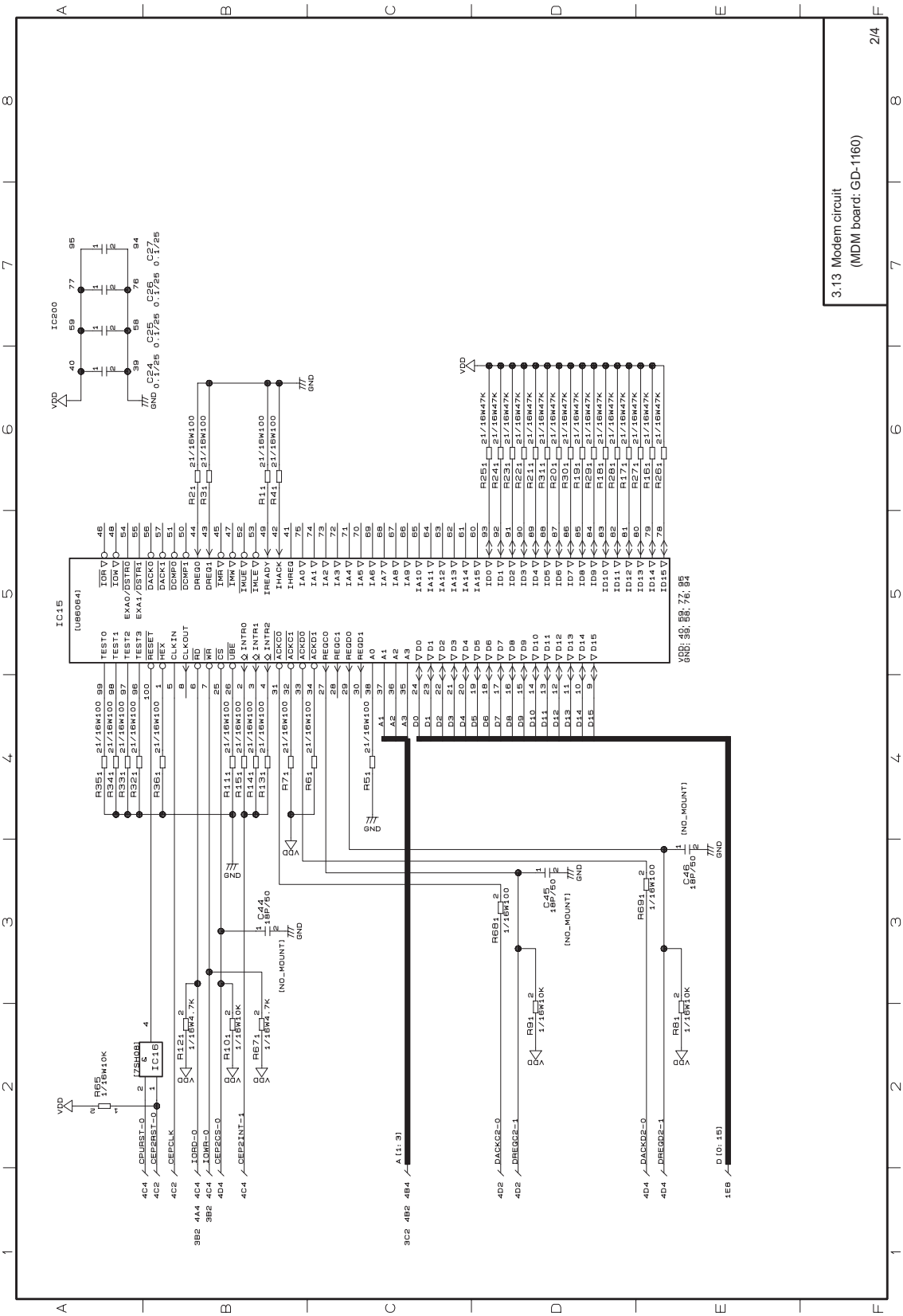


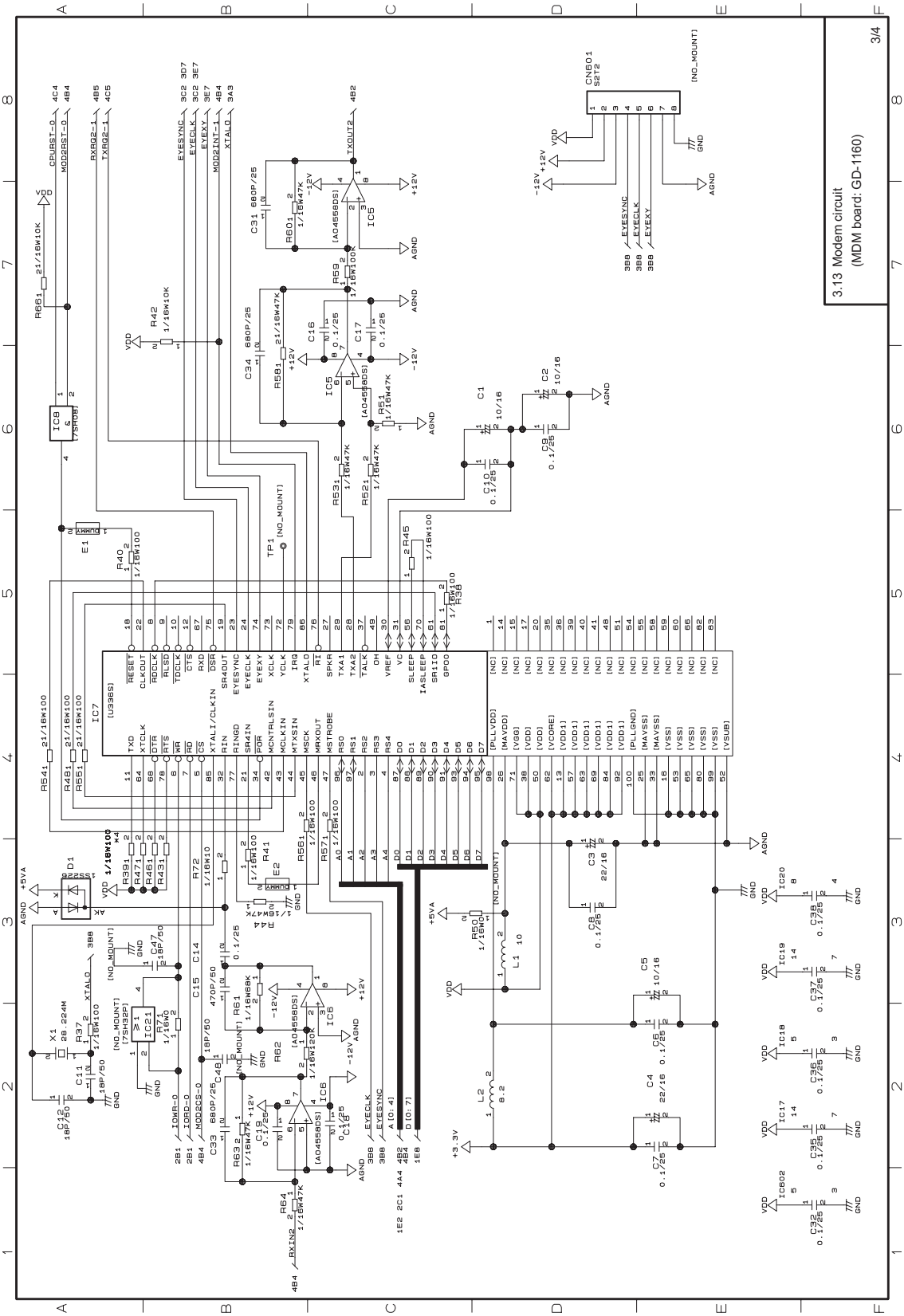


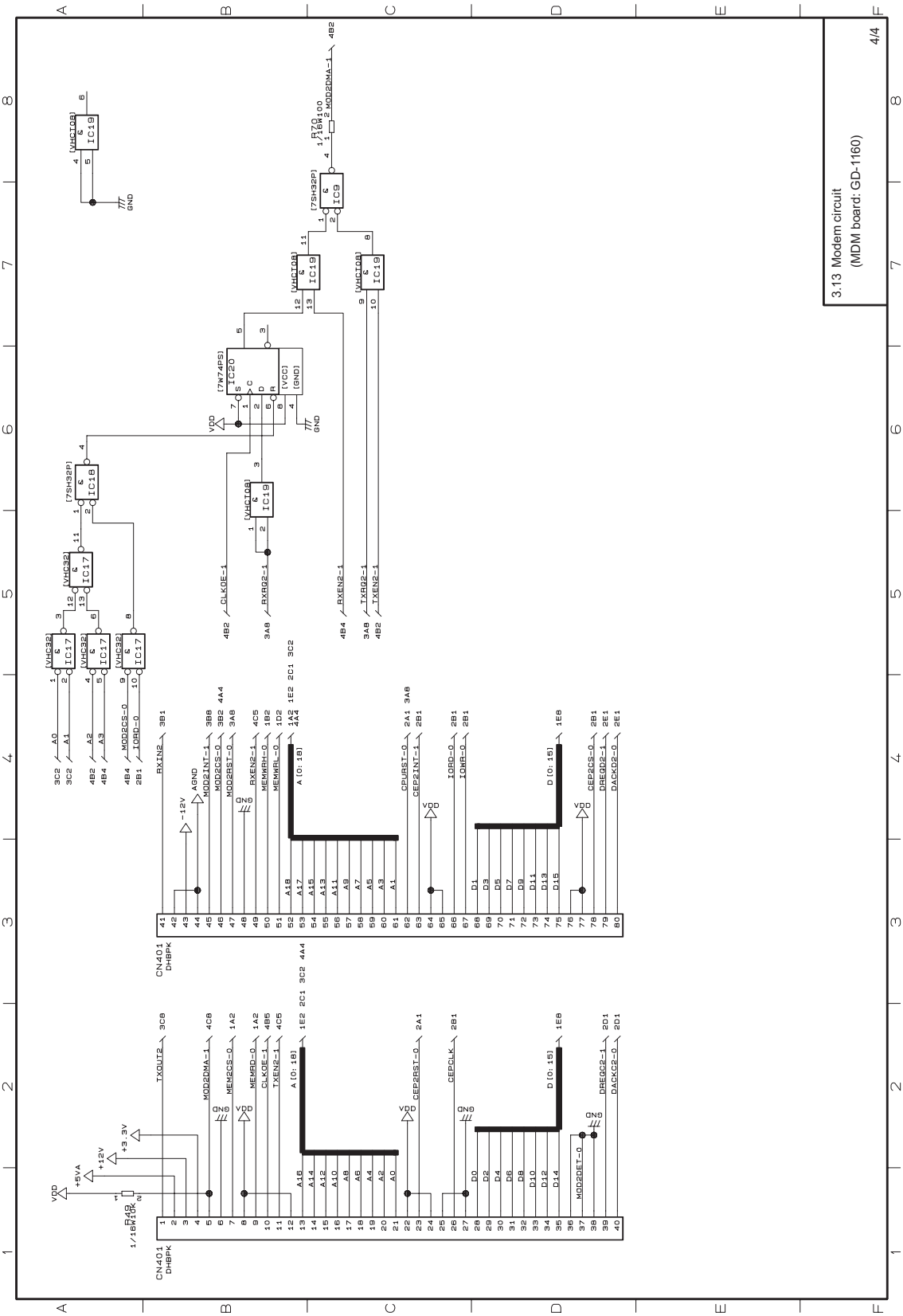


# 3.13 Modem circuit (MDM board: GD-1160)

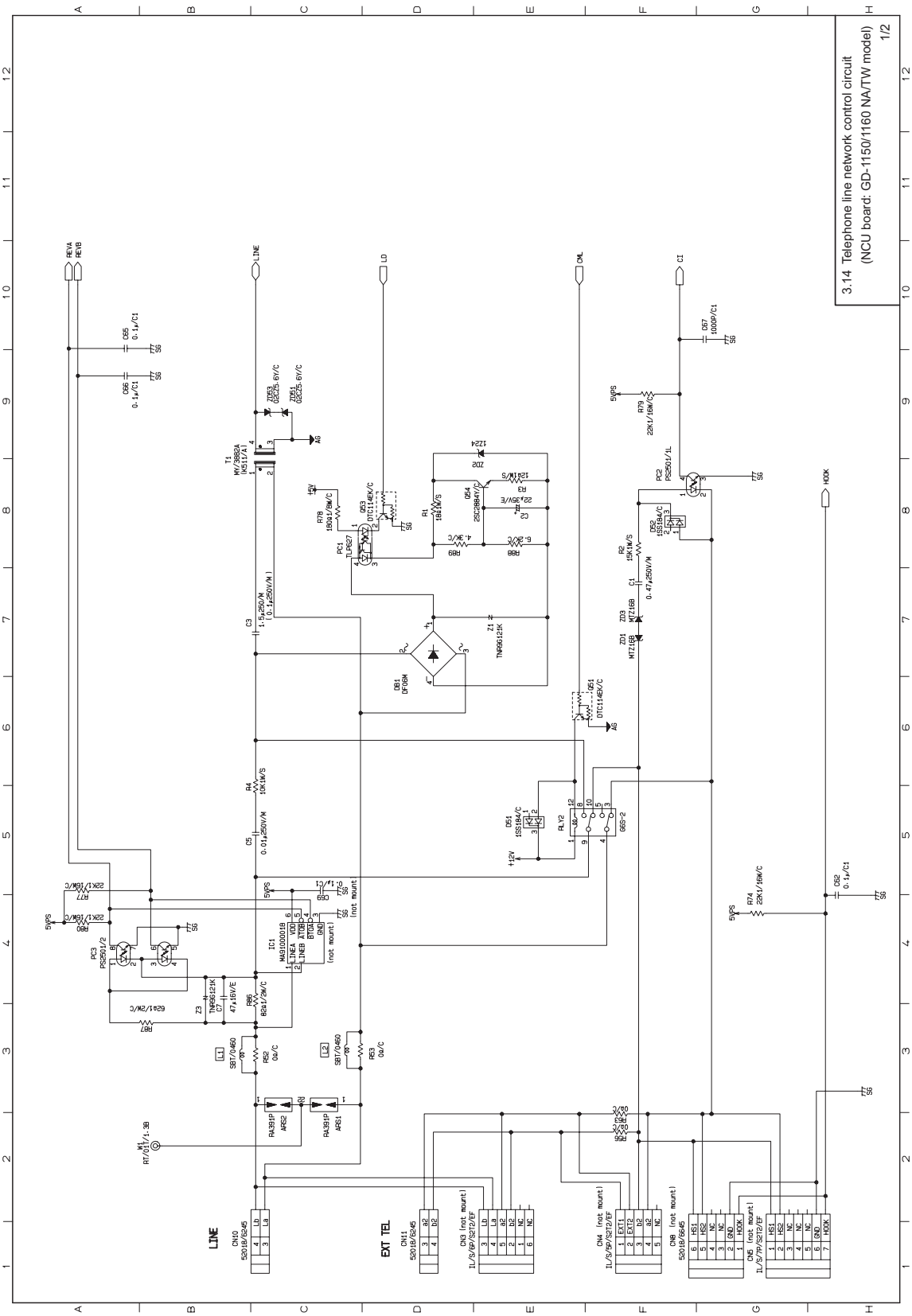


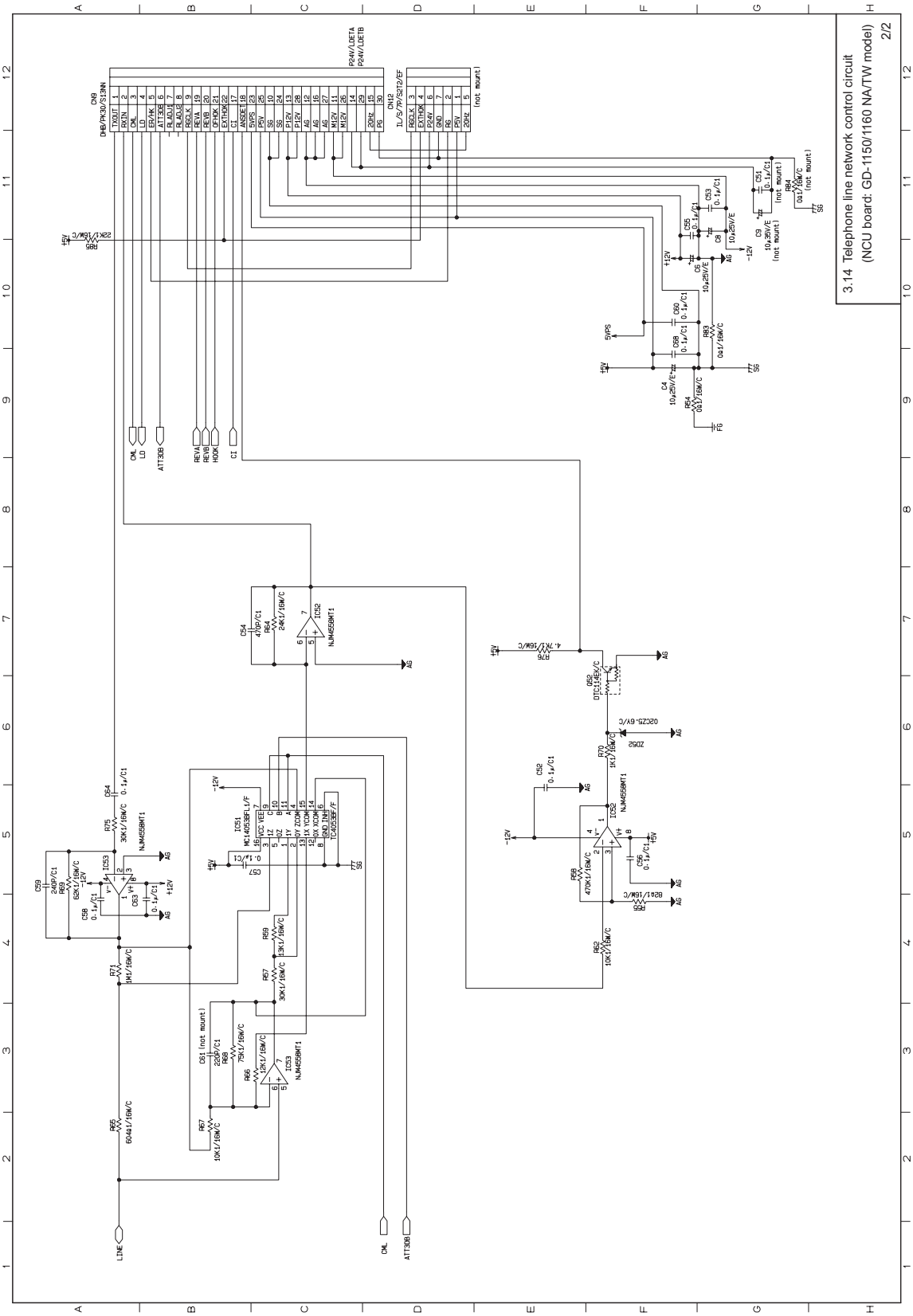




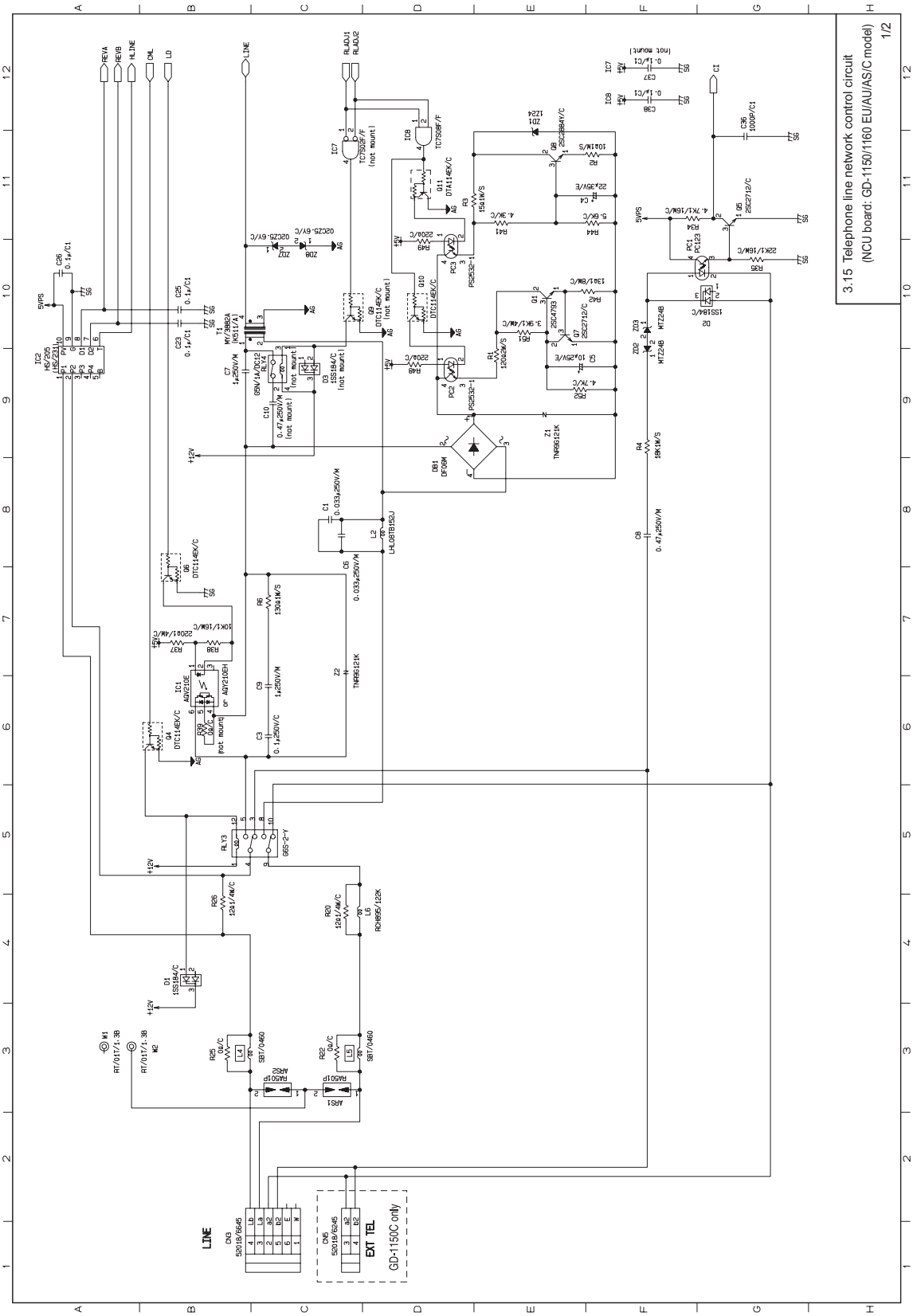


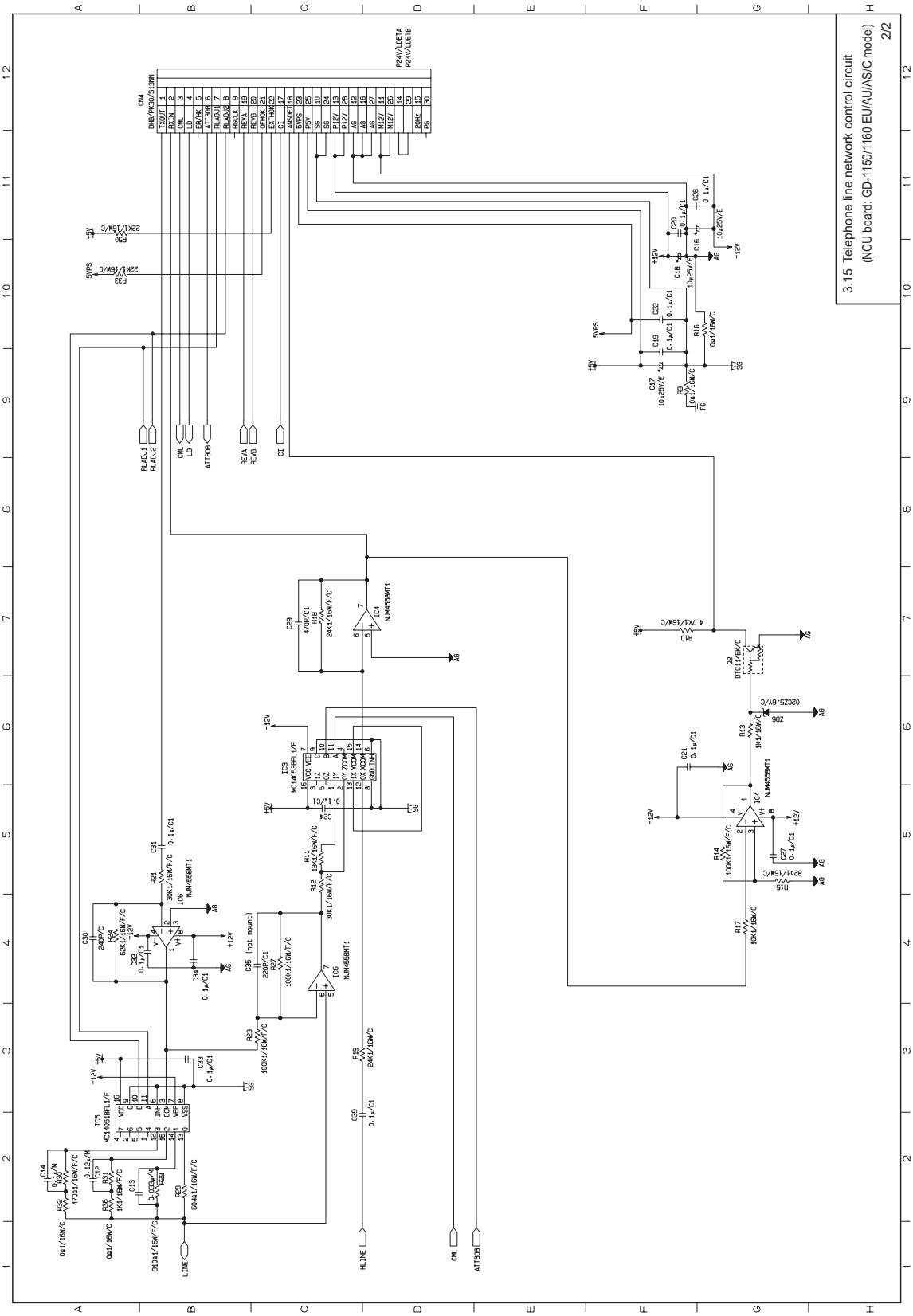
# 3.14 Telephone line network control circuit (NCU board: GD-1150/ 1160 NA/TW models)





# 3.15 Telephone line network control circuit (NCU board: GD-1150/ 1160 EU/AU/AS/C models)





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